



May 4, 1995

### **DESCRIPTION**

The WT8045 is a silicon monolithic circuit designed for synchronous signal processing and power saving detection of multi-sync display monitors, which can cope with many kinds of PC's and workstations.

It can be applied to display monitors supporting standard IBM VGA, VESA super VGA and IBM 8514/A video modes. It can also be used in other high-end display monitors supporting non-standard video modes with user-defined horizontal/vertical frequency ranges.

The WT8045 incorporates many functional circuits, including horizontal/vertical frequency discrimination, display mode selection, and synchronous pulse polarity and power saving detection, into this single chip IC.

WT8045 is more convenient for you to shrink the PC board size and to reduce the material and labor cost with fewer components.

### **FEATURES**

- Accepting two separated H&V synchronous signals with positive/ negative polarity.
- Support VESA VGA (640X480, 640X400, 640X350), VESA SVGA (800X600), European SVGA (800X600), VESA new SVGA (800X600), XGA (1024X768) and 1280x1024.
- Capable of processing horizontal frequency between 25KHZ to 80KHZ.
- Standard IBM video mode control outputs (1024X768, 640X480, 640X400, 640X350).
- Five non-standard horizontal frequency control outputs in predefined frequency range.
- Power saving mode - It can detect the conditions of monitor to decide which one will be selected as following: ON/STANDBY/SUSPEND/OFF mode.
- Fixed polarity outputs on both horizontal and vertical synchronous signals.

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**Weltrend Semiconductor, Inc.**

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## WT8045

Synchronous Signal Discriminator and  
Power Saving Detector for Green Monitor

- Power supply voltage: DC 5 volts; but for those pins with open-drain structure, such like the mode select control output and frequency discrimination control output pins, can be connected to 12 volts through pull-high resistor.

### APPLICATION

- Auto size control for Multi-Sync Display Monitors

### ORDERING INFORMATION

| Part No.    | Package            | Note                 |
|-------------|--------------------|----------------------|
| WT8045N24P1 | P-DIP 24L          | V * 128              |
| WT8045N24P3 | P-DIP 24L          | Without Mute         |
| WT8045N24P4 | P-DIP 24L          | Without Mute         |
| WT8045N24P5 | P-DIP 24L          | V * 1                |
| WT8045N24P6 | P-DIP 24L          | With Mute            |
| WT8045N24P7 | P-DIP 24L          | Without Mute         |
| WT8045N24P8 | P-DIP 24L          | With Mute            |
| WT8045N28P1 | P-DIP 28L (skinny) | V * 128 Without Mute |
| WT8045N28P2 | P-DIP 28L (skinny) | V * 128 Without Mute |
| WT8045N28P3 | P-DIP 28L (skinny) | V * 1 Without Mute   |
| WT8045N28P4 | P-DIP 28L (skinny) | V * 128 With Mute    |
| WT8045N28P5 | P-DIP 28L (skinny) | V * 1 With Mute      |
| WT8045N28P6 | P-DIP 28L (skinny) | V * 1 Without Mute   |
| WT8045N28P7 | P-DIP 28L (skinny) | V * 128 With Mute    |
| WT8045N28P8 | P-DIP 28L (skinny) | V * 1 With Mute      |
| WT8045N32   | P-DIP 32L          | --                   |

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## PIN CONFIGURATION

**WT8045N24P1**

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 24 | VDD             |
| OSCout | 2  | 23 | 1024x768(56.5K) |
| HSin   | 3  | 22 | 1024x768 (NI)   |
| VSin   | 4  | 21 | 1024x768 (I)    |
| H_out  | 5  | 20 | 800x600(48K)    |
| V_out  | 6  | 19 | 800x600(37.5K)  |
| F43.5K | 7  | 18 | 800x600(35.2K)  |
| F36.2K | 8  | 17 | 640x480         |
| F33K   | 9  | 16 | 640x400         |
| QV128  | 10 | 15 | 640x350         |
| QVRC   | 11 | 14 | QH              |
| Vss    | 12 | 13 | QHRC            |

**WT8045N24P3**

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 24 | VDD             |
| OSCout | 2  | 23 | 1024x768(56.5K) |
| HSin   | 3  | 22 | 1024x768 (NI)   |
| VSin   | 4  | 21 | 1024x768 (I)    |
| H_out  | 5  | 20 | 800x600(48K)    |
| V_out  | 6  | 19 | 800x600(37.5K)  |
| F43.5K | 7  | 18 | 800x600(35.2K)  |
| F36.2K | 8  | 17 | 640x480         |
| F33K   | 9  | 16 | 640x400         |
| Vss    | 10 | 15 | 640x350         |
| PM1    | 11 | 14 | QH              |
| PM3    | 12 | 13 | QHRC            |

**WT8045N24P4**

|        |    |    |                          |
|--------|----|----|--------------------------|
| OSCin  | 1  | 24 | VDD                      |
| OSCout | 2  | 23 | 1024x768 (I)             |
| HSin   | 3  | 22 | 800x600(37.5K)           |
| VSin   | 4  | 21 | NC                       |
| Hout   | 5  | 20 | 800x600(35.2K)           |
| Vout   | 6  | 19 | 640x480(31.5K)           |
| F36.2K | 7  | 18 | 640x400(31.5K)           |
| F33K   | 8  | 17 | 640x480<br>(37.5K/72Hz)  |
| NC     | 9  | 16 | 640x350<br>(31.5K/37.5K) |
| NC     | 10 | 15 | NC                       |
| VSS    | 11 | 14 | PM3                      |
| PM1    | 12 | 13 | PM2                      |

**WT8045N24P5**

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 24 | VDD             |
| OSCout | 2  | 23 | 1024x768(56.5K) |
| HSin   | 3  | 22 | 1024x768 (NI)   |
| VSin   | 4  | 21 | 1024x768 (I)    |
| H_out  | 5  | 20 | 800x600(48K)    |
| V_out  | 6  | 19 | 800x600(37.5K)  |
| F43.5K | 7  | 18 | 800x600(35.2K)  |
| F36.2K | 8  | 17 | 640x480         |
| F33K   | 9  | 16 | 640x400         |
| QV1    | 10 | 15 | 640x350         |
| QVRC   | 11 | 14 | QH              |
| Vss    | 12 | 13 | QHRC            |

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# WT8045

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## WT8045N24P6

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 24 | VDD             |
| OSCout | 2  | 23 | 1024x768(56.5K) |
| HSin   | 3  | 22 | 1024x768 (NI)   |
| VSin   | 4  | 21 | 1024x768 (I)    |
| H_out  | 5  | 20 | 800x600(48K)    |
| V_out  | 6  | 19 | 800x600(37.5K)  |
| F43.5K | 7  | 18 | 800x600(35.2K)  |
| F36.2K | 8  | 17 | 640x480         |
| F33K   | 9  | 16 | 640x400         |
| Vss    | 10 | 15 | 640x350         |
| Mute   | 11 | 14 | QH              |
| PM3    | 12 | 13 | QHRC            |

## WT8045N24P7

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 24 | VDD             |
| OSCout | 2  | 23 | 1024x768(56.5K) |
| HSin   | 3  | 22 | 1024x768 (NI)   |
| VSin   | 4  | 21 | 1024x768 (I)    |
| H_out  | 5  | 20 | 800x600(48K)    |
| V_out  | 6  | 19 | 800x600(37.5K)  |
| F43.5K | 7  | 18 | 800x600(35.2K)  |
| F36.2K | 8  | 17 | 640x480         |
| F33K   | 9  | 16 | 640x400         |
| Vss    | 10 | 15 | 640x350         |
| P52K   | 11 | 14 | PM3             |
| PM1    | 12 | 13 | PM2             |

## WT8045N24P8

|         |    |    |                 |
|---------|----|----|-----------------|
| OSCin   | 1  | 24 | VDD             |
| OSCout  | 2  | 23 | 1024x768(56.5K) |
| HSin    | 3  | 22 | 1024x768 (NI)   |
| VSin    | 4  | 21 | 1024x768 (I)    |
| H_out   | 5  | 20 | 800x600(48K)    |
| V_out   | 6  | 19 | 800x600(37.5K)  |
| F43.5K  | 7  | 18 | 800x600(35.2K)  |
| F36.2K  | 8  | 17 | 640x480         |
| F33K    | 9  | 16 | 640x400         |
| Vss     | 10 | 15 | 640x350         |
| P52K    | 11 | 14 | PM3             |
| PM1+PM2 | 12 | 13 | Mute            |

## WT8045N32

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 32 | VDD             |
| OSCout | 2  | 31 | 1024x768(56.5K) |
| HSin   | 3  | 30 | 1024x768 (NI)   |
| VSin   | 4  | 29 | 1280x1024(64K)  |
| H_out  | 5  | 28 | 1024x768 (I)    |
| V_out  | 6  | 27 | 800x600(48K)    |
| F43.5K | 7  | 26 | 800x600(37.5K)  |
| F36.2K | 8  | 25 | 800x600(35.2K)  |
| F33K   | 9  | 24 | 640x480         |
| QV128  | 10 | 23 | 640x400         |
| QVRC   | 11 | 22 | 640x350         |
| Vss    | 12 | 21 | QH              |
| SELPIN | 13 | 20 | QHRC            |
| -QH    | 14 | 19 | PM3             |
| F52K   | 15 | 18 | PM2             |
| F60K   | 16 | 17 | PM1             |

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# WT8045

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## WT8045N28P1

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 28 | VDD             |
| OSCOut | 2  | 27 | 1024x768(56.5K) |
| HSin   | 3  | 26 | 1024x768 (NI)   |
| VSin   | 4  | 25 | 1024x768 (I)    |
| H_out  | 5  | 24 | 800x600(48K)    |
| V_out  | 6  | 23 | 800x600(37.5K)  |
| F43.5K | 7  | 22 | 800x600(35.2K)  |
| F36.2K | 8  | 21 | 640x480         |
| F33K   | 9  | 20 | 640x400         |
| QV128  | 10 | 19 | 640x350         |
| QVRC   | 11 | 18 | QH              |
| Vss    | 12 | 17 | QHRC            |
| F52K   | 13 | 16 | PM3             |
| PM1    | 14 | 15 | PM2             |

## WT8045N28P3

|        |    |    |                 |
|--------|----|----|-----------------|
| OSCin  | 1  | 28 | VDD             |
| OSCOut | 2  | 27 | 1024x768(56.5K) |
| HSin   | 3  | 26 | 1024x768 (NI)   |
| VSin   | 4  | 25 | 1024x768 (I)    |
| H_out  | 5  | 24 | 800x600(48K)    |
| V_out  | 6  | 23 | 800x600(37.5K)  |
| F43.5K | 7  | 22 | 800x600(35.2K)  |
| F36.2K | 8  | 21 | 640x480         |
| F33K   | 9  | 20 | 640x400         |
| QV1    | 10 | 19 | 640x350         |
| QVRC   | 11 | 18 | QH              |
| Vss    | 12 | 17 | QHRC            |
| F52K   | 13 | 16 | PM3             |
| PM1    | 14 | 15 | PM2             |

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## WT8045

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### WT8045N28P4

|             |    |    |                 |
|-------------|----|----|-----------------|
| OSCin       | 1  | 28 | VDD             |
| OSCout      | 2  | 27 | 1024x768(56.5K) |
| HSin        | 3  | 26 | 1024x768 (NI)   |
| VSin        | 4  | 25 | 1024x768 (I)    |
| H_out       | 5  | 24 | 800x600(48K)    |
| V_out       | 6  | 23 | 800x600(37.5K)  |
| F43.5K      | 7  | 22 | 800x600(35.2K)  |
| F36.2K      | 8  | 21 | 640x480         |
| F33K        | 9  | 20 | 640x400         |
| QV128       | 10 | 19 | 640x350         |
| QVRC        | 11 | 18 | QH              |
| Vss         | 12 | 17 | QHRC            |
| F52K        | 13 | 16 | PM3             |
| PM1<br>+PM2 | 14 | 15 | Mute            |

### WT8045N28P5

|             |    |    |                 |
|-------------|----|----|-----------------|
| OSCin       | 1  | 28 | VDD             |
| OSCout      | 2  | 27 | 1024x768(56.5K) |
| HSin        | 3  | 26 | 1024x768 (NI)   |
| VSin        | 4  | 25 | 1024x768 (I)    |
| H_out       | 5  | 24 | 800x600(48K)    |
| V_out       | 6  | 23 | 800x600(37.5K)  |
| F43.5K      | 7  | 22 | 800x600(35.2K)  |
| F36.2K      | 8  | 21 | 640x480         |
| F33K        | 9  | 20 | 640x400         |
| QV1         | 10 | 19 | 640x350         |
| QVRC        | 11 | 18 | QH              |
| Vss         | 12 | 17 | QHRC            |
| F52K        | 13 | 16 | PM3             |
| PM1<br>+PM2 | 14 | 15 | Mute            |

Note: The Hout and Vout pin of N28P1, N28P3, N28P4 and N28P5 are negative pulse.

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**ABSOLUTE MAXIMUM RATINGS**

| ITEM                           | SYMBOL    | VALUE           | UNIT     |
|--------------------------------|-----------|-----------------|----------|
| Digital Supply Voltage         | $V_{DD}$  | 5.5             | V        |
| Horizontal Sync. Input Voltage | $V_{HS}$  | $V_{DD(5)+0.3}$ | $V_{PP}$ |
| Vertical Sync. Input Voltage   | $V_{VS}$  | $V_{DD(5)+0.3}$ | $V_{PP}$ |
| Power Dissipation              | $P_D$     | 300             | mW       |
| Operating Temperature Range    | $T_{OPT}$ | 0 to 70         | °C       |
| Storage Temperature Range      | $T_{STG}$ | -40 to 125      | °C       |

**RECOMMENDED OPERATING CONDITIONS**

| ITEM                                   | SYMBOL      | MIN.   | TYP. | MAX.            | UNIT       |
|----------------------------------------|-------------|--------|------|-----------------|------------|
| Digital Supply Voltage                 | $V_{DD(5)}$ | 4.5    | 5    | 5.5             | V          |
| Supply Current (Standby)               | $I_P$       |        |      | 13              | mA         |
| Synchronous Input Voltage Low          | $V_{IL}$    |        |      | 0.8             | $V_{PP}$   |
| Synchronous Input Voltage High         | $V_{IH}$    | 2.4    | 4    | 5.5             | $V_{PP}$   |
| Horizontal Synchronous Frequency Range | $F_H$       | 25     | 30   | 80<br>(for N32) | KHz        |
| Vertical Synchronous Frequency Range   | $F_V$       | 50     | 60   | 120             | Hz         |
| Crystal Clock Frequency                | $F_{CLK}$   | 3.5764 | 3.58 | 3.5836          | MHz        |
| Open Drain Pull High Voltage           | $V_{OH}$    |        |      | 12              | V          |
| Resistance of Monostable for Hsin      | $R_H$       | 10     |      | 100             | k $\Omega$ |
| Capacitance of Monostable for Hsin     | $C_H$       | 10     | 100  | 10              | pF         |
| Resistance of Monostable for Vsin      | $R_V$       | 10     |      | 500             | k $\Omega$ |
| Capacitance of Monostable for Vsin     | $C_V$       | 10     | 100  | 10              | pF         |



## ***ELECTRICAL CHARACTERISTICS***

( $V_{DD}=5V$ ,  $T_{OPT}=25^{\circ}C$ , Crystal=3.58MHz)

| ITEM                                                         | SYMBOL    | MIN. | TYP. | MAX. | UNIT     |
|--------------------------------------------------------------|-----------|------|------|------|----------|
| Discrimination of H.<br>Synchronous Frequency                | F33K      | 32.9 | i Ø  | 33.1 | KHz      |
|                                                              | F36.2K    | 36.1 | i Ø  | 36.3 | KHz      |
|                                                              | F43.5K    | 43.4 |      | 43.6 | KHz      |
|                                                              | F52K      | 51.9 | i Ø  | 52.1 | KHz      |
|                                                              | F60K      | 59.9 | i Ø  | 60.1 | KHz      |
| Output Low (H-out, V-out),<br>when $I_{OL} = 4mA$            | $V_{OL1}$ |      |      | 0.4  | $V_{PP}$ |
| Output High (H-out, V-out),<br>when $I_{OH} = -400\mu A$     | $V_{OH1}$ | 2.4  |      |      | $V_{PP}$ |
| Open Drain Output Low<br>when $I_{OL} = 6mA$                 | $V_{OL2}$ |      |      | 0.4  | $V_{PP}$ |
| Output Sink Current (H-out, V-out)<br>when $V_{OL1} = 0.4V$  | $I_{OL1}$ |      |      | 4    | mA       |
| Output Drive Current (H-out, V-out)<br>when $V_{OH1} = 2.4V$ | $I_{OH1}$ |      |      | 400  | $\mu A$  |
| Open Drain Sink Current<br>when $V_{OL2} = 0.4V$             | $I_{OL2}$ |      | 10   |      | mA       |
| Open Drain Sink Current<br>when $V_{OL2} = 5V$               | $I_{OL2}$ |      | 40   |      | mA       |



***MONO\_STABLE DYNAMIC ELECTRICAL CHARACTERISTICS***

(Ta=25°C; Input  $t_r, t_f=20\text{ns}$ ,  $C_L=50\text{PF}$ )

| ITEM                                                                            | MIN.   | TYP. | MAX.  | UNITS |
|---------------------------------------------------------------------------------|--------|------|-------|-------|
| Input H_SYNC Pulse Width                                                        | 0.558  | i Ø  | 4     | £ g   |
| Input V_SYNC Pulse Width                                                        | 0.0384 | i Ø  | 0.125 | ms    |
| Output Pulse Transition Time                                                    | i Ø    | 100  | 200   | ns    |
| Output Pulse Propagation Delay                                                  | i Ø    | 300  | 600   | ns    |
| Output Pulse Width Adjust Range                                                 | 10     | i Ø  | 90    | ¢ M   |
| H_MONO_STB:                                                                     |        |      |       |       |
| 31KHz i Ø7.5KHz                                                                 |        |      | 26.66 | £ g   |
| 31KHz i Ø8KHz                                                                   |        |      | 20.83 | £ g   |
| 31KHz i Ø7KHz                                                                   |        |      | 17.54 | £ g   |
| 31KHz i Ø4KHz                                                                   |        |      | 15.62 | £ g   |
| V_MONO_STB:                                                                     |        |      |       |       |
| (50Hz i Ø20Hz)*128                                                              |        |      | 65.10 | £ g   |
| 6.4KHz i Ø5.36KHz                                                               |        |      |       |       |
| (50Hz i Ø0Hz)*128                                                               |        |      | 97.66 | £ g   |
| 6.4KHz i Ø0.2KHz                                                                |        |      |       |       |
| (50Hz i Ø20Hz)*1                                                                |        | 10   |       | ms    |
| Typical Pulse width Variation as a function of Temperature at 75¢ Jto 24 ¢ J    | i Ø    | i Ø  | i Ø   | ¢ M   |
| Typical Pulse Width Variation as a function of Supply Voltage at 4.75V to 5.25V | i Ø    | i Ø  | i Ø   | ¢ M   |
| Output Low (Sink) Current                                                       | 1      | i Ø  | 6     | mA    |
| Output Voltage Low-Level                                                        | i Ø    | 0    | 0.05  | V     |
| Output Voltage High-Level                                                       | 4.95   |      | i Ø   | V     |
| Output Jitter (Hout & Vout)                                                     |        |      | 5     | ns    |
| Hin & Vin Rise time and Fall time = 200ns                                       |        |      |       |       |



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**APPLICATION INFORMATION**

| Name    | Function                                                                                                                                                 | Struncure of Terminal   |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|
| OSCin   | A clock generating circuit is built into the chip. So if a resonator is connected to OSCin/OS Cout, a clock signal can be obtained                       | I                       |
| OS Cout | Refer to OSCin pin                                                                                                                                       | O                       |
| Hsin    | Input terminal of horizontal synchronous signal                                                                                                          | I, TTL compatible       |
| Vsin    | Input terminal of vertical synchronous signal                                                                                                            | I, TTL compatible       |
| H_OUT   | Output pin, fixed negative polarity of original H_SYNC signal with same pulse width (but, positive for N28P2, N28P6,N28P7 and N28P8)                     | I, TTL compatible       |
| V_OUT   | Output pin, fixed negative polarity of original V_SYNC signal with same pulse width (but, positive for N28P2, N28P6,N28P7 and N28P8)                     | O, TTL compatible       |
| F43.5k  | >43.5k then active low, <43.5k then high                                                                                                                 | O, open drain           |
| F36.2k  | >36.2k then active low, <36.2k then high                                                                                                                 | O, open drain           |
| F33k    | >33k then active low, <33k then high                                                                                                                     | O, open drain           |
| QV      | Output pin, fixed positive polarity of vertical signal; pulse width depend upon RV & CV.                                                                 | O, open drain           |
| QVRC    | Input pin, connected to Vdd through RV & to ground through CV                                                                                            | I                       |
| Vss     | Ground                                                                                                                                                   |                         |
| SELPIN  | Input pin, to select which one of H_SYNC or V_SYNC appears on the output pin of QV; N.C. selects the V-SYNC on the output, grounding selects the H_SYNC. | I, (N.C.-no connection) |
| -QH     | Output pin, fixed negative polarity of horizontal signal; pulse width depend upon RH & CH.                                                               | O, open drain           |
| F52k    | >52k then active low, <52k then high                                                                                                                     | O, open drain           |
| F60k    | >60k then active low, < 60k then high                                                                                                                    | O, open drain           |
| PM1     | Indicate in STAND-BY mode                                                                                                                                | O, open drain           |

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| Name           | Function                                                                                                                   | Struncure of Terminal |
|----------------|----------------------------------------------------------------------------------------------------------------------------|-----------------------|
| PM2            | Indicate in SUSPEND mode                                                                                                   | O, open drain         |
| PM3            | Indicate in OFF mode                                                                                                       | O, open drain         |
| QHRC           | Input pin, connected to Vdd through RH & to ground through CH.                                                             | I                     |
| QH             | Output pin, fixed positive polarity of horizontal signal; pulse width depend upon RH & CH                                  | O, open drain         |
| 640i 550       | Mode select control output, if IBM VGA 640i 550 mode, or VESA VGA 640i 550 mode. Then active "low", else open state output | O, open drain         |
| 640i 680       | VESA VGA mode 640i 680 (37.5k/72Hz)                                                                                        | O, open drain         |
| 640i 800       | If IBM VGA 640i 800 mode, or VESA VGA 640i 800 mode then active "low" (640i 800, 31.5k, for N24P4)                         | O, open drain         |
| 640i 880       | If IBM VGA 640i 880 mode, or VESA VGA 640i 880 mode then active "low" (640i 880, 31.5k, for N24P4)                         | O, open drain         |
| 800i 600       | VESA super VGA mode<br>(H_SYNC = 35.2k, V_SYNC = 56Hz)                                                                     | O, open drain         |
| 800i 600       | European super VGA mode<br>(H_SYNC = 37.5k, V_SYNC = 60Hz)                                                                 | O, open drain         |
| 800i 600       | VESA new super VGA mode<br>(H_SYNC = 48k, V_SYNC = 72Hz)                                                                   | O, open drain         |
| 1024i 768(I)   | IBM 8512/A interlace mode<br>(H_SYNC = 35.5k, V_SYNC = 86Hz)                                                               | O, open drain         |
| 1280i 1024     | 1280i 1024 mode control output<br>(H_SYNC = 64k, V_SYNC = 60Hz)                                                            | O, open drain         |
| 1024i 768(NI)  | IBM 8514/A non-interlace mode<br>(H_SYNC = 48.5k, V_SYNC = 60Hz)                                                           | O, open drain         |
| 1024i 768(57k) | XGA 1024i 768 mode Hsync freq. 57kHz<br>(H_SYNC = 56.5k, V_SYNC = 72Hz)                                                    | O, open drain         |
| Vdd            | 5 Volts power supply                                                                                                       |                       |

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**APPLICATION DESCRIPTION****DPMS (Display Power Management Signaling) Detection**

As per DPMS proposal version 1.0P, revision 0.54P, WT8045 provides Monitor Power Management Detection Circuit for the convenience of monitor designers in designing power saving monitors, or the so called "Green Monitors". Please refer to the table 1 as below for power states defined in the DPMS.

DPMS requires at least 5 seconds delay before transition from ON state to any power saving state, to avoid unintentionally entering a power saving state during display resolution changes and timing mode changes. And it can be done instantaneously, for the transition between any power saving state.

Table 1 Display Power Management Summary

| State    | Signals    |           |         | DPMS Compliance Requirement | Power Savings | Recovery Time    |
|----------|------------|-----------|---------|-----------------------------|---------------|------------------|
|          | Horizontal | Vertical  | Video   |                             |               |                  |
| On       | Pulses     | Pulses    | Active  | Mandatory                   | None          | Not Applicable   |
| Stand-by | No Pulses  | Pulses    | Blanked | Optional                    | Minimal       | Short            |
| Suspend  | Pulses     | No Pulses | Blanked | Mandatory                   | Substantial   | Longer           |
| Off      | No Pulses  | No Pulses | Blanked | Mandatory                   | Maximum       | System Dependent |

\* "No-Pulse" represents the frequency of Hsin or Vsin less than or equal to 10Hz, but "Pulses" represents that frequency of Hsin greater than or equal to 10KHz and Vsin greater than or equal to 40Hz

**The way WT8045 implements VESA DPMS**

As shown on Table 2, WT8045 use PM1 to represent Stand-by State, PM2 as Suspend State and PM3 as OFF State. When H\_SYNC / V\_SYNC signals transition from ON State to any one of the three power saving states, WT8045 will delay 5.9 seconds to meet the VESA DPMS requirement: the minimum 5 seconds delay to avoid unintentionally entering a power saving state during display resolution and timing mode changes. If during this delay time period, H\_SYNC and V\_SYNC signals return to ON State, then all three power management pins (PM1, PM2 and PM3) will remain ON state. If power management state of H\_SYNC and V\_SYNC prolong for more than 5.9 seconds, then these three power management pins will change to the corresponding states. While changing from any power saving state back to ON State will take about 0.368 second for H\_SYNC / VSYNC pulse checking. And transition between any power saving state will be done immediately.

Table 2: The truth table of Power Saving Detector

| MODE     | Hsin            | Vsin      | PM1 | PM2 | PM3 |
|----------|-----------------|-----------|-----|-----|-----|
| ON       | Pulses          | Pulses    | 1   | 1   | 1   |
| STAND_BY | No Pulses       | Pulses    | 0   | 1   | 1   |
| SUSPEND  | Pulses          | No Pulses | 0   | 0   | 1   |
| OFF      | No Pulses       | No Pulses | 0   | 0   | 0   |
| OVERRIDE | No Pulses       | No Pulses | 1   | 1   | 1   |
|          | Manually PWR ON |           |     |     |     |

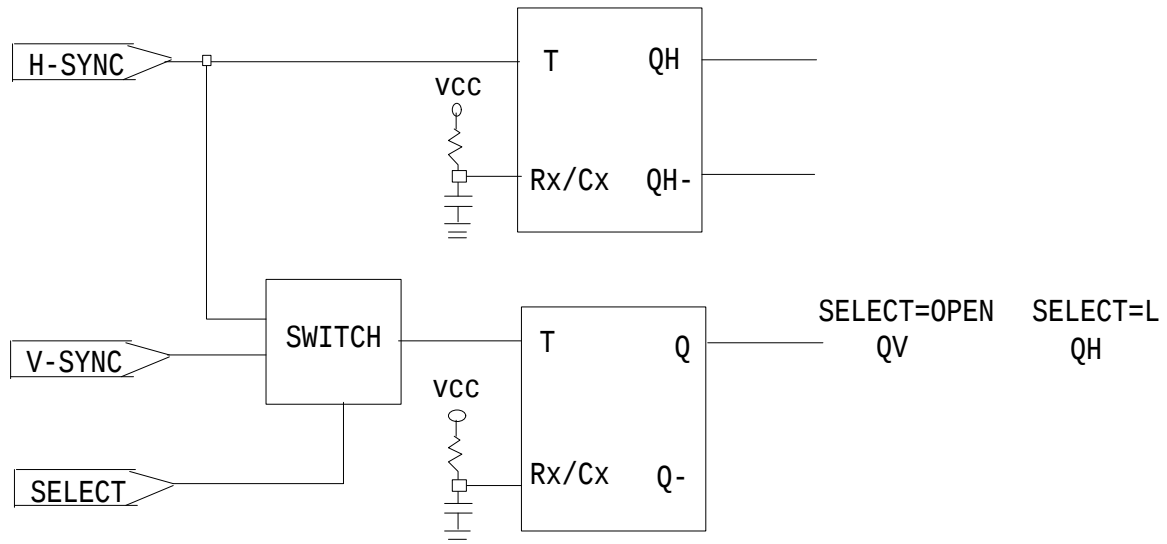
**OVERRIDE mode:**

To initial override, both horizontal and vertical sync signals shall be in the no pulses condition when the display is maintained during the entire time override is required. As soon as pulses are detected on horizontal and vertical sync signal. The display shall enter DPMS operation.

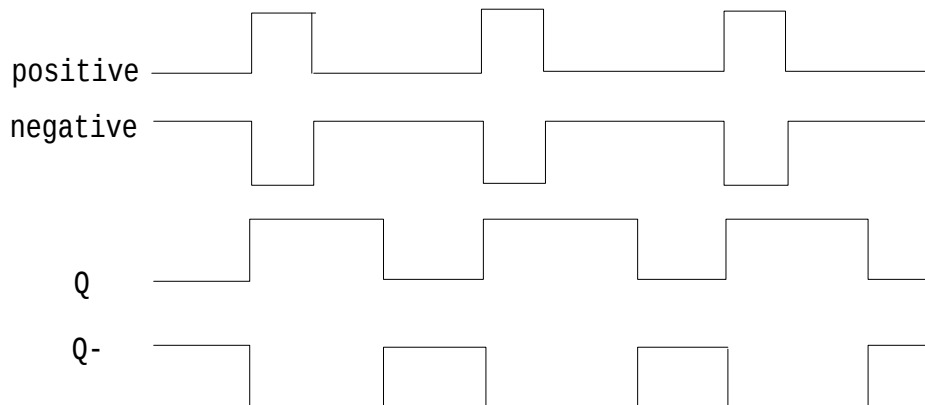
Three power management pins are open drain structure and active low. If you do not need all those three power saving states in your design. You can just short two or three pins of the pins PM1/PM2/PM3. for example, by shorting pin PM1 and pin PM2, you will have only two power saving states, that is OFF and Suspend states, so you have three states total, including ON State. Please refer to Application Circuit 2.

**Mono\_Stable Circuit**

WT8045 includes two sets of Mono\_Stable Circuits, one uses H\_SYNC as trigger signal, the other uses either H\_SYNC or V\_SYNC as trigger signal (this only can be done on 32 pin package, for 24 pin and 28 pin packages the trigger signal is fixed to H\_SYNC); for N24p4 package, there is no mono-stable circuit. Please refer to the figure as below:



The Mono\_Stable Circuit is triggered by positive edge, no matter H\_SYNC or V\_SYNC is used as trigger signal. Please refer to the timing chart as below:

**Trigger Pulse**


The output of Mono\_Stable Circuit is open drain structure, and can be pulled up to +12V maximum.



In case of using output pulse of V\_MONO\_STABLE as voltage source, in order to prevent the problem of slow response time, causing from the low frequency on vertical synchronous signal, WT8045 internally increases the vertical signal frequency to 128 times the original frequency, that is from 50Hz - 120 Hz to 6.4KHz - 15.36KHz. Then WT8045 uses this increased frequency as the input signal of MONO\_STABLE, so the leading edge of the signal of the increased frequency will trigger the MONO\_STABLE circuit.

An external resistor (Rx) and an external capacitor (Cx) control the timing and accuracy of the circuit. Adjustment of Rx and Cx provides a wide range of output pulse widths from the Q and Q-bar terminals. The delay time from trigger input to output transition is independent of Rx and Cx.

The minimum value of external resistor Rx is 10k ohms. The typical value of external capacitor Cx is 100 pF. The time period (T) for this multi-vibrator can be calculated with the formula:  $T \approx 1.1 R_x \bullet C_x$ .

### **H/V Frequency Divisions and Video Modes**

Figure 1 illustrates the typical frequency ranges of H and V sync signals for display monitors. The operating video modes are determined by the H and V frequencies, and occasionally, by their polarities. The typical video modes of display monitors include the IBM VGA, VESA VGA, European VGA/super VGA, VESA super VGA, IBM 8514/A, XGA, and 1280x 1024.

WT8045 can determine 13 standard video modes for 32 pin package (refer to Table 3) according to H and V frequencies and polarities. These standard video modes include the IBM VGA, VESA VGA, VESA super VGA and IBM 8514/A. This provides the users with the capability to adjust the screen size for different modes.

WT8045 pre-sets the discriminating points both on H and V frequencies. The discriminating points for H sync are 33KHz, 36.2KHz, 43.5KHz, 52KHz and 60KHz (for 32 pin). These discriminating points will be able to identify various video modes as shown in Fig. 1. WT8045 also provides the flexibility for users to define these discriminating points through mask option.



The tolerance for H sync frequency discrimination is  $\pm 0.1\text{KHz}$ . For instance, the 33KHz discriminating point will be able to distinguish the H sync frequency that is either "less than or equal to" 32.9KHz, or "greater than or equal to" 33.1KHz. There is an ambiguous region between 32.9KHz and 33.1KHz.

WT8045 has two discriminating points, 64Hz and 78Hz, for the V sync signal as shown in Fig.1. The tolerance is  $\pm 0.4\text{Hz}$ . The discrimination results of V sync frequency are used internally for mode selection.

Base on the package consideration, IBM VGA mode and VESA VGA mode (both have same resolution: 640x480, 640x400, 640x350) are decoded on same open Drain structure output pins. In case of these whole six modes decoding is needed, the horizontal frequency discrimination pin F33k or F36.2k must take into consideration. The horizontal frequency of IBM VGA mode is 31.5kHz, and VESA IBM VGA mode is 37.5kHz. Using F33k or F36.2k pin can clearly identify these two standard modes. The decoding circuit is attached on application section for reference.

| Graphic Standard          | Resolution | Horizontal | Vertical | Polarities |
|---------------------------|------------|------------|----------|------------|
| IBM VGA                   | 640X350    | 31.5kHz    | 70Hz     | +, -       |
|                           | 640X400    | 31.5kHz    | 70Hz     | -, +       |
|                           | 640X480    | 31.5kHz    | 60Hz     | -, -       |
| VESA Super VGA            | 800X600    | 35.2kHz    | 56Hz     |            |
| IBM 8512/A Interlaced     | 1024X768   | 35.5kHz    | 86Hz     |            |
| VESA VGA                  | 640X350    | 37.5kHz    | 83Hz     | +, -       |
|                           | 640X400    | 37.5kHz    | 83Hz     | -, +       |
|                           | 640X480    | 37.5kHz    | 72Hz     | -, -       |
| European Super VGA        | 800X600    | 37.5kHz    | 60Hz     |            |
| VESA New Super VGA        | 800X600    | 48.0kHz    | 72Hz     |            |
| IBM 8514/A Non-Interlaced | 1024X768   | 48.5kHz    | 60Hz     |            |
| VESA New 1024X768         | 1024X768   | 56.5kHz    | 72Hz     |            |
| Work Station 1280X1024    | 1280X1024  | 64.0kHz    | 60Hz     |            |

Table 3: Graphic Standard and Frequencies

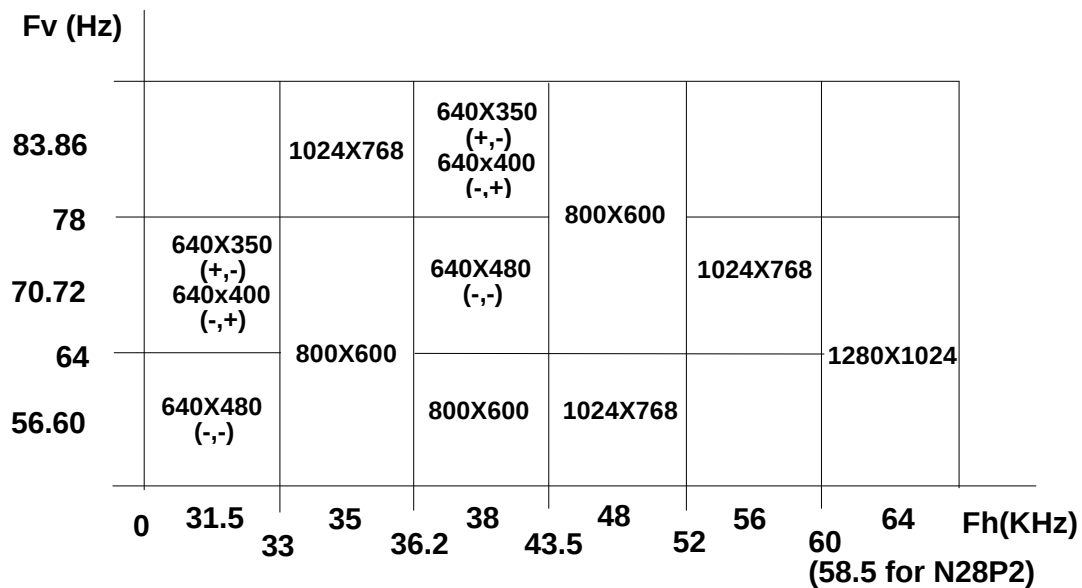


Figure 1: H/V Frequency Division and Video Mode

| PIN  |         | 640X480 | 640X400 | 640X350 |
|------|---------|---------|---------|---------|
| Mode | IBM     |         |         |         |
|      | 640X480 | 0       | 1       | 1       |
| VGA  | 640X400 | 1       | 0       | 1       |
|      | 640X350 | 1       | 1       | 0       |
| VESA | 640X480 | 0       | 1       | 1       |
|      | 640X400 | 1       | 0       | 1       |
| VGA  | 640X350 | 1       | 1       | 0       |

Table 4: IBM VGA/ VESA VGA Decoding Table

**Horizontal Frequency Discriminator**

There are horizontal frequency discriminator pins on different type package: 33k, 36.2k (for N24P4 package); 33k, 36.2k, 43.5k (for 24 pin); 33k, 36.2k, 43.5k, 52k (for 28 pin); 33k, 36.2k, 43.5k, 52k, 60k (for 32 pin); please refer to table 5 for the logical truth table of these pins. These frequency discriminator pins output can be used for  $C_S$  Capacitor Control directly as well as other application.

| Signal<br>Hsync | F33k | F36k | F43.5k | F52k | F60k |
|-----------------|------|------|--------|------|------|
| Hs<33k          | 1    | 1    | 1      | 1    | 1    |
| 36k>Hs>33k      | 0    | 1    | 1      | 1    | 1    |
| 43.5k>Hs>36k    | 0    | 0    | 1      | 1    | 1    |
| 52k>Hs>43.5k    | 0    | 0    | 0      | 1    | 1    |
| 60k>Hs>52k      | 0    | 0    | 0      | 0    | 1    |

Table 5: Truth table of Frequency discriminator

**Mute function Timing Diagram****Weltrend Semiconductor, Inc.**

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**WT8045**

Synchronous Signal Discriminator and  
Power Saving Detector for Green Monitor

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***APPLICATION CIRCUIT I***

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***APPLICATION CIRCUITII***

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***APPLICATION CIRCUIT III***

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***APPLICATION CIRCUIT IV***

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***DIP OUTLINE DIMENSIONS***

|               | A    | B   | C   | D   | E   | F   | G   |
|---------------|------|-----|-----|-----|-----|-----|-----|
| N24           | 1250 | 542 | 152 | 100 | 130 | 650 | 600 |
| N28<br>SKINNY | 1385 | 288 | 130 | 100 | 130 | 355 | 310 |
| N32           | 1650 | 542 | 154 | 100 | 130 | 650 | 600 |

┆ Dimension in mil

┆ 1mm = 39.37 mil

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## WT8045

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### WT8045N28P2

|        |    |    |                          |
|--------|----|----|--------------------------|
| OSCin  | 1  | 28 | VDD                      |
| OSCout | 2  | 27 | 1024x768(56.5K)          |
| HSin   | 3  | 26 | 1024x768 (NI)            |
| VSin   | 4  | 25 | 1024x768 (I)             |
| H_out  | 5  | 24 | 800x600(48K)             |
| V_out  | 6  | 23 | 800x600(37.5K)           |
| F43.5K | 7  | 22 | 800x600(35.2K)           |
| F36.2K | 8  | 21 | 640x480(31.5K)           |
| F33K   | 9  | 20 | 640x400<br>(31.5K/37.5K) |
| QV128  | 10 | 19 | 640x480(37.5K)           |
| QVRC   | 11 | 18 | QH                       |
| Vss    | 12 | 17 | QHRC                     |
| F52K   | 13 | 16 | PM3                      |
| PM1    | 14 | 15 | PM2                      |

### WT8045N28P6

|        |    |    |                          |
|--------|----|----|--------------------------|
| OSCin  | 1  | 28 | VDD                      |
| OSCout | 2  | 27 | 1024x768(56.5K)          |
| HSin   | 3  | 26 | 1024x768 (NI)            |
| VSin   | 4  | 25 | 1024x768 (I)             |
| H_out  | 5  | 24 | 800x600(48K)             |
| V_out  | 6  | 23 | 800x600(37.5K)           |
| F43.5K | 7  | 22 | 800x600(35.2K)           |
| F36.2K | 8  | 21 | 640x480(31.5K)           |
| F33K   | 9  | 20 | 640x400<br>(31.5K/37.5K) |
| QV1    | 10 | 19 | 640x480(37.5K)           |
| QVRC   | 11 | 18 | QH                       |
| Vss    | 12 | 17 | QHRC                     |
| F52K   | 13 | 16 | PM3                      |
| PM1    | 14 | 15 | PM2                      |

### WT8045N28P7

|        |    |    |                          |
|--------|----|----|--------------------------|
| OSCin  | 1  | 28 | VDD                      |
| OSCout | 2  | 27 | 1024x768(56.5K)          |
| HSin   | 3  | 26 | 1024x768 (NI)            |
| VSin   | 4  | 25 | 1024x768 (I)             |
| H_out  | 5  | 24 | 800x600(48K)             |
| V_out  | 6  | 23 | 800x600(37.5K)           |
| F43.5K | 7  | 22 | 800x600(35.2K)           |
| F36.2K | 8  | 21 | 640x480(31.5K)           |
| F33K   | 9  | 20 | 640x400<br>(31.5K/37.5K) |
| QV128  | 10 | 19 | 640x480(37.5K)           |
| QVRC   | 11 | 18 | QH                       |
| Vss    | 12 | 17 | QHRC                     |
| F52K   | 13 | 16 | PM3                      |
| PM1    | 14 | 15 | Mute                     |

### WT8045N28P8

|             |    |    |                          |
|-------------|----|----|--------------------------|
| OSCin       | 1  | 28 | VDD                      |
| OSCout      | 2  | 27 | 1024x768(56.5K)          |
| HSin        | 3  | 26 | 1024x768 (NI)            |
| VSin        | 4  | 25 | 1024x768 (I)             |
| H_out       | 5  | 24 | 800x600(48K)             |
| V_out       | 6  | 23 | 800x600(37.5K)           |
| F43.5K      | 7  | 22 | 800x600(35.2K)           |
| F36.2K      | 8  | 21 | 640x480(31.5K)           |
| F33K        | 9  | 20 | 640x400<br>(31.5K/37.5K) |
| QV1         | 10 | 19 | 640x480(37.5K)           |
| QVRC        | 11 | 18 | QH                       |
| Vss         | 12 | 17 | QHRC                     |
| F52K        | 13 | 16 | PM3                      |
| PM1<br>+PM2 | 14 | 15 | Mute                     |

Note: The Hout and Vout pin of N28P2, N28P6, N28P7 and N28P8 are positive pulse.

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