

Surface Mount Dual N-Channel Enhancement Mode MOSFET

(Pb) Lead(Pb)-Free

Features:

*Super high dense cell design for low $R_{DS(ON)}$

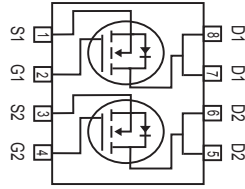
$$R_{DS(ON)} < 14m\Omega @ V_{GS} = 10V$$

$$R_{DS(ON)} < 20m\Omega @ V_{GS} = 4.5V$$

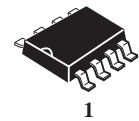
*Simple Drive Requirement

*Dual N MOSFET Package

*SO-8 Package



DRAIN CURRENT
10 AMPERES
DRAIN SOURCE VOLTAGE
30 VOLTAGE



1

SO-8

Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ⁽¹⁾ ($T_A = 25^\circ C$) ($T_A = 70^\circ C$)	I_D	10	A
		8	A
Pulsed Drain Current ⁽²⁾	I_{DM}	30	A
Power Dissipation ⁽¹⁾ ($T_A = 25^\circ C$)	P_D	2	W
Maximax Junction-to-Ambient ⁽¹⁾	$R_{\theta JA}$	62.5	$^\circ C/W$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

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Device Marking

WTK4224=4224SS

Electrical Characteristics(T_j = 25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	30	-	-	V	V _{GS} =0, I _D =250μA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _j	-	0.03	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250μA
Forward Transconductance	g _{fs}	-	16	-	S	V _{DS} =10V, I _D =10A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	μA	V _{DS} =30V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	25	μA	V _{DS} =24V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	14	mΩ	V _{GS} =10V, I _D =10A
		-	-	20		V _{GS} =4.5V, I _D =7A
Total Gate Charge ²	Q _g	-	23	15	nC	I _D =10A V _{DS} =24V V _{GS} =4.5V
Gate-Source Charge	Q _{gs}	-	6	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	14	-		
Turn-on Delay Time ²	T _{d(on)}	-	12	-	ns	V _{DS} =15V I _D =1A V _{GS} =10V R _G =3.3Ω R _D =15Ω
Rise Time	T _r	-	8	-		
Turn-off Delay Time	T _{d(off)}	-	34	-		
Fall Time	T _f	-	16	-		
Input Capacitance	C _{iss}	-	1910	3070	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	400	-		
Reverse Transfer Capacitance	C _{rss}	-	280	-		
Gate Resistance	R _g	-	0.9	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =1.7A, V _{GS} =0V, T _j =25°C
Reverse Recovery Time ²	T _{rr}	-	30	-	ns	I _S =10A, V _{GS} =0V di/dt=100A/μs
Reverse Recovery Charge	Q _{rr}	-	24	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300μs, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

Characteristics Curve

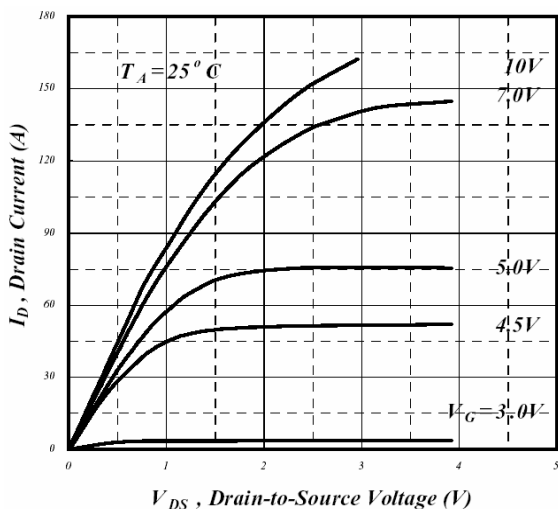


Fig 1. Typical Output Characteristics

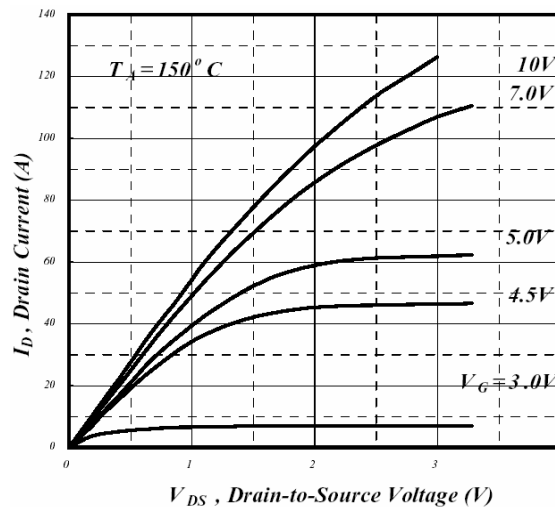


Fig 2. Typical Output Characteristics

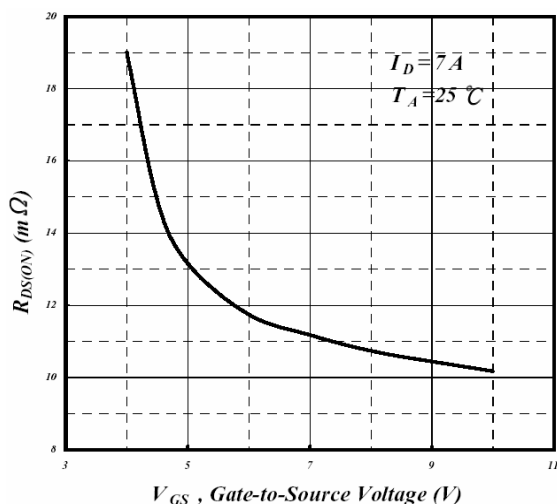


Fig 3. On-Resistance v.s. Gate Voltage

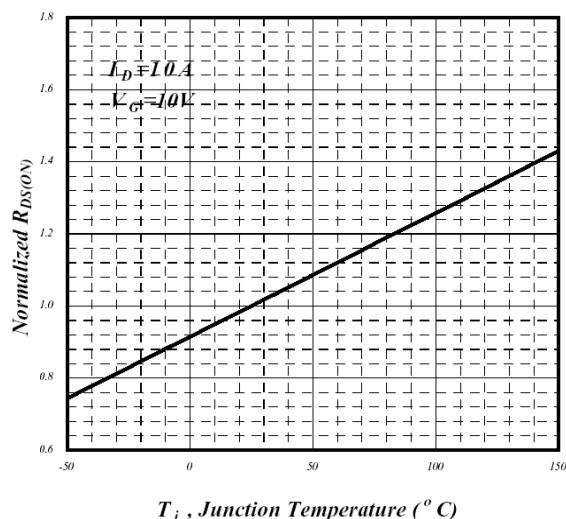


Fig 4. Normalized On-Resistance v.s. Junction Temperature

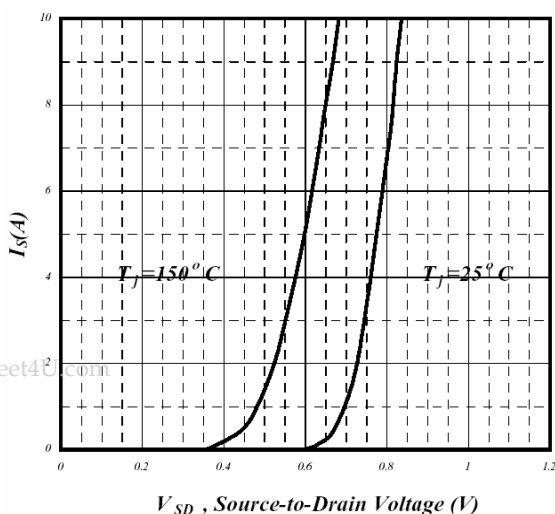


Fig 5. Forward Characteristics of Reverse Diode

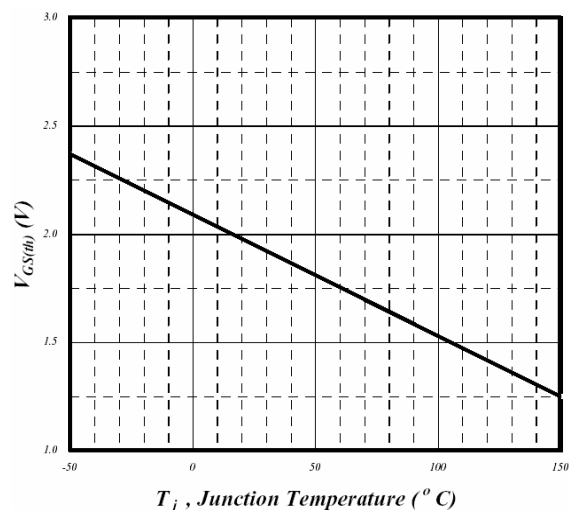


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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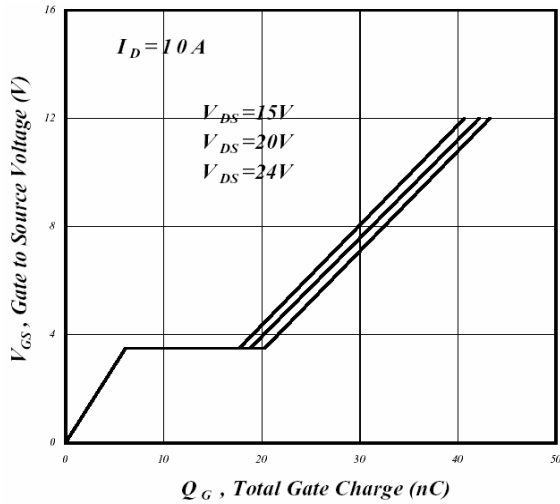


Fig 7. Gate Charge Characteristics

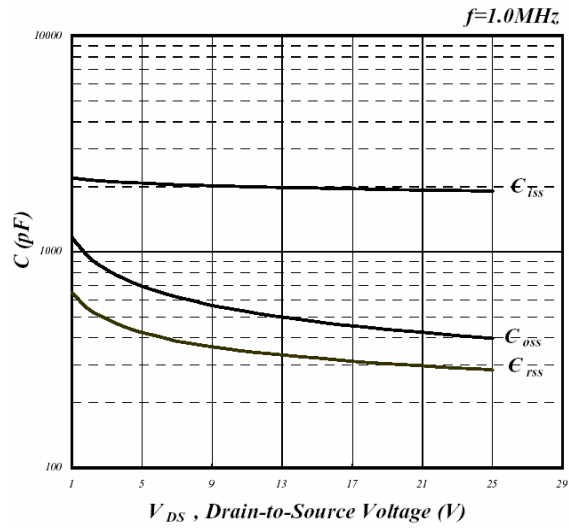


Fig 8. Typical Capacitance Characteristics

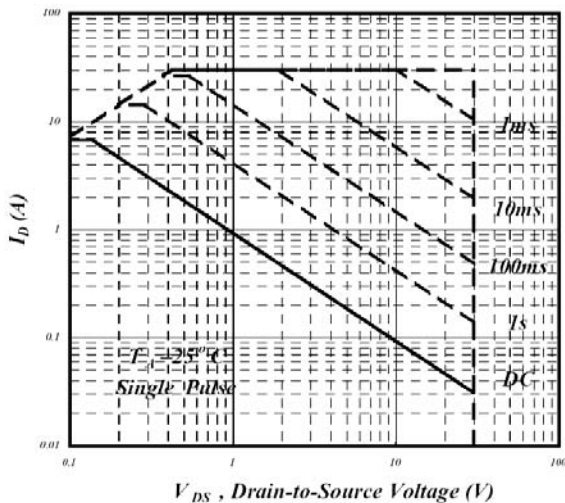


Fig 9. Maximum Safe Operating Area

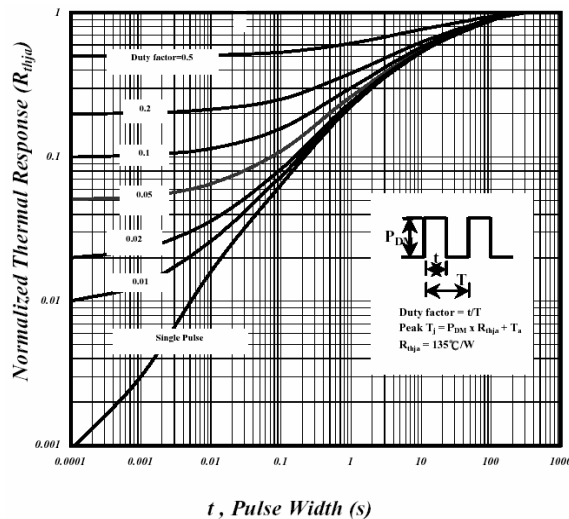


Fig 10. Effective Transient Thermal Impedance

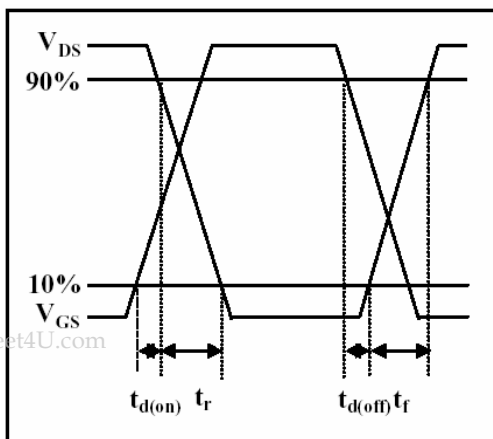


Fig 11. Switching Time Waveform

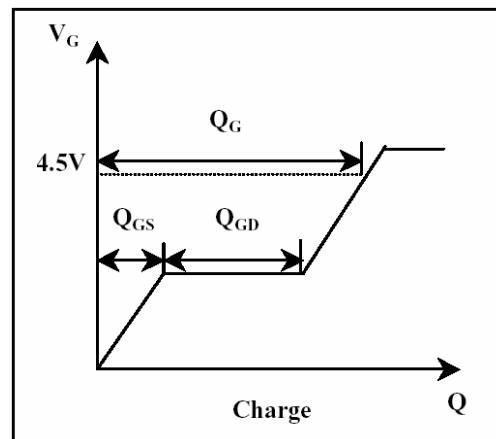
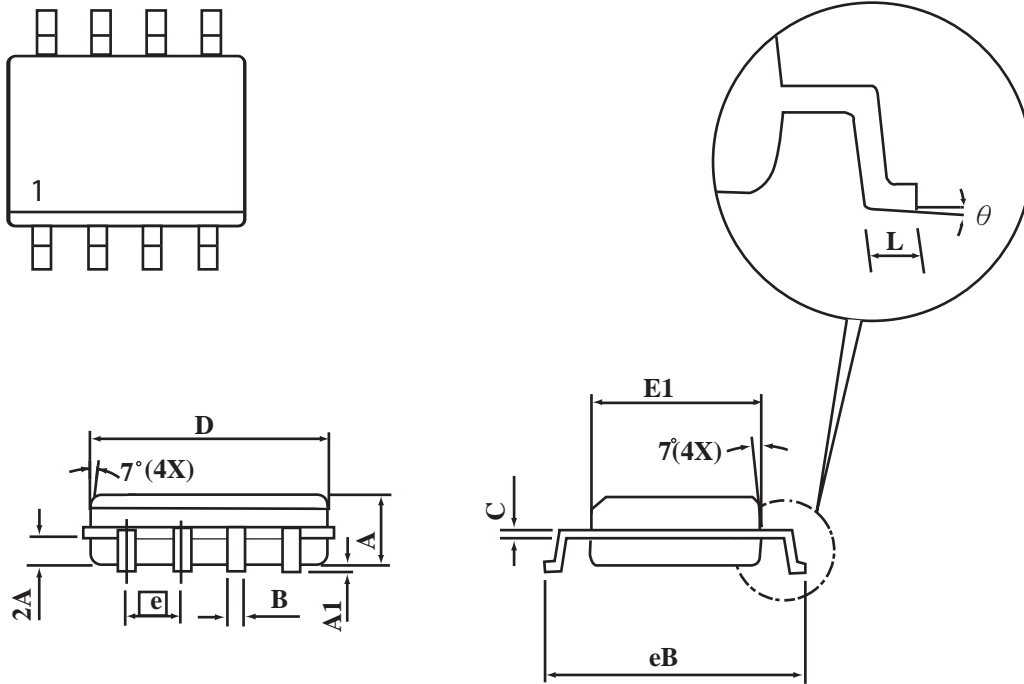


Fig 12. Gate Charge Waveform

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SO-8 Package Outline Dimensions

Unit:mm



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.20
B	0.35	0.45
C	0.18	0.23
D	4.69	4.98
E1	3.56	4.06
eB	5.70	6.30
e	1.27 BSC	
L	0.60	0.80
θ	0°	8°