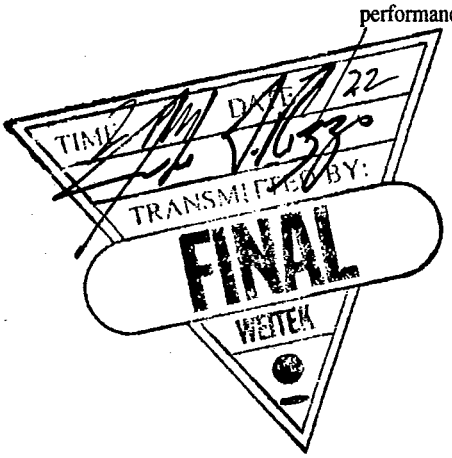
WEITEK

WTL 1232/WTL 1233 FLOATING POINT MULTIPLIER AND ALU

July, 1986

The WTL 1232 floating point multiplier and the WTL 1233 floating point ALU provide high speed, low power 32-bit numeric processing. In the highest speed grades, each chip delivers 10 MFLOP single precision performance.



Contents

WTL 1232/1233 32-BIT FLOATING POINT MULTIPLIER AND ALU

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Features

COMPLETE FLOATING POINT ARITHMETIC SOLUTION FOR HIGH SPEED PROCESSING

FULL 32-BIT CONFORMANCE TO IEEE STANDARD 754, VERSIONS 8.0 AND 10.0

FULL FUNCTION

Add
Subtract
Multiply
Conversion to and from 24-bit fixed point and 32-bit floating point
Absolute value

HIGH SPEED

10 MFlops (WTL 1232/1233-10) in three-stage pipeline mode

FAST CYCLE TIMES

Two 16-bit data input and one data output operation every cycle

FLOWTHROUGH MODE

Full 32-bit delay time of nine cycles for ALU and multiplier scalar operations

PIPELINE MODE

Full 32-bit throughput every two cycles for ALU and multiplier vector operations
Five operations can be in progress at one time
Full 32-bit delay time of 10 cycles

LOW POWER

0.6 watts maximum, WTL 1232; 2.0 watts maximum, WTL 1233-5

FLEXIBLE CONTROL INTERFACE

Single edge-triggered clock
Function control included in pipeline; no cycles wasted changing functions
Fully registered inputs and output with separate load and unload controls
Tri-state TTL outputs with high drive capability

STANDARD 64-PIN DIP AND 68-PIN LEADLESS CHIP CARRIER OR PIN GRID ARRAY PACKAGES AVAILABLE

Description

The low power WTL 1232 multiplier and WTL 1233 arithmetic logic unit (ALU) provide the essential 32–bit data path elements for high speed implementation of IEEE Standard 754 for single precision floating point arithmetic.

MOS VLSI design allows all functional elements to be combined in two low power chips with fast cycle times. While the WTL 1232 is a CMOS part, the WTL 1233 is a NMOS device. Flexible I/O lines and control signals allow the WTL 1232/1233 chip set to be used with a broad range of bus systems in a wide variety of applications.

The WTL 1232/1233 chip set conforms to the requirements of the IEEE standard for single precision operations and exception handling, including rounding modes, infinity, NaN, denormalized and zero operand representations, as well as the treatment of exceptions, such as overflow, underflow, invalid and inexact operations. This assures complete software portability between systems designed using the WTL 1232/1233 and general purpose computer systems which may be used to prototype algorithms and applications software. The WTL 1232 "FAST" mode of operation removes the time penalty of underflow exception handling by substituting zero for denormalized results, but retains all other IEEE features.

The ALU and multiplier both use dedicated circuit arrays to perform arithmetic processing functions, providing significantly faster processing than designs which rely solely on sequential, clocked logic. Array operation times include the time for performing the arithmetic functions, denormalization, renormalization and exponent adjustments.

Description, continued

The data path architecture for the WTL 1232 multiplier and WTL 1233 ALU is shown in Figure 1. As shown, a common data path structure is used for both chips. The architecture is divided into two stages in which data is loaded and unloaded, and three array stages in which arithmetic operations are performed. When the multiplier or ALU operates in pipeline mode, the three pipeline registers shown in Figure 1 separate the three array stages and three different arithmetic operations can be performed at once. When the WTL 1232 or WTL 1233 operates in flowthrough mode, internal pipeline registers appear transparent and operands flow directly through array stages 1, 2 and 3. In flowthrough mode, only one type of operation can be performed at one time.

All inputs and outputs are fully registered. To insure that data can be input and output at the maximum pipeline rate, 16-bit I/O transfers occur at twice that speed. In addition, 16-bit I/O buses reduce WTL 1232/1233 power consumption and allow the parts to be packaged in 64-pin DIP and 68-pin leadless chip carrier or pin grid array packages.

Data Path

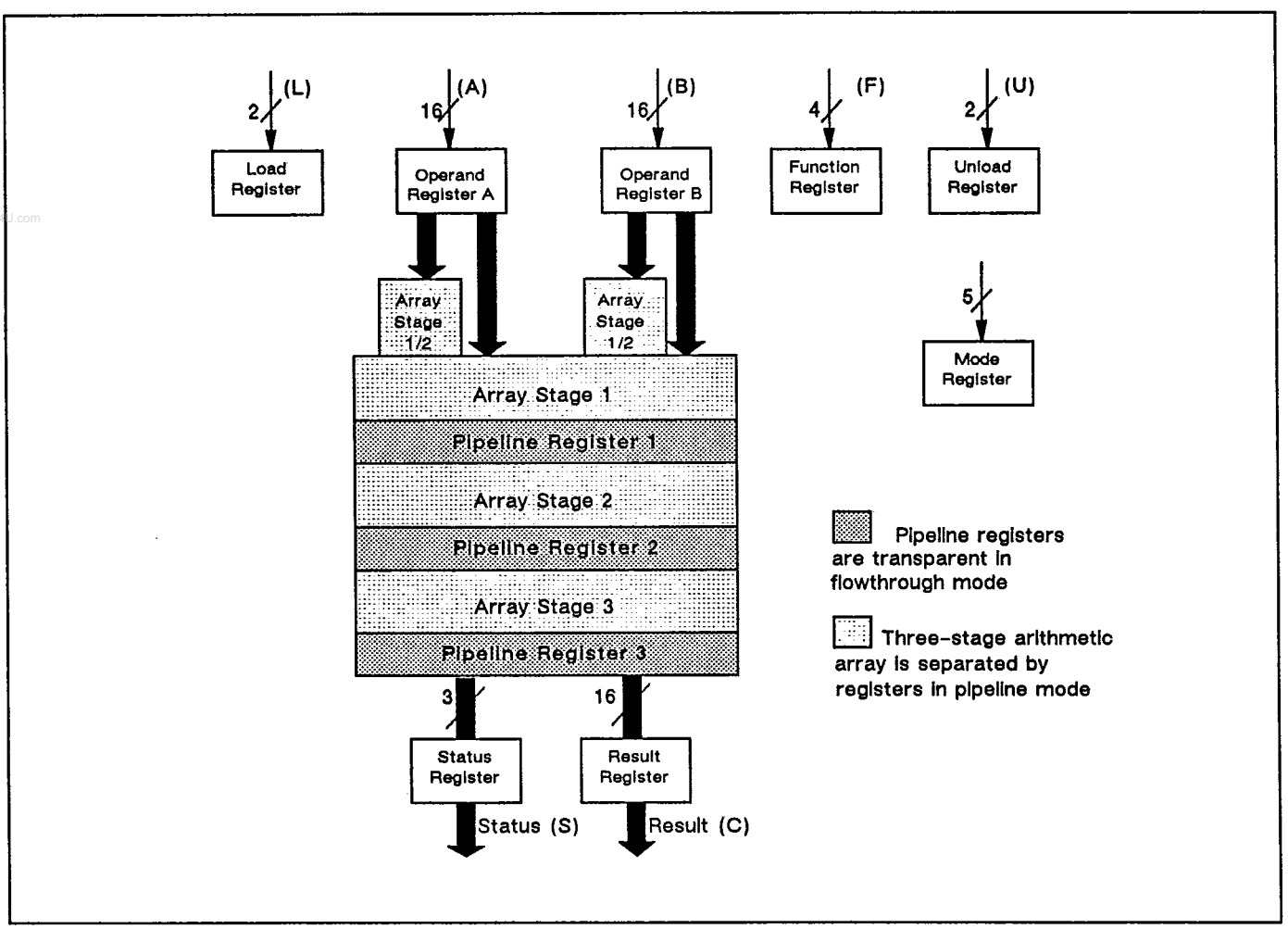


Figure 1. WTL 1232 Multiplier and 1233 ALU Data Path Architecture

July 1986

Specifications

ABSOLUTE MAXIMUM RATINGS (Above Which The Useful Life May Be Impaired)

Supply voltage ..... −0.5 to 7.0 V
Input voltage ..... −0.5 to 5.5 V
Output voltage ..... −0.5 to 5.5 V
Operating temperature range
(T_{CASE}) ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Lead temperature (10 seconds) ..... 300°C
Junction temperature ..... 175°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	1232/1233-5 COMMERCIAL		1232/1233-8 & -10 COMMERCIAL		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.75	5.25	4.75	5.25	V
V_{DD} Supply voltage	4.75	5.25	3.8	5.25	V
T_{CASE} Operating temperature	0	70	0	70	°C

PARAMETER	1232/1233-5 MILITARY		1232/1233-8 MILITARY		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{DD} Supply voltage	4.5	5.5	3.6	5.5	V
T_{CASE} Operating temperature	−55	125	−55	125	°C

Specifications, continued

DC ELECTRICAL CHARACTERISTICS, 1

PARAMETER	TEST CONDITIONS	1232/1233-5 COMM.		1232/1233-8 COMM.		1232/1233-10 COMM.		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH} High level input voltage	V_{CC}/V_{DD} = MAX	2.0		2.0		2.0		V
V_{IL} Low level input voltage	V_{CC}/V_{DD} = MIN		0.8		0.8		0.8	V
V_{OH} High level output voltage	V_{CC}/V_{DD} = MIN, I_{OH} = -.4 mA	2.4		2.4		2.4		V
V_{OL} Low level output voltage	V_{CC}/V_{DD} = MIN, I_{OL} = 4.0 mA		0.4		0.4		0.4	V
I_{IH} High level input current	V_{CC}/V_{DD} = MAX, V_{IN} = V_{CC}		±10		± 10		±10	µ A
I_{IL} Low level input current	V_{CC}/V_{DD} = MAX, V_{IN} = 0V		±10		± 10		±10	µ A
I_{OZH} Tri-state leakage current high	V_{CC}/V_{DD} = MAX, V_{IN} = V_{CC} High Z		±10		± 10		±10	µ A
I_{OZL} Tri-state leakage current low	V_{CC}/V_{DD} = MAX, V_{IN} = 0V High Z		±10		± 10		±10	µ A
I_{CC} Standby current	V_{CC} = MAX, DC conditions V_{IN} = TTL							
	1232		150		150		150	mA
	1233		50		50		50	mA
I_{CC} Standby current	V_{CC} = MAX, DC conditions V_{IL} = 0V or V_{DD}							
	1232		75		75		75	mA
	1233		50		50		50	mA
$I_{CC}+I_{DD}$ Dynamic current	V_{CC} = MAX, T_{CY} = MIN TTL Inputs							
	1232		250		250		250	mA
	1233		450		450		450	mA

Specifications, continued

DC ELECTRICAL CHARACTERISTICS, 1

PARAMETER	TEST CONDITIONS	1232/1233-5 MILITARY		1232/1233-8 MILITARY		UNIT
		MIN	MAX	MIN	MAX	
V_{IH} High level input voltage	V_{CC}/V_{DD} = MAX	2.0		2.0		V
V_{IL} Low level input voltage	V_{CC}/V_{DD} = MIN		0.8		0.8	V
V_{OH} High level output voltage	V_{CC}/V_{DD} = MIN, I_{OH} = −.4 mA	2.4		2.4		V
V_{OL} Low level output voltage	V_{CC}/V_{DD} = MIN, I_{OL} = 4.0 mA		0.4		0.4	V
I_{IH} High level input current	V_{CC}/V_{DD} = MAX, V_{IN} = V_{DD}		±10		±10	μA
I_{IL} Low level input current	V_{CC}/V_{DD} = MAX, V_{IN} = 0V		±10		±10	μA
I_{OZH} Tri-state leakage current high	V_{CC}/V_{DD} = MAX, V_{IN} = V_{CC} High Z		±10		±10	μA
I_{OZL} Tri-state leakage current low	V_{CC}/V_{DD} = MAX, V_{IN} = 0V High Z		±10		±10	μA
I_{CC} Standby current	V_{CC} = MAX, DC conditions V_{IN} = TTL					
	1232		200		200	mA
	1233		50		50	mA
I_{CC} Standby current	V_{CC} = MAX, DC conditions V_{IL} = 0V or V_{DD}					
	1232		100		100	mA
	1233		50		50	mA
$I_{CC}+I_{DD}$ Dynamic current	V_{CC} = MAX, DC conditions TTL inputs					
	1232		300		300	mA
	1233		500		500	mA

Specifications, continued

AC SWITCHING CHARACTERISTICS, 1, 2

PARAMETER	TEST COND.	1232/1233-5 COMMERCIAL		1232/1233-8 COMMERCIAL		1232/1233-10 COMMERCIAL		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{CY} Clock cycle time	V_{CC}/V_{DD} = MIN See Figure 8	100		62.5		50		nsec
T_{CH} Clock high time	See Figure 8	40		25		20		nsec
T_{CL} Clock low time	See Figure 8	40		25		20		nsec
T_S Input setup time	See Figure 8	25		20		15		nsec
T_H Input hold time	See Figure 8	3		3		3		nsec
T_{DO} Output delay time	See Figure 8		35		35		35	nsec
T_{ENA} Tri-state enable time	See Figure 9		55		55		47	nsec
T_{DIS} Tri-state disable time (3)	See Figure 9		55		55		47	nsec
	See Figure11							
T_{OP} Flowthrough operation time								
WTL1232 Floating Point Multiplier			700		435		350	nsec
WTL1233 Floating Point ALU			700		435		350	nsec
T_{LA} Total latency			900		565		450	nsec
	See Figure 12							
T_{OP} Pipelined operation time per stage								
WTL1232 Floating Point Multiplier			200		125		100	nsec
WTL1233 Floating Point ALU			200		125		100	nsec
T_{LA} Total latency			1000		625		500	nsec

Specifications, continued

AC SWITCHING CHARACTERISTICS, 1, 2

PARAMETER	TEST CONDITIONS	1232/1233-5 MILITARY		1232/1233-8 MILITARY		UNIT
		MIN	MAX	MIN	MAX	
T_{CY} Clock cycle time	V_{CC}/V_{DD} = MIN See Figure 8	100		62.5		nsec
T_{CH} Clock high time	See Figure 8	40		25		nsec
T_{CL} Clock low time	See Figure 8	40		25		nsec
T_S Input setup time	See Figure 8	25		15		nsec
T_H Input hold time	See Figure 8	3		3		nsec
T_{DO} Output delay time	See Figure 8		35		35	nsec
T_{ENA} Tri-state enable time	See Figure 9		55		55	nsec
T_{DIS} Tri-state diable time (3)	See Figure 9		55		55	nsec
T_{OP} Flowthrough operation time	See Figure 11					
WTL1232 Floating Point Multiplier			700		435	nsec
WTL1233 Floating Point ALU			700		435	nsec
T_{LA} Total latency			900		565	nsec
T_{OP} Pipelined operation time per stage	See Figure 12					
WTL1232 Floating Point Multiplier			200		125	nsec
WTL1233 Floating Point ALU			200		125	nsec
T_{LA} Total latency			1000		625	nsec

1. Worst case over temperature and power range.
2. TTL inputs of 0.4V and 3.5V. Timing transitions measured at 1.5V unless otherwise noted.
3. Device must be powered for at least 20 ms before measurement is performed. T_{DIS} is not tested but is guaranteed by design.

Specifications subject to change without notice.

I/O Characteristics

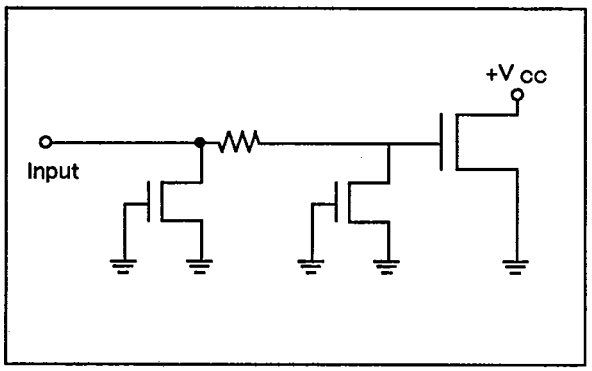


Figure 2. WTL 1233 Input Equivalent Circuit

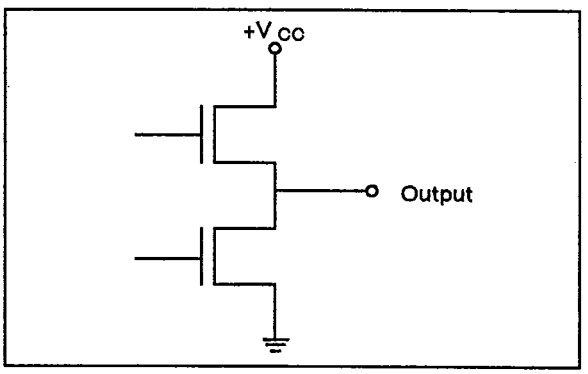


Figure 3. WTL 1233 Output Equivalent Circuit

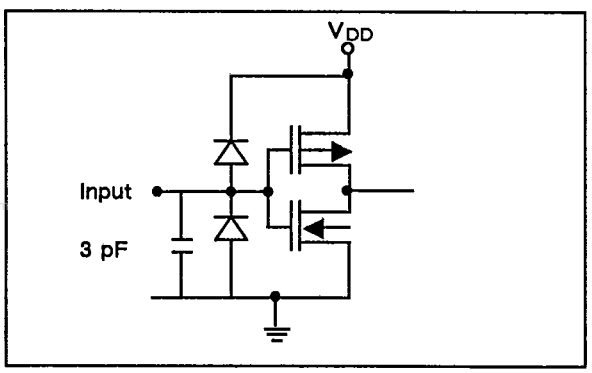


Figure 4. WTL 1232 Input Equivalent Circuit

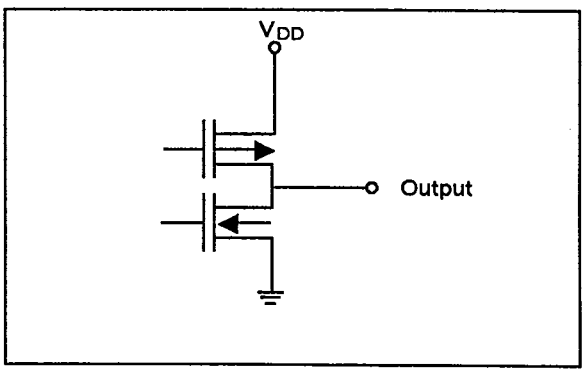


Figure 5. WTL 1232 Output Equivalent Circuit

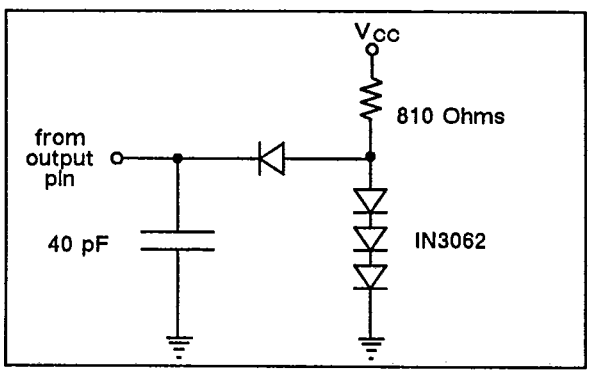


Figure 6. Test Load for Delay Measurement

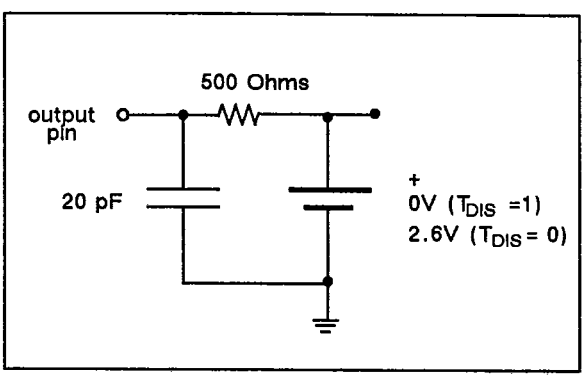


Figure 7. Test Load for Tri-State Delay Measurement

I/O Characteristics, continued

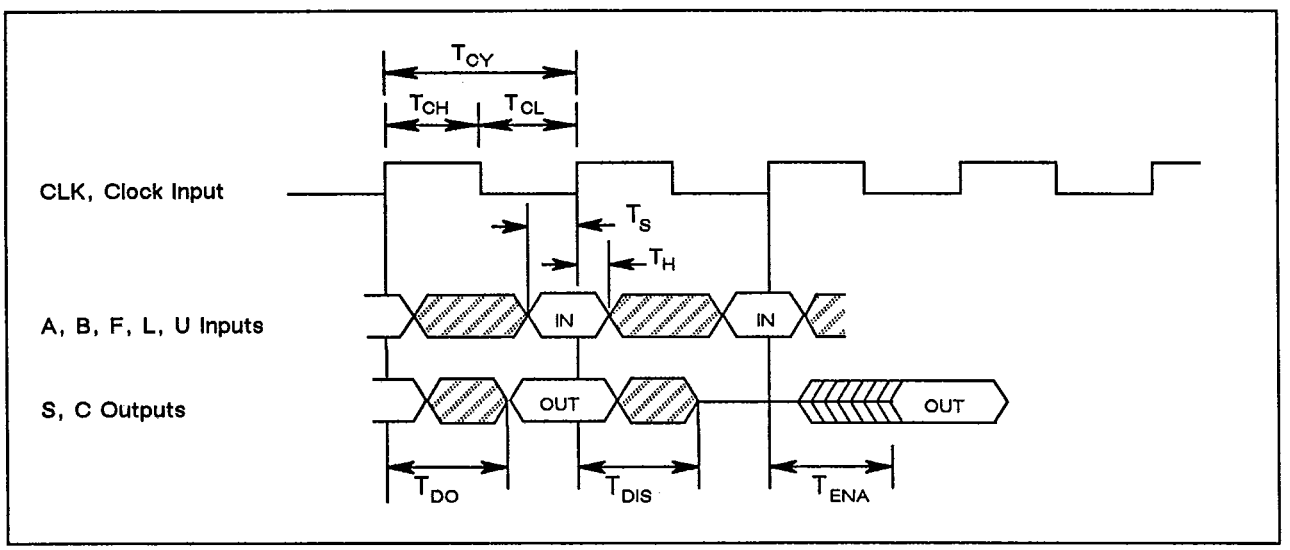


Figure 8. Switching Characteristics

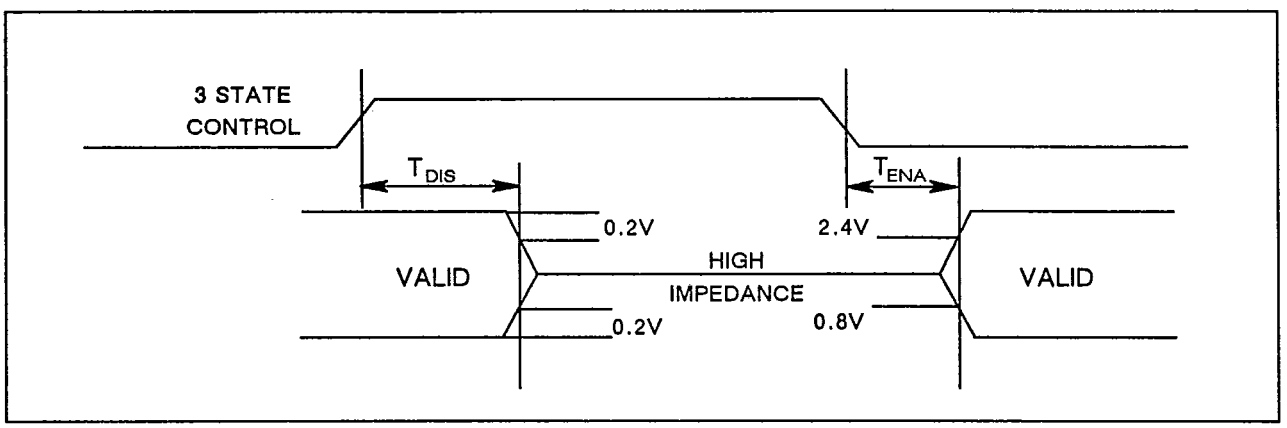


Figure 9. Tri-State Enable/Disable Timing Diagram

Signal Description

A_{15-0}

A inputs alternately contain the most significant half (16 bits) and the least significant half of the 32-bit A operand. A_0 is the least significant bit. The most significant word is loaded when specified by the load inputs; the least significant is loaded on the next CLK.

B_{15-0}

B inputs alternately contain the most significant half (16 bits) and the least significant half of the 32-bit B operand. B_0 is the least significant bit. The most significant word is loaded when specified by the load inputs; the least significant is loaded on the next CLK.

Signal Descriptions, continued

C_{15-0}

C outputs are 16-bit portions of the 32-bit result. The most or least significant half is selected by the unload inputs.

CLK

This signal clocks the internal registers. The positive-going edge loads all input and output registers as well as pipeline registers, when enabled by load instructions.

L_{1-0}

LOAD inputs control the transfer of input data from input registers A, B and F into internal processor registers and the mode register.

U_{1-0}

UNLOAD inputs select either the most significant half (MSH) or the least significant half (LSH) to be loaded into output registers. Unload inputs also enable and disable tristate output buffers. U_0 is used to load the mode register.

F_{3-0}

FUNCTION inputs select which functions are performed by the multiplier and ALU. FUNCTION inputs are also used to load the mode register.

S_{2-0}

STATUS outputs indicate exception conditions specified by IEEE Standard 754 (Overflow, Underflow, Invalid or Inexact) and multiplier denormalized operand.

GND

All GND pins must be connected to system ground (0.0 volts).

V_{CC}

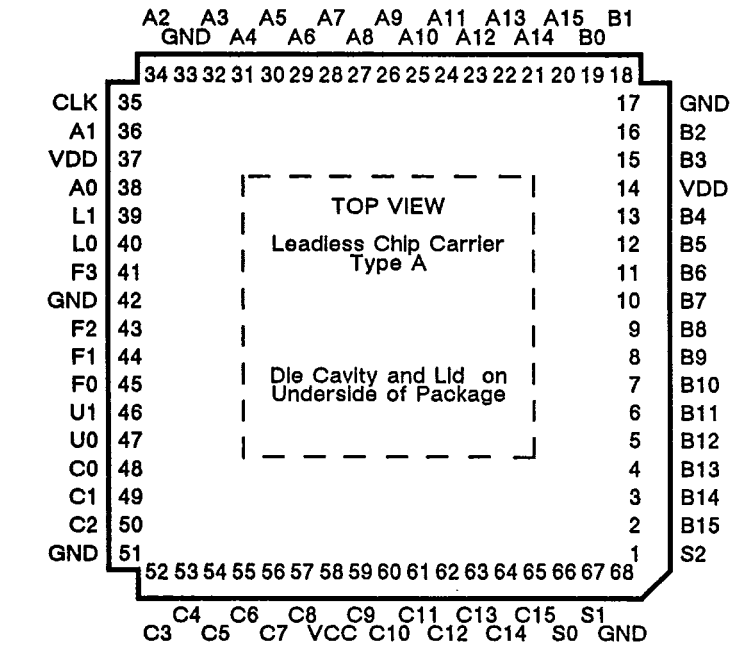
All V_{CC} pins must be connected to supply voltages of +5.0 volts.

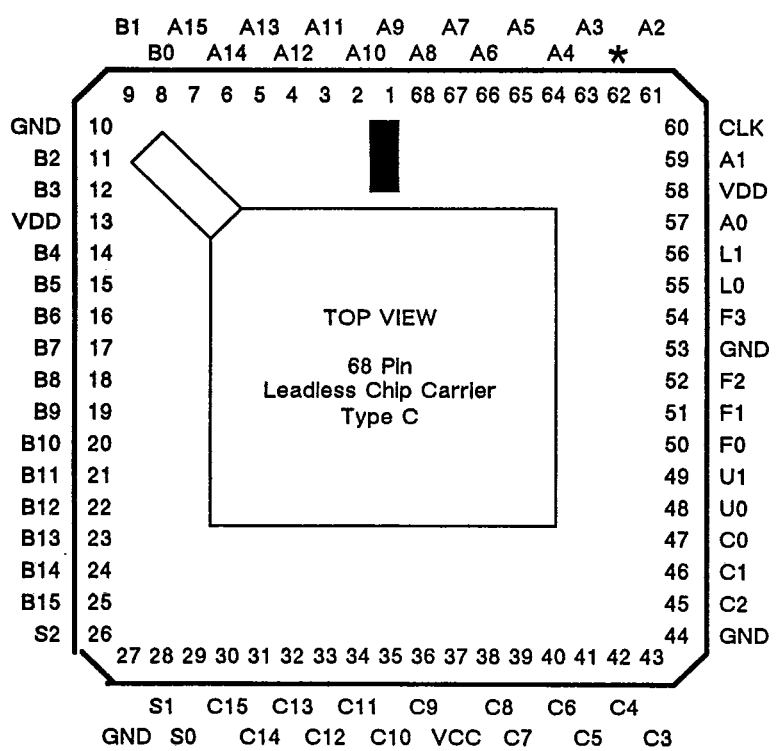
V_{DD}

The V_{DD} pins may be connected to either a +5V or +4V supply.

July 1986

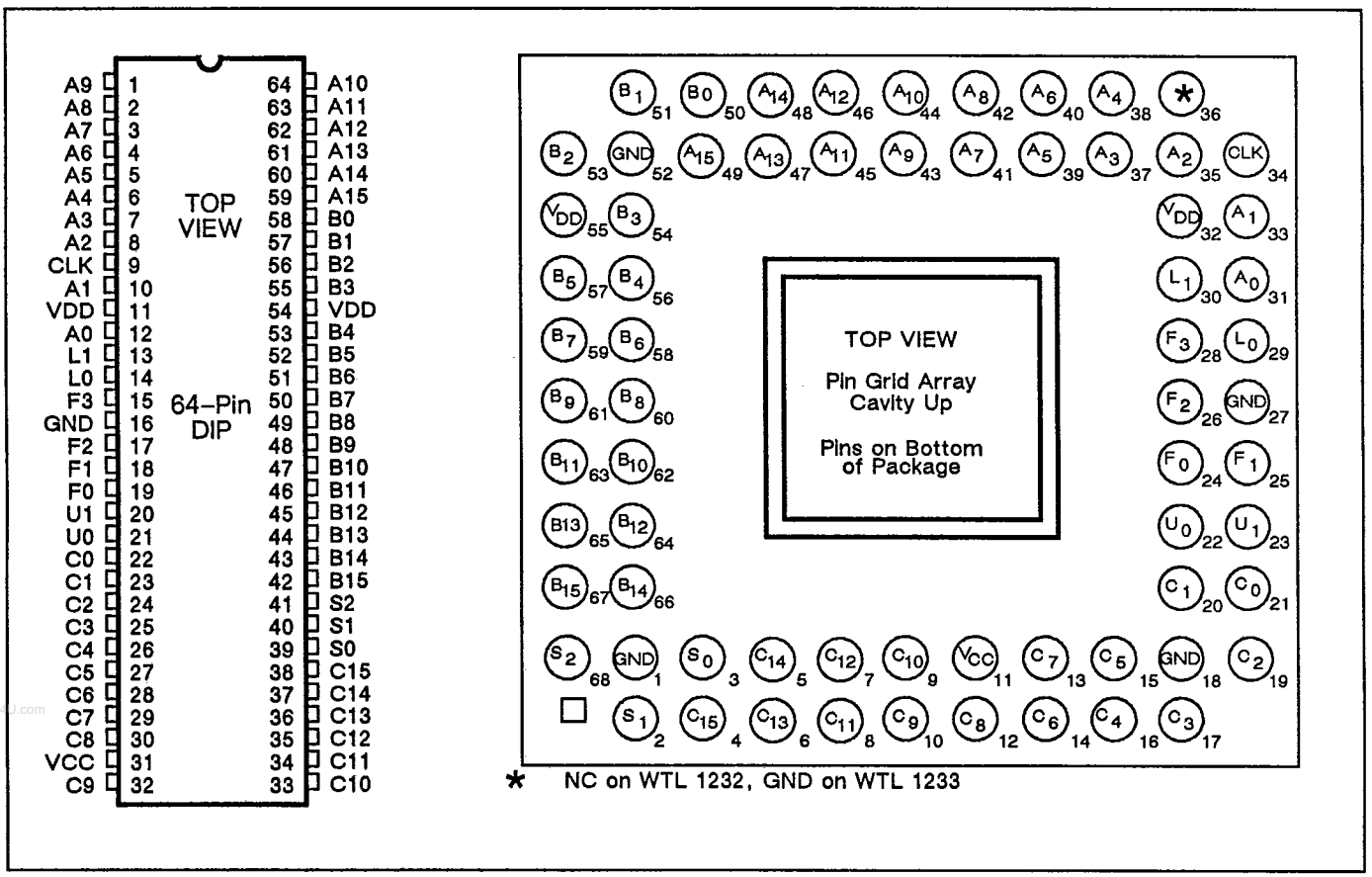
Pin Configuration





*NC on WTL 1232, GND on WTL 1233

Pin Configuration, continued

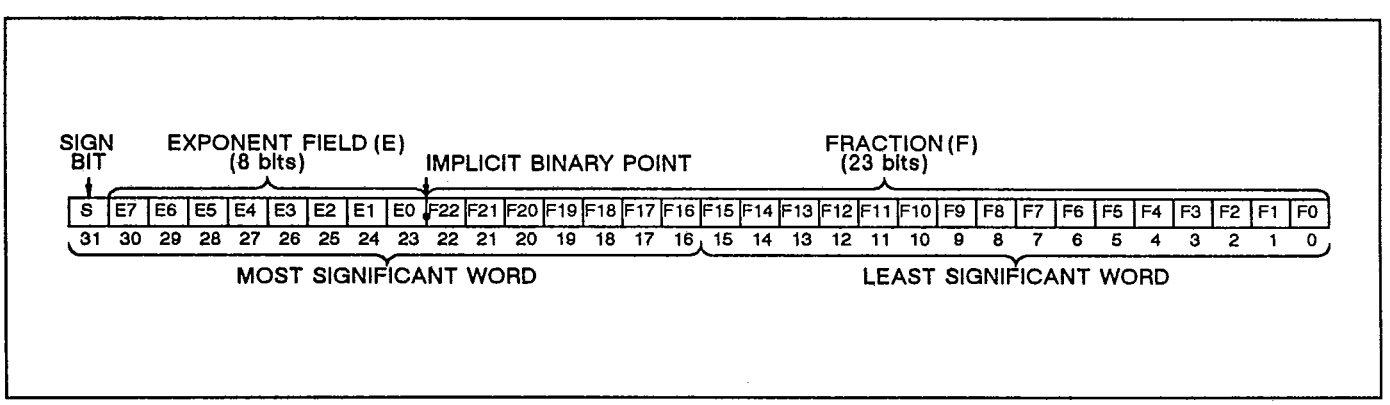


Data Formats

32-BIT FLOATING POINT (IEEE STANDARD)

The IEEE standard 32-bit floating point word is divided into three fields: a sign bit, an 8-bit exponent and a 23-bit fraction field, as shown below.

The sign bit indicates the sign of the floating point number. Negative numbers have a sign bit value of 1; positive numbers have a sign bit value of 0. The value zero may have either sign.



Data Formats, continued

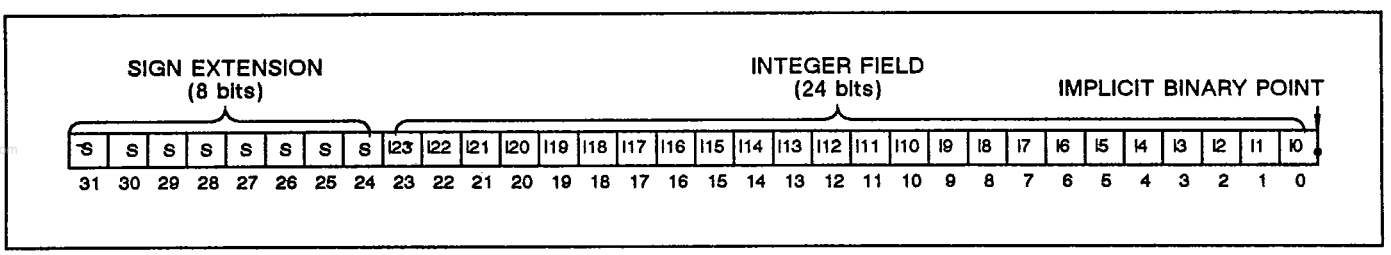
The value is determined by the following:

E	F	VALUE	NAME	MNEMONIC
255	Not all zeros	—	Not a number	NaN
255	All zeros	$(-1)^S$ (Infinity)	Infinity	INF
1–254	Any	$(-1)^S (1.F)2^{E-127}$	Normalized number	NOR
0	Not all zeros	$(-1)^S (0.F)2^{-126}$	Denormalized number	DNRM
0	Zero	$(-1)^S$ 0.0	Zero	ZERO

The value contained in the 8-bit exponent field represents a power of two with a bias value of +127 added, as shown in the value chart. The significand is multiplied by two raised to the power (–127) to produce a floating point value.

The significand field contains the 23-bit fraction and the hidden bit. Inserted during arithmetic processing, the hidden bit has a value of 1 for all normalized numbers and 0 for zero and denormalized number values. The fraction is the 23 least significant bits to the right of the hidden bit. Bit F_{22} has a value of 2^{-1}; bit F_0 has a value of 2^{-23}; the hidden bit has a value of 2^0.

24-BIT FIXED POINT TWO'S COMPLEMENT



The value of the 24-bit integer field shown above can range from $2^{23}-1$ to -2^{23} and must be sign-extended to 32 bits before performing a FLOAT operation, in which the number is converted to floating point format. The eight-bit sign extension field is a repeat of bit 23, the "sign" bit of the two's complement number. When presenting two's complement integers to the WTL 1233, the value of the eight sign extension bits must be consistent with the sign bit.

ALU operations to convert between the two data formats are described in "Function Controls".

Definitions

AFFINE MODE

A mode of operation in which the the sign of infinity is preserved.

BIASED EXPONENT

The true exponent of a floating point number, plus a constant. For single precision IEEE floating point numbers, the constant is 127.

DENORMALIZED NUMBER

A number with absolute magnitude less than 2^{-126} (the smallest normalized number). Denormalized numbers have a hidden bit value of 0.

EXPONENT

A number representing the power of two by which a floating point number's significand is to be multiplied. For the floating point number 1.101×2^{-3}, for example, the exponent is −3.

"FAST" MODE

In the multiplier, a mode of operation in which zero is substituted for denormalized inputs and underflow results, eliminating special handling and time penalties.

FLOATING POINT NUMBER

A bit string that contains a sign, a biased exponent and a significand; it has a value equal to the signed product of the significand and two raised to the power of the unbiased exponent.

FLOWTHROUGH MODE

A mode of operation in which internal pipeline registers appear transparent to data.

FRACTION

The least significant 23 bits of the significand that lie to the right of a number's implied binary point.

HIDDEN BIT

The most significant bit (MSB) of a significand that lies to the left of the implied binary point. The hidden bit is not stored in memory, instead it is added by the floating point processor in the first stages of an operation.

IEEE MODE

A mode of operation which facilitates denormalized number handling by the multiplier chip.

NORMALIZED NUMBER

A number in which the significand's hidden bit equals 1. The true exponent of a normalized number is between −126 and 127.

OPERATION TIME

The minimum number of clock cycles required between successive operations.

PIPELINE MODE

A mode of operation in which up to five operations can be in progress at one time: data is loaded and output in two stages, while operations are performed in three internal stages separated by pipeline registers.

ROUNDING MODES

Four modes in which the infinitely precise result may be rounded to fit the floating point destination format.

SIGNIFICAND

The portion of a floating point number containing the fraction and hidden bit, which is then multiplied by a power of two to produce the floating point number.

TOTAL LATENCY

The number of clock cycles between the start of an operation and the time when the result may be used to start a subsequent operation.

WRAPPED NUMBER

The result of an ALU wrap operation that converts a denormalized number into a format usable by the multiplier.

Operations

ALU OPERATION

A typical floating point operation performed by the ALU is an add or subtract operation. WTL 1232/1233 results are rounded to 24 bits of significand. In the following example, however, a 5-bit significand is used for simplicity.

Operand A		Operand B		Result	
$1.1101 \cdot 2^4$	+	$1.1010 \cdot 2^2$	=	$1.0010 \cdot 2^5$ *	* RN Rounding Mode

The MSH of both operands is loaded into the data path first through operand registers A and B as shown in Figure 1. The 16-bit MSH always contains the operand exponent and the most significant bits of the significand fraction. The LSH is loaded next, while Array Stage 1/2 begins processing the MSH.

At Array Stage 1/2, the exponent is examined to see if it is 0. If the exponent is 0, it indicates either zero or a denormalized number, and the hidden bit is set to 0. Otherwise, the hidden bit is set to 1. The exponents are then compared. Since operand exponents must be the same to perform floating point operations, a flag is set to indicate which exponent is larger. In the sample given above, operand A is larger than operand B; the difference between exponents is two. The difference between the two exponents is stored for use in Stage 1.

At Array Stage 1, the fraction of the smaller operand is right-shifted until the exponents are the same. In our example, the fraction of operand B is right-shifted two digits while the exponent is incremented thus:

$$\text{Stage 1 Result} = 1.1010 \cdot 2^2 = 0.01101 \cdot 2^4$$

The two fractions are then added and the result — in our example, 10.00111 — is sent to Array Stage 2.

In Array Stage 2, the Stage 1 result is examined to determine if it is normalized. If the result is not a normalized number, Array Stage 2 determines how many bit shifts are required to normalize it. Since the IEEE format has a sign-magnitude representation for the significand, a negative (two's complement) result is complemented before being passed on to Array Stage 3. In our example, the Stage 1 result must be right-shifted one bit to be normalized, but it is positive and does not need to be complemented.

At Array Stage 3, the significand is rounded and normalized. The exponent is adjusted and checked for underflow or overflow and exception flags are sent to the status register. To normalize our example result, the significand is right-shifted one bit and the exponent is incremented:

$$10.00111 \cdot 2^4 = 1.000111 \cdot 2^5$$

As mentioned, round-to-nearest, or RN, mode is selected in our example operation and at Stage 3 the significand is rounded to five bits to produce the final result:

$$1.000111 \cdot 2^5 = 1.0010 \cdot 2^5$$

There is no underflow or overflow in this operation, but since the result is not equal to the infinitely precise result ($1.000111 \cdot 2^5$), an exception flag is generated in the status register, indicating that the result is inexact. An inexact result is generated if any of the discarded significand bits is equal to one.

Operations, continued

MULTIPLIER OPERATION

The multiplier array is conceptually simpler than the ALU. In Array Stage 1/2, the exponent range is extended so that wrapped exponents become unwrapped (valid) exponents. The multiplier does not align operands in Stage 1. Instead, array stages 1 and 2 comprise a two-stage combinational array that performs 24 x 24-bit significand multiplication. Source exponents are added together.

In Array Stage 3, multiply results are normalized and rounded. The rounded result is checked for overflow and underflow (IEEE/"FAST" mode) and the status code is generated. The result produced on underflow is dependent on $MODE_4$ and is described below. The result produced on overflow is dependent on the rounding mode and is defined in the Overflow Output Table in the Status Output section.

Block Diagram

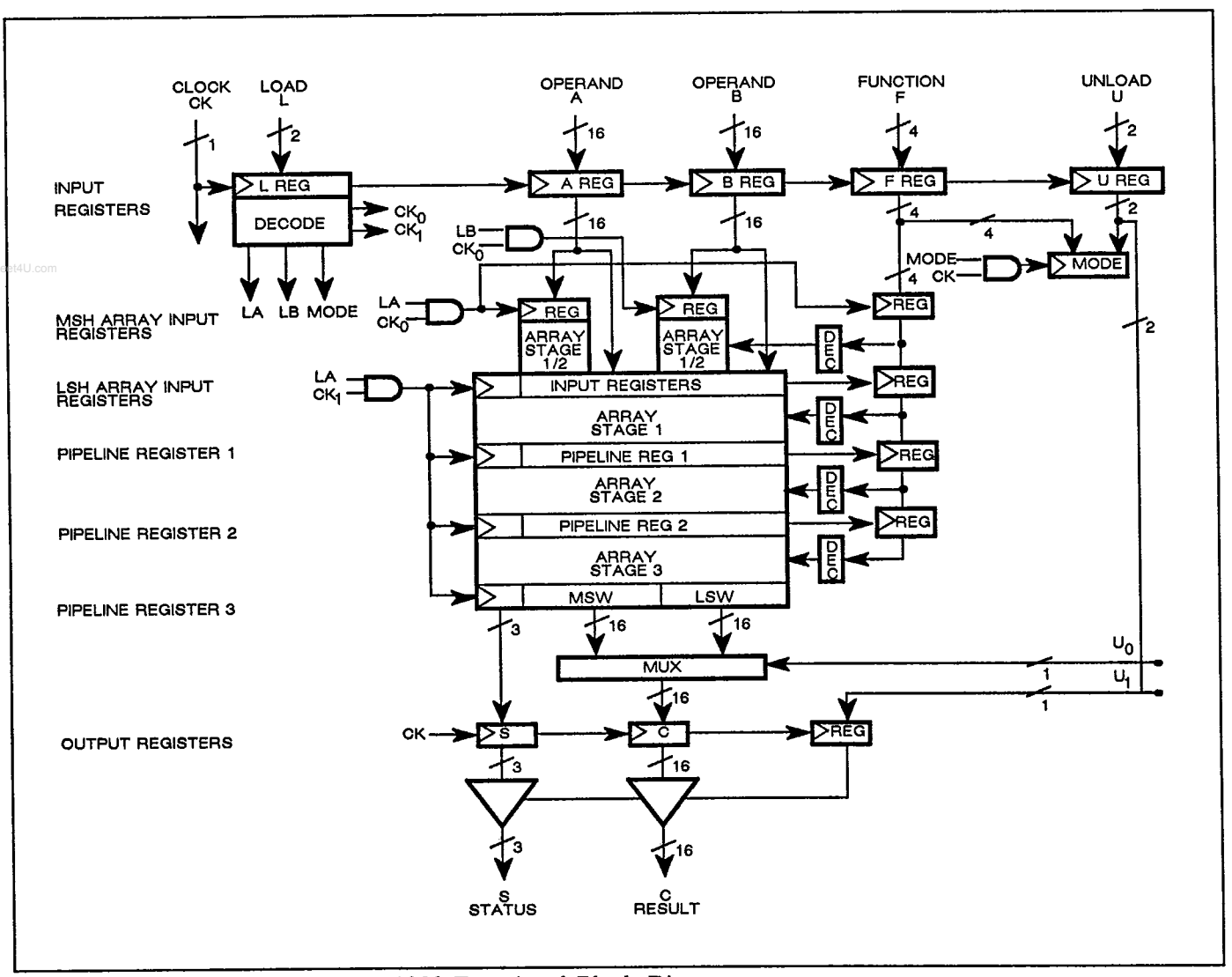


Figure 10. WTL 1232 and WTL 1233 Functional Block Diagram

Functional Description

FUNCTION CONTROLS

The 4-bit function instruction determines which arithmetic operations are performed by the ALU and multiplier during each cycle. Function bits are decoded differently for the two chips, as shown in the separate ALU and Multiplier Instruction tables.

On each positive clock transition, the arithmetic function is entered in the F Input Register and is transferred to the array on the next clock transition following a LAB or LA instruction. The function instruction must be furnished at the same time as the MSH of the operands.

IEEE Standard 754, Version 10 incorporates denormalized numbers (DNRMs) to allow a means of gradual underflow for operations that produce non-zero results too small to be expressed as a normalized floating point number (for example, 2^{-139}). The WTL 1233 conforms to the requirements of the IEEE standard for handling denormalized numbers. The WTL 1232 does not directly perform operations on denormalized numbers but facilitates complete denormalized number handling using ALU WRAP and UNWRAP instructions. See the following ALU and multiplier function descriptions for information on denormalized number handling.

Multiplier Functions

The WTL 1232 multiplier operates in two modes, IEEE and "FAST". IEEE mode is used when denormalized number handling is required. In IEEE mode, operations are performed on normalized and wrapped normalized numbers. "FAST" mode is used to avoid the overhead associated with denormalized number handling. Wrapped multiplies are not used in "FAST" mode.

Denormalized operands are treated differently in the two modes. In "FAST" mode, denormalized inputs and outputs are flushed to zero and no further processing is needed. In IEEE mode, the multiplier generates a denormalized operand exception to the Status Register when a denormalized operand is detected.

The ALU performs a WRAP instruction on the denormalized operand(s), normalizing the significand by permitting the exponent field to "wrap around" so that the number is normalized, although it may have a negative exponent. The number is then sent back to the multiplier where it is multiplied using one of the wrapped multiply function codes.

At the completion of the multiply operation, if the multiplication gives a value smaller than the smallest normalized number (2^{-126}), the status code indicates UNF or UNF + INX (status codes 2 and 3). In this case, the WTL 1232 produces a normalized, unrounded value (UNRM) and the result must be turned into a denormalized number in the ALU with an UNWRAP instruction. At the completion of the UNWRAP operation, the status code correctly indicates underflow conditions. If the result of the multiply operation is within the normalized number range, no further processing is required. See the ALU function description for more information on WRAP and UNWRAP operations.

FUNCTION INSTRUCTION TABLE
1232 FLOATING POINT MULTIPLIER

F_3 F_2 F_1 F_0	MNEMONIC	OPERATION
0 0 0 0	A x B	Multiply normalized floating point operands A and B
0 0 0 1	WA x B	Multiply wrapped (negative exponent) operand A and normalized floating point operand B
0 0 1 0	A x WB	Multiply normalized floating point operand A and wrapped (negative exponent) operand B
0 0 1 1	WA x WB	Multiply wrapped (negative exponent) operands A and B
0 1 x x	–	Reserved
1 x x x	–	Reserved

Note: F_2 and F_3 must be low during all multiplier load cycles.

ALU Functions

The ALU always operates in IEEE mode. It performs single precision floating point operations that conform to the requirements of IEEE Standard 754, as well as the WRAP, UNWRAP, FLOAT and FIX operations described below.

Functional Description, continued

WRAP operations are performed on denormalized numbers (DNRMs). DNRMs have an unbiased exponent value of −126 and a hidden bit value of 0. In a WRAP function, the ALU converts a DNRM to a wrapped normalized number (WNRM) by left-shifting the fraction as many bit positions as necessary until the hidden bit is a one. The exponent is changed to 1 minus the number of bit positions shifted left, with the exponent allowed to "wrap around" or become negative. The WRNM result can then be used as an operand by the multiplier following the wrapped multiply instructions.

UNWRAP operations are performed on unrounded, normalized numbers (UNRMs). UNRMs are created by the WTL 1232 multiplier when the result of a multiply operation is smaller than the smallest normalized number (2^{-126}). Since the multiplier cannot produce denormalized numbers directly, the UNRM must be changed to a DNRM using the UNWRAP instruction. The UNRM is placed on the A operand input of the ALU and the inexact bit (Status Bit 0 from the multiply operation) is placed into the least significant bit of the B operand. The inexact bit is required for the denormalized result to be correctly rounded. At the conclusion of the UNWRAP operation, the status code will correctly indicate true IEEE conditions (underflow, inexact result).

WRAP and UNWRAP operations are only used when the multiplier is in IEEE mode. The multiplier flushes DNORMs to zero in "FAST" mode and the ALU handles denormalized numbers directly.

FLOAT operations convert 24-bit, fixed point, two's complement integer values to 32-bit floating point. Before performing a FLOAT operation, the 24-bit integer must be sign-extended to 32 bits. The 8-bit sign extension field is a repeat of bit 23, the "sign" bit of the two's complement number. The value of an integer can range from $2^{23}-1$ to -2^{23}.

A FIX operation converts 32-bit floating point numbers to 24-bit two's complement integers (sign-extended to 32 bits). A FIX function can only be performed when the RZ rounding option is selected. If the floating point number is larger than the maximum 24-bit integer value, an overflow (OVF) exception is signaled. For values with magnitudes between 2^{23} and 2^{24} the maximum representable integer value with the correct sign is the result. For values with magnitudes of 2^{24} or larger the result is not defined. For more information on exceptions, see the Status Output description.

FUNCTION INSTRUCTION TABLE
WTL 1233 FLOATING POINT ALU

F_3 F_2 F_1 F_0	MNEMONIC	OPERATION
0 0 0 0	WRAP A	Converts a denormalized number to a normalized number with an underflowed or wrapped exponent
0 0 0 1	UNWRAP A	Converts an unrounded normalized underflow result to a rounded denormalized number
0 0 1 0	FLOAT A	Converts a 24-bit integer to a 32-bit normalized floating point number
0 0 1 1	FIX A	Converts a 32-bit floating point number to a 24-bit integer
0 1 0 0	A + B	Floating point addition of operands A and B
0 1 0 1	A − B	Floating point subtraction of operands A minus B
0 1 1 0	−A + B	Floating point addition of operands minus A plus B
0 1 1 1	|A| + |B|	Floating point addition of operands |A| plus |B|
1 0 0 0	|A − B|	Absolute value of floating point subtraction of operand A minus B
1 0 0 1	|A + B|	Absolute value of floating point addition of operands A plus B
1 0 1 x	–	Reserved
1 1 x x	–	Reserved

Functional Description, continued

LOAD CONTROLS

Load instructions, as shown in the Load Instruction Table, control the loading of operands through operand input registers A and B, and loading the Mode register through input registers F and U. At power up, LMODE must be generated to initialize and load the Mode register; during operation, LMODE is used to change modes.

The LAB operation loads the A and B operands into the array. Two consecutive load instructions are required to load the MSH and LSH. Operands are always loaded into the array MSH first, followed immediately by the LSH.

During a multiplication or addition with a constant, LAB is used to load both the first and the constant operands into the array. From that point on, LA is used to load new operands; the WTL 1232/1233 retain operand B until a new B operand is loaded. After NOP or LMODE, the operation should always start with loading MSH first.

In flowthrough mode, NOP is used for no-operand loading. At least five NOP cycles occur between loading an operation's LSH and unloading the resultant MSH. NOP cannot be inserted between loading MSH and LSH into the array.

LOAD INSTRUCTION TABLE

L_1 L_0	MNEMONIC	OPERATION
0 0	NOP	No loading
0 1	LAB	Load operands A and B into array
1 0	LA	Load operand A only into array
1 1	LMODE	Load MODE register from F and U input registers

UNLOAD CONTROLS

Unload instructions control the transfer of array data into the C Output Register and the transfer of status information into the S Output Register. In addition, Unload instructions enable tristate register outputs. Data is typically unloaded from the array most significant half (UMS) first, followed by the least significant half (ULS). Unload data is selected at the first positive clock edge following an unload command; at the next positive clock edge, the data is loaded into registers C and S, and the register outputs are enabled.

UNLOAD INSTRUCTION TABLE

U_1 U_0	MNEMONIC	OPERATION
0 0	UMS	Unload most significant half from array into output register
0 1	ULS	Unload least significant half from array into output register
1 x	DAB	Disable output register's three-state outputs to high impedence

MODE CONTROLS

The Mode register controls the operation of the WTL 1232/1233 floating point chip set. A user can select between pipeline or flowthrough operations, between four rounding modes and between either IEEE or "FAST" modes. Mode options are selected by four function input bits and unload bit U_0.The operating mode is entered into the F and U input registers on the same positive clock transition as the LMODE instruction. The new mode is effective after the next positive clock transition. The mode register must be loaded at power up before the first operand is loaded. mode register contents should not be changed while operations are in progress. Mode instruction decoding is shown below.

Functional Description, continued

F_3 F_2 F_1 F_0 U_0	MODE INSTRUCTION TABLE	
M_4 M_3 M_2 M_1 M_0	MNEMONIC	OPERATION
x x x x 0	FLOW	Data flows through array without pipeline registers
x x x x 1	PIPE	Data is clocked through three pipeline registers in the array
x x 0 0 x	RN	Round to nearest number, or even number if a tie
x x 0 1 x	RZ	Round to zero
x x 1 0 x	RP	Round toward positive infinity
x x 1 1 x	RM	Round toward minus infinity
x 0 x x x	AI*	Affine infinity (sign preserved)
0 x x x x	IEEE	Treats denormalized operands according to IEEE standard
1 x x x x	FAST	Replaces denormalized operands with 0 (WTL 1232 only)

*M_3 must be set to zero.

"FAST"/IEEE Modes

Remember that the WTL 1232 floating point multiplier can operate in either "FAST" or IEEE mode. The WTL 1233 operates in IEEE mode only, since denormalized numbers are handled directly.

IEEE mode allows full support of all IEEE single precision formats including denormalized numbers. Denormalized numbers are flagged when used as multiply operands. The ALU WRAP instruction is used to normalize the input operand and denormalized results are produced with the UNWRAP instruction. (See the function definitions for the multiplier and ALU for more information on IEEE handling.) FLOW mode is usually selected when operating in IEEE mode, (M_0 = 0).

"FAST" mode allows support of all IEEE single precision formats except for denormalized numbers. In "FAST" mode, denormalized inputs and outputs smaller than 2^{-126} are replaced with 0. This eliminates the extra handling required for processing denormalized numbers in the multiplier. "FAST" mode is usually selected when operating in PIPE mode (M_0 = 1).

FLOWTHROUGH/PIPELINE MODES

Pipeline mode allows maximum performance to be obtained in situations where operations may be overlapped, such as graphics transformations and digital signal processing. Flowthrough mode is used for applications where one instruction must be completed before another may be started. An example of a flowthrough mode application might be a floating point coprocessor for an engineering workstation.

This section describes the flowthrough and pipeline modes of operation for the WTL 1232 multiplier and WTL 1233 ALU. Refer to Figure 10 (functional block diagram) and figures 11 and 12 (flowthrough and pipeline mode timing diagrams). In this description, references to clock cycles imply the rising clock edge, unless otherwise stated.

Flowthrough Operation

LMODE is used when changing from pipeline to flowthrough mode. This occurs at the start of the first clock cycle, as shown in Figure 11. Changing to flowthrough mode causes pipeline registers 1, 2 and 3 to be bypassed, decreasing total latency by one cycle but allowing only one operation at a time in the arithmetic array.

During cycles 2 and 3, operands and the function instruction are loaded through A, B and F registers. Two successive LA or LAB Load commands first load the MSH of operand A or operands A and B in Cycle 2, immediately followed in Cycle 3 by the LSH. The function instruction must be valid at the same time as the MSH. The arithmetic array is loaded with the operands one cycle later, at Cycle 4.

Functional Description, continued

Operand and function loading is followed by at least five NOP (No Operation) load instruction cycles. At the beginning of Cycle 9, an Unload command (UMS) is loaded, causing the MSH of the result to be clocked into the output register (Register C) and enabled onto the C Bus at the start of Cycle 10. A ULS instruction is clocked into the U register at Clock Cycle 10, which selects the LSH to be clocked into the output register at the start of Cycle 11. The status register is loaded at the beginning of Cycle 10 and is valid for two cycles. Note that unloading the part does not destroy the result.

New data and functions may be loaded at the start of Cycle 9, causing the input registers to the arithmetic unit to be loaded at Cycle 11. Note that unloading the part does not destroy the result. Results are guaranteed to be valid until two clock cycles after a new load operation has begun. As shown in the timing diagram, operation time begins with Cycle 3 and ends with Cycle 10 for a minimum operation time of seven cycles. Latency begins at Cycle 2 and ends at Cycle 11 for a Total Latency of nine cycles.

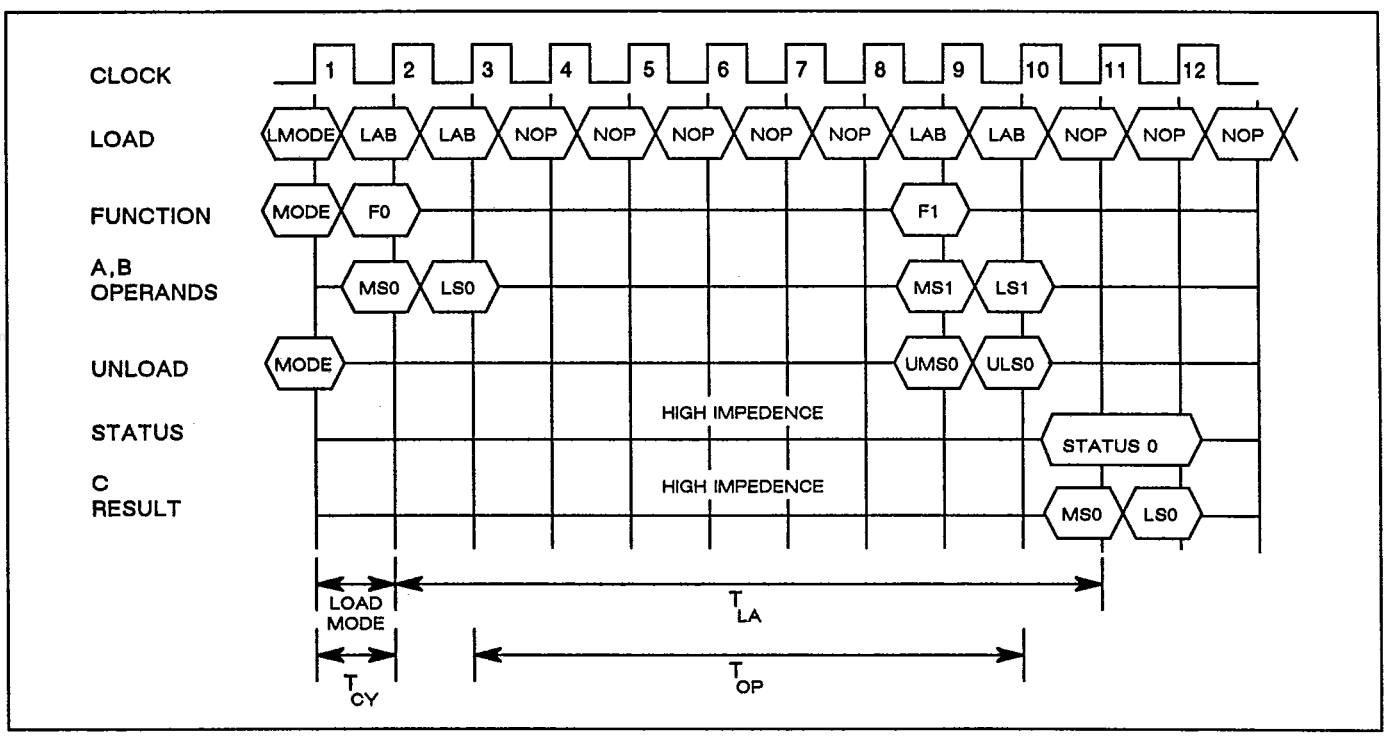


Figure 11. Flowthrough Mode Timing Diagram

Pipeline Operation

In pipeline mode, new values and instructions may be entered every two cycles. This is possible because the arithmetic array is divided into three stages, separated by pipeline registers. This adds one cycle to the total latency for an operation but allows multiple operations to be in progress at the same time.

The LMODE instruction is clocked at the start of Cycle 1. The mode instruction selects pipeline operations ($M_0 = 1$) and should select "FAST" mode ($M_4 = 1$). Loading the mode register enables the three pipeline registers and resets the input phase of the devices so that at Cycle 2 the most significant 16 bits of the operands are loaded, followed by the least significant at Cycle 3. The input phase cycles MSH, LSH, MSH, etc., until another LMODE or NOP instruction is input. For valid operation, LMODE or NOP should be asserted only after loading LSH.

Functional Description, continued

New instructions are loaded in cycles 2, 4, 6, 8, ..., although the first operation is not finished until Cycle 12. The clock cycles 2 to 11 are referred to as "filling the pipe". At the start of Cycle 4, the first two operands (MS_0 and LS_0) are loaded into the input registers of the arithmetic array. At Cycle 6, the result of Array Stage 1 is loaded into Pipeline Register 1 and at the same time, MS_1 and LS_1 are clocked into the array input registers. In general, as new operations are started, those operations currently in progress advance to the next stage. Once the pipe is full, results appear every two cycles, starting in Cycle 11.

Note that in pipeline mode, operations are advanced by issuing load instructions (a load-driven pipeline). This means that additional load instructions are required to propagate the last instruction through the pipeline (draining the pipeline).

In pipeline systems, Lo is often tied to Vcc through a resistor to save microcode and only LAB and LMODE instructions are used. This causes the pipeline to advance automatically every two cycles, except when LMODE instructions are executed.

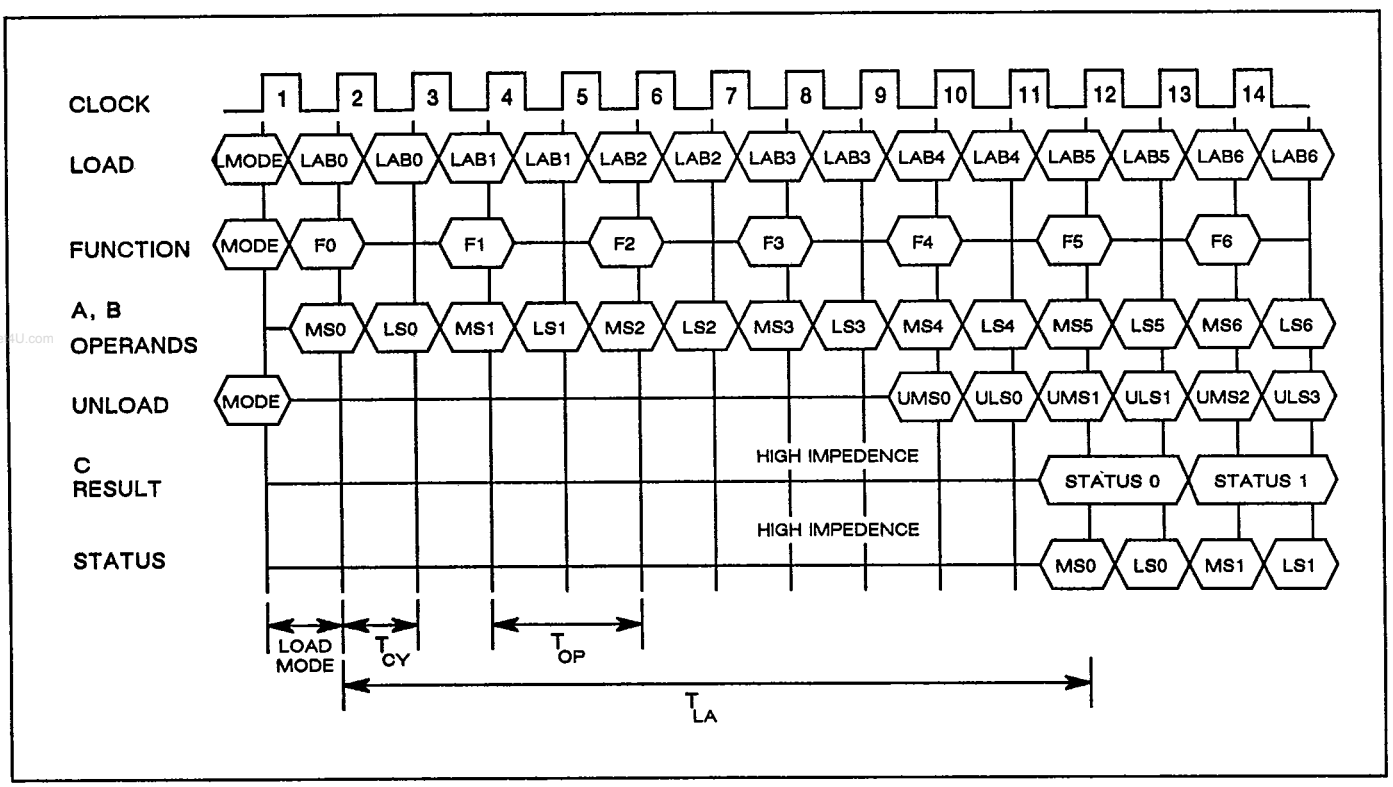


Figure 12. Pipeline Mode Timing Diagram

Affine Mode

Affine Infinity Mode is a mode where the sign of infinity is significant, implying that plus and minus infinity are not the same. The low power WTL 1232/1233 always operate in Affine Infinity Mode.

Rounding Modes

Rounding is used in digital systems because of limited register length. It is performed in Array Stage 3 of the floating point processors and is performed on the result of Array Stage 2 (the infinitely precise result) prior to determining exception cases, such as overflow or underflow.

The WTL 1232/1233 floating point processor chip set offers four rounding modes, which are selected by mode register bits M_{2-1} . The decoding of mode bits M_{2-1} is shown in the Mode Instruction Table and a comparision of rounding modes is shown below.

Functional Description, continued

ROUNDING MODE COMPARISION TABLE								
Exact Value	Rounded Value (3 digits)				Rounding Error (fraction of LSB)			
	RN	RP	RM	RZ	RN	RP	RM	RZ
9.5555	9.56	9.56	9.55	9.55	.45	.45	-.55	-.55
9.8950	9.90	9.90	9.89	9.89	.50	.50	-.50	-.50
9.8850	9.88	9.90	9.88	9.88	-.50	.50	-.50	-.50
-5.4321	-5.43	-5.43	-5.44	-5.43	.21	.21	-.79	.21
-5.4350	-5.44	-5.43	-5.44	-5.43	-.50	.50	-.50	.50

Round to Nearest (RN) rounds the result to a value nearest the infinitely precise result. If the two nearest values are equal, RN selects the value with an LSB equal to 0. Round to Nearest is often chosen for floating point operations because it provides the least amount of maximum rounding error.

Round to Zero (RZ) rounds the result toward 0. Positive values are rounded to a value less than or equal to the infinitely precise result; negative values are rounded to a value greater than or equal to the infinitely precise result. RZ must be used when converting floating point numbers to integers (FIX functions, as described in FUNCTION CONTROLS). In RZ mode, overflow results default to the maximum representable number less than infinity. This makes RZ mode the preferred mode in systems requiring saturation arithmetic; overflow results stick at the maximum value.

Round to Plus or Minus Infinity (RP and RM) modes allow limits to be placed around the infinitely precise result. RP rounds the result toward positive infinity; the rounded result is larger than or equal to the infinitely precise result. RM rounds the result toward negative infinity; the rounded result is less than or equal to the infinitely precise result. This makes RP and RM modes useful in interval arithmetic implementations where an algorithm is run first with RP set and then with RM set to determine limits on each side of the infinitely precise result. For digital signal processing applications such as recursive filters, RP or RM modes can help determine system sensitivity to rounding errors.

Status Outputs

The Status Output Table contains decoding for the six flags clocked into the S Register and report the status of floating point operations. For all operations except compare, status flags indicate when an operation is invalid ($\infty \times 0$, for example) or when an operation has produced an overflow, underflow, non-numerical result (Not-a-Number, or NAN), or an inexact result. Information in the Status Register is valid at the same time as the operation being unloaded.

STATUS OUTPUT TABLE		
S_2 S_1 S_0	MNEMONIC	EXCEPTIONS
0 0 0	-	No exceptions
0 0 1	INX	Inexact result
0 1 0	UNF	Exponent underflow
0 1 1	UNF + INX	Exponent underflow and inexact result
1 0 0	-	
1 0 1	OVF + INX	Exponent overflow and inexact result
1 1 0	INV	Invalid operand or operation
1 1 1	DIN	Denormalized operand (WTL 1232 only)

Status Outputs, continued

INX is set when a rounding error occurs. In general, an inexact exception is generated if any of the discarded significand bits are equal to one.

UNF or UNF+INX occur when a multiply result is smaller than the smallest normalized number (2^{-126}). In IEEE mode, the result output is a UNRM which is converted to a DNRM with an UNWRAP instruction. At the conclusion of the UNWRAP instruction, the status outputs correctly indicate exception conditions. In "FAST" mode, the result is set to 0 and no further processing is required. Underflow in "FAST" mode can produce UNF or UNF+INX, however, the result is always inexact. UNF+INX occurs when an ALU operation result underflows the destination format. The ALU produces 0 or a denormalized number as the result of an underflow.

OVF+INX is set when an operation overflows the destination format. The result is either INF or MAX.NRM (maximum normalized number) depending on the rounding mode as shown below.

OVERFLOW OUTPUT TABLE

ROUNDING MODE	RESULT SIGN	RESULT FORMAT (HEX)	
Round to Nearest (RN)	+	7F800000	(+ INF)
Round to Nearest (RN)	–	FF800000	(– INF)
Round to Zero (RZ)	+	7F7FFFFF	(+ MAX.NRM)
Round to Zero (RZ)	–	FF7FFFFF	(– MAX.NRM)
Round to Positive Infinity (RP)	+	7F800000	(+ INF)
Round to Positive Infinity (RP)	–	FF7FFFFF	(– MAX.NRM)
Round to Minus Infinity (RM)	+	7F7FFFFF	(+ MAX.NRM)
Round to Minus Infinity (RM)	–	FF800000	(– INF)

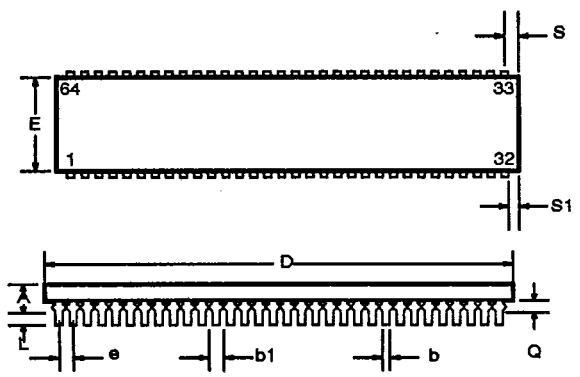
INV is set when an operation is performed with invalid data (for example, $0/\infty$). A NaN is returned as the result of an invalid operation.

The DIN status flag is set by the multiplier if a denormalized number is detected during IEEE mode operation. The denormalized operand is then normalized with a WRAP instruction before proceeding with the multiply. The result of an operation with DIN status is a zero.

July 1986

Physical Dimensions

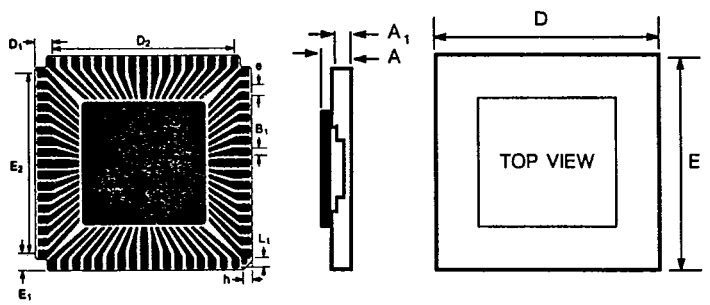
64-PIN DUAL IN-LINE PACKAGE



Symbol	LIMITS INCHES		MM	
	MIN	MAX	MIN	MAX
A	.135	.250	3.43	6.35
b	.015	.022	0.38	0.56
b1	.030	.060	0.76	1.52
c	.008	.013	0.20	0.33
D	3.140	3.260	79.76	82.80
E	.775	.825	19.69	20.96
E1	.880	.920	22.35	23.37
e	.090	.110	2.29	2.79
L	.120	.160	3.05	4.06
Q	.040	.100	1.02	2.54
α	0°	15°	0°	15°
S*		.098		2.49
S1**	.005		.127	

* From centerline of end lead
** From edge of end lead

68-PIN LEADLESS CHIP CARRIER (Type A)

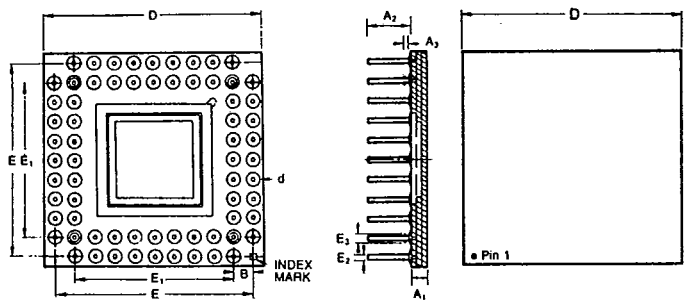


Use 3M Textool socket # 268-5400 with flat plate lid #268-5400-00

Symbol	LIMITS INCHES		MM	
	MIN	MAX	MIN	MAX
A	.082	.120	2.08	3.05
A1	.054	.065	1.37	1.65
B1	.033	.040	0.84	1.0
D	.938	.962	23.83	24.43
D1	.075 REF		1.91 REF	
D2	.800 REF		20.32 REF	
D4	–	.578	–	14.68
E	.938	.962	23.83	24.43
E1	.075 REF		1.91 REF	
E2	.800 REF		20.32 REF	
E4	–	.578	–	14.68
e	.050 BSC		1.27 BSC	
h	.035	.058	0.89	1.47
L1	.045	.055	1.14	1.40

Physical Dimensions, continued

68-PIN PIN GRID ARRAY



BOTTOM VIEW SIDE VIEW TOP VIEW

Use 3M Textool socket # 268-5400 with flat plate lid #68-5400-00

Symbol	Measurements	
	Inches	mm
A_1	.1375 ± 0.017	3.49 ± .43
A_2	0.160 ± 0.008	4.06 ± .20
A_3	0.050	1.27
D	1.100 ± 0.012 sq	27.94 ± .30
E	1.000 ± 0.012 sq	25.4 ± .30
E_1	0.800 ± 0.012 sq	20.32 ± .30
E_2	0.018	.46 typ
E_3	0.050 dia. typ	1.27 dia. typ

* From centerline of end lead
** From edge of end lead

Ordering Information

PACKAGE TYPE	TEMPERATURE RANGE	ORDER NUMBER
Hermetic DIP	T = 0 to +70°C	WTL 1232-XX-JC/1233-XX-JC
Hermetic DIP	T = -55 to +125°C	WTL 1232-YY-JM/1233-YY-JM
Hermetic DIP, Extended Temp.	T = -55 to +125°C	WTL 1232-YY-JE/1233-YY-JE
Leadless chip carrier, Type A	T = 0 to +70°C	WTL 1232-XX-LCA/1233-XX-LCA
Leadless chip carrier, Type A	T = -55 to +125°C	WTL 1232-YY-LMA/1233-YY-LMA
Leadless chip carrier, Type C	T = 0 to +70°C	WTL 1232-XX-LCC/1233-XX-LCC
Leadless chip carrier, Type C	T = -55 to +125°C	WTL 1232-YY-LMC/1233-YY-LMC
Pin Grid Array	T = 0 to +70°C	WTL 1232-XX-GCU/1233-XX-GCU
Pin Grid Array	T = -55 to +125°C	WTL 1232-YY-GMU/1233-YY-GMU

NOTE: XX = 100, 60, 50
YY = 100, 60

For flatpack contact headquarters in Sunnyvale