Series W

Surface Mount Clock Oscillator

- **High frequency range**
- **Tight stability available**

RoHS COMPLIANT 2002 / 95 / EC

Part Numbering Example: WU33AQ - XX.XXXX M

W	U	33	A	Q		XX.XXXXM
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	SYMMETRY	OPERATING TEMP.	STABILITY	FREQUENCY
W	Blank=Cmos T = TTL	O = Full Size OH = Half Size U = 5X7 G = 3.2X5	18= 1.8V 25= 2.5V 33= 3.3V 50= 5.0V	Blank=40/60% A=45/55%	N= -55 °C +105°C Q= -55 °C +125°C (MIL-STD-883B) M= -55 °C +125°C (MIL-PRF-55310D)	Blank = ±50ppm 2 = ±25ppm 3 = ±20ppm	0.50 ~200.000 MHz

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	0.5		133.000	MHz
Available Stability Options:	-50		50	ppm
	-25		25	ppm
	-20		20	ppm
Programmable Supply Voltage:				
(1–133 MHz)	4.5	5.0	5.5	V
(1–100 MHz)	3.0	3.3	3.6	V
Operating Temperature	-40		+85	
Range Options:	-55		+105	°C
	-55		+125	
Storage Temperature:	-55			
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V			±3	ppm
Programmable Output Level:	TTL/Cmos			

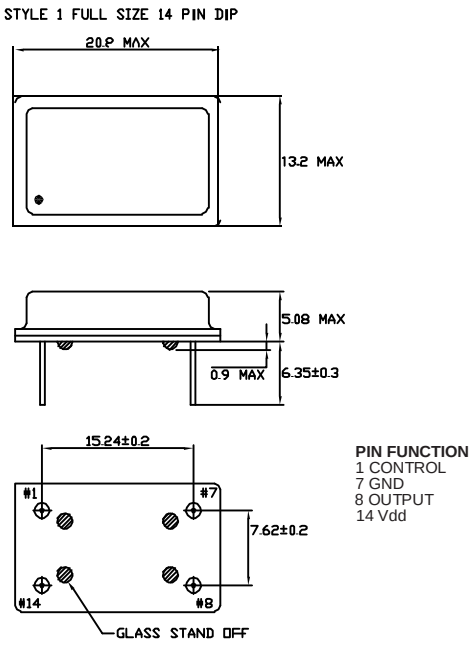
Operating Conditions:

	Description			Unit
Vdd	Supply Voltage	3.0	5.5	V
C_{TTL}	Max Capacitive Load on outputs for TTL levels			
	4.5V–5.5V Vdd ≤ 40 MHz		50	pF
	4.5V–5.5V Vdd > 40–133 MHz		25	pF
C_{CMOS}	Max Capacitive Load on outputs for CMOS levels			
	4.5V–5.5V Vdd, ≤ 66 MHz		50	pF
	4.5V–5.5V Vdd, >66–200MHz		25	pF
	2.25V–3.6V Vdd, ≤ 40 MHz		30	pF
	2.25V–3.6V Vdd, >40–200MHz		15	pF
	1.62V–1.89V Vdd, ≤ 40 MHz		25	pF
	1.62V–1.98V Vdd, >40–200MHz		15	pF

Environmental And Mechanical	
Mechanical Shock	Per MIL-STD-883 ,Method 2002 ,Cond.B
Thermal Shock	Per MIL-STD-883 ,Method 1011 ,Cond.A
Vibration	Per MIL-STD-883 ,Method 2007 ,Cond.A
Seal	Per MIL-STD-883, Method 1014, Condition B & C
Solderability	Per MIL-STD-883 ,Method 2003 ,Cond.A

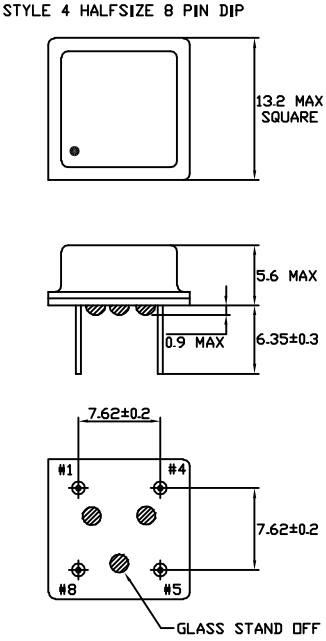
Surface Mount Clock Oscillator

Style O Full Size 14 Pin Dip



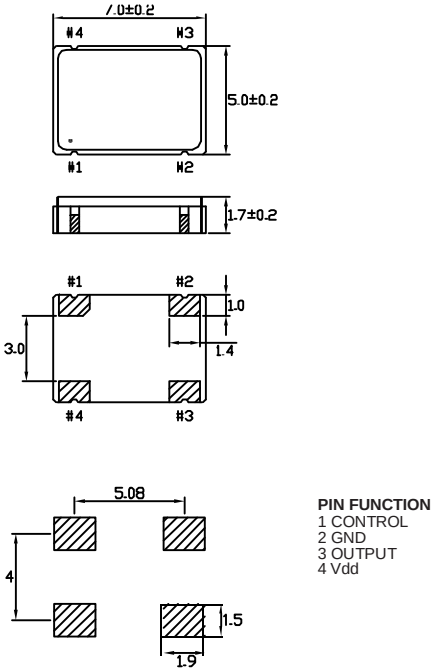
PIN FUNCTION
1 CONTROL
7 GND
8 OUTPUT
14 Vdd

Style OH Half Size 8 Pin Dip



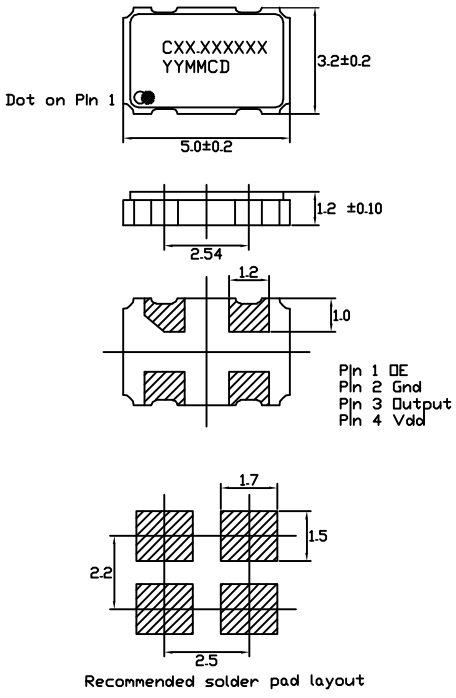
PIN FUNCTION
1 CONTROL
4 GND
5 OUTPUT
8 Vdd

Style U 5x7 Ceramic SMD



PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Style G 3.2x5 Ceramic SMD



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Series W

Electrical Characteristics

Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V_{IL}, Low–Level Input Voltage	4.5–5.5V Vdd			0.8	V
TO DISABLE OUTPUT	1.62–3.6V Vdd			0.2Vdd	V
V_{IH}, High–Level Input Voltage	4.5–5.5V Vdd	2.0			V
TO ENABLE OUTPUT OPEN	1.62–3.6V Vdd	0.7VddV			
I_{IL}, Input Low Current	V_{IN} = 0V			10	µA
I_{IH}, Input High Current	V_{IN} =Vdd			5	µA
Output Characteristics:					
V_{OL}, Low–Level Output Voltage	4.5V–5.5V Vdd, 16 mA I_{OL}			0.4	V
	1.62V–3.6V Vdd, 8 mA b_L			0.4	V
V_{OHTTL}, High-level Output Voltage TTL	4.5V–5.5V Vdd, -16 mA I_{OL}	2.4			V
V_{OHCMOS},	4.5V–5.5V Vdd, -16 mA I_{OL}	Vdd-0.4			V
High-level CMOS Voltage	1.62V–3.6V Vdd, -8 mA b_L	Vdd-0.4			V
Power Supply Current:	4.5–5.5 Vdd, Output Freq ≤ 133 MHz			45	mA
(unloaded)	1.62–3.6 Vdd,Output Freq ≤ 200 MHz			25	mA
Standby Current:			10	50	µA
Pull-Up (Pin 1)	4.5–5.5 Vdd, V_{IN} = 0V	1.1	3.0	8.0	MΩ
	4.5–5.5 Vdd, V_{IN} = 0.7V	50	100	200	KΩ
Tri-State Leakage Current	5.0 Vdd		20		µA
Output Enable Mode:	Output is Tri-Stated				

Output Clock Switching Characteristics

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle:	≤ 50 MHz, C_L = 50 pF	45		55	%
TTL @ 1.4 V	50–66 MHz, C_L = 15 pF	45		55	%
4.5-5.5 Vdd	66–125 MHz, C_L = 25 pF	45		55	%
	125–200 MHz, C_L = 15 pF	45		55	%
Duty Cycle:	≤ 66 MHz, C_L ≤ 25 pF	45		55	%
CMOS @ Vdd/2	66–125 MHz, C_L ≤ 25 pF	45		55	%
4.5-5.5 Vdd	125–200 MHz, C_L ≤ 15 pF	45		55	%
1.62–3.6 Vdd	≤ 40 MHz, C_L ≤ 30 pF	45		55	%
	40-200 MHz, C_L ≤ 15 pF	45		55	%
Output Clock Rise/Fall	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 50			1.8	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 25			1.2	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C_L = 15			0.9	ns
	0.2–0.8Vdd, 4.5-5.5 Vdd, C_L = 50			3.4	ns
	0.2–0.8Vdd, 1.62–3.6 Vdd, C_L = 30			3.4	ns
	0.2–0.8Vdd, 1.62–3.6 Vdd, C_L = 15			2.4	ns
Start Up Time	From power on			2	ms
Output Disable Time					
Synchronous	OE pin LOW to output Hi-Z		T/2	T+10	ns
Asynchronous	T = Frequency oscillator period		10	15	ns
Output Enable Time				50	ns
RMS Period Jitter:			5	10	ps

* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.