

2GB – 2x128Mx72 SDRAM, REGISTERED

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- Dual Rank
- 168 Pin DIMM JEDEC
 - PCB - AD2: 28.58mm (1.125") TYP

DESCRIPTION

The WV3DG72256V is a 2x128Mx72 synchronous DRAM module which consists of eighteen 256Mx4 stack SDRAM components (stacked from 128Mx4) in TSOP II package, two 18 bit Drive ICs for input control signal and one 2Kb EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 pin DIMM multilayer FR4 Substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

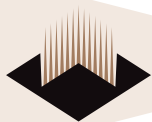
PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK
1	V _{SS}	29	DQM1	57	DQ18	85	V _{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	NC	59	V _{CC}	87	DQ33	115	RAS#	143	V _{CC}
4	DQ2	32	V _{SS}	60	DQ20	88	DQ34	116	V _{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V _{CC}	34	A2	62	*V _{REF}	90	V _{CC}	118	A3	146	*V _{REF}
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V _{SS}	92	DQ37	120	A7	148	V _{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V _{SS}	40	V _{CC}	68	V _{SS}	96	V _{SS}	124	V _{CC}	152	V _{SS}
13	DQ9	41	V _{CC}	69	DQ24	97	DQ41	125	NC	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V _{SS}	71	DQ26	99	DQ43	127	V _{SS}	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V _{CC}	101	DQ45	129	CS3#	157	V _{CC}
18	V _{CC}	46	DQM2	74	DQ28	102	V _{CC}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	CB0	49	V _{CC}	77	DQ31	105	CB4	133	V _{CC}	161	DQ63
22	CB1	50	NC	78	V _{SS}	106	CB5	134	NC	162	V _{SS}
23	V _{SS}	51	NC	79	NC	107	V _{SS}	135	NC	163	NC
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V _{CC}	54	V _{SS}	82	SDA	110	V _{CC}	138	V _{SS}	166	SA1
27	WE#	55	DQ16	83	SCL	111	CAS#	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	V _{CC}	112	DQM4	140	DQ49	168	V _{CC}

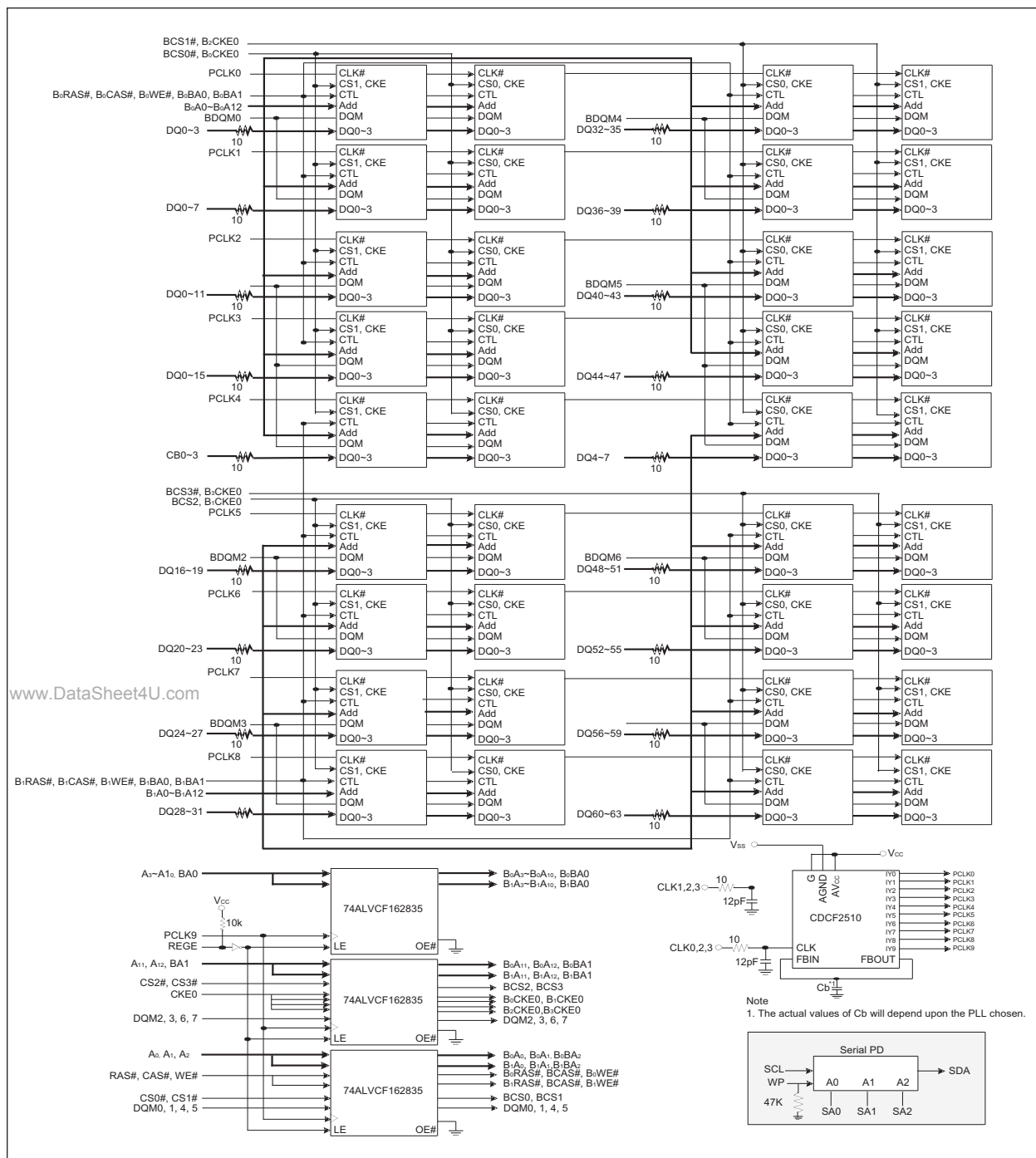
PIN NAMES

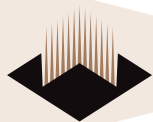
A0 – A12	Address Input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CB0-7	Check Bit (Data-In/Data-Out)
CLK0	Clock Input
CKE0	Clock Enable Input
CS0# - CS3#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V _{CC}	Power Supply (3.3V)
V _{SS}	Ground
V _{REF}	Power Supply for Reference
REGE	Register Enable
SDA	Serial Data I/O
SCL	Serial Clock
SA0-2	Address in EEPROM
NC	No Connect

* Pins not used in this module.



FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T _{STG}	-55 ~ +150	°C
Power Dissipation	P _D	36	W
Short Circuit Current	I _{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V _{CC}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	3.0	V _{CCQ} +0.3	V	1
Input Low Voltage	V _{IL}	-0.3	—	0.8	V	2
Output High Voltage	V _{OH}	2.4	—	—	V	I _{OH} = -2mA
Output Low Voltage	V _{OL}	—	—	0.4	V	I _{OL} = -2mA
Input Leakage Current	I _{LI}	-10	—	10	μA	3

Note: 1. V_{IH} (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{CCQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

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CAPACITANCE

T_A = 25 °C, f = 1MHz, V_{CC} = 3.3V, V_{REF} = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12, BA0-BA1)	C _{IN1}	15	pF
Input Capacitance (RAS#, CAS#, WE#)	C _{IN2}	15	pF
Input Capacitance (CKE0)	C _{IN3}	15	pF
Input Capacitance (CLK0)	C _{IN4}	20	pF
Input Capacitance (CS0# - CS3#)	C _{IN5}	15	pF
Input Capacitance (DQM0-DQM7)	C _{IN6}	15	pF
Data input/output capacitance (DQ0-DQ63), (CB0-BC7)	C _{OUT}	22	pF



OPERATING CURRENT CHARACTERISTICS

$V_{CC} = 3.3V$, $0^{\circ}C \leq T_A \leq 70^{\circ}C$

Parameters	Symbol	Conditions	Versions	Units	Note
			133/100		
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC(min)}$ $I_{OL} = 0mA$	2,520	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	$C_{KE} \leq V_{IL(max)}$, $t_{CC} = 10ns$	530	mA	
	I_{CC2PS}	$C_{KE} \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	130	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	$C_{KE} \geq V_{IH(min)}$, $CS \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are charged one time during 20	1,170	mA	
	I_{CC2NS}	$C_{KE} \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ Input signals are stable	410	mA	
Active standby current in power-down mode	I_{CC3P}	$C_{KE} \geq V_{IL(max)}$, $t_{CC} = 10ns$	670	mA	
	I_{CC3PS}	$C_{KE} \& CLK \leq V_{IL(max)}$, $t_{CC} = \infty$	270	mA	
Active standby in current non power- down mode	I_{CC3N}	$C_{KE} \geq V_{IH(min)}$, $CS \geq V_{IH(min)}$, $t_{CC} = 10ns$ Input signals are charged one time during 20ns	1,530	mA	
	I_{CC3NS}	$C_{KE} \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$, $t_{CC} = \infty$ input signals are stable	950	mA	
Operating current (Burst mode)	I_{CC4}	$I_O = mA$ Page burst 4 Banks activated $t_{CCD} = 2CLK$	2,610	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$	4,590	mA	2
Self refresh current	I_{CC6}	$C_{KE} \leq 0.2V$	420	mA	

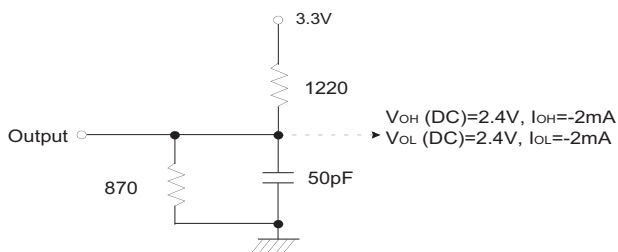
Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.



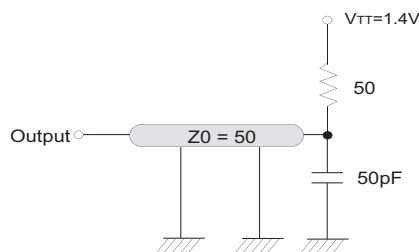
AC OPERATING TEST CONDITIONS

 $V_{CC} = 3.3V, 0^{\circ}C \leq T_A \leq 70^{\circ}C$

Parameter	Value	Units
AC Input level (V_{IN}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

AC OPERATING TEST CONDITIONS

Parameter	Symbol	Value	Units	Notes
		133/100		
Row active to row active delay	$t_{RRD}(\text{MIN})$	15	ns	1
RAS# to CAS# delay	$t_{RCD}(\text{MIN})$	20	ns	1
Row Precharge time	$t_{RP}(\text{MIN})$	20	ns	1
Row active time	$t_{RAS}(\text{MIN})$	45	ns	1
	$t_{RAS}(\text{MAX})$	100	μs	
Row cycle time	$t_{RC}(\text{MIN})$	65	ns	1
Last data in to row precharge	$t_{RDL}(\text{MIN})$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\text{MIN})$	$2 \text{ CLK} + t_{RP}$	—	
Last data in to new col. address delay	$t_{CDL}(\text{MIN})$	1	CLK	1
Last data in to burst stop	$t_{BDL}(\text{MIN})$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\text{MIN})$	1	CLK	2
Number of valid output data	CAS Latency = 3	2	CLK	3
	Cas Latency = 2	1	ea	4

Notes: 1. The minimum number of clock cycles is determined by driving the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.



OPERATING AC PARAMETER

Parameter		Symbol	133/100		Units	Notes
			Min	Max		
CLK cycle time	CAS latency = 3	t _{CC}	7.5	1,000	ns	1
	CAS latency = 2		–			
CLK to valid output delay	CAS latency = 3	t _{SAC}		5.4	ns	1, 2
	CAS latency = 2			–		
Output data hold time	CAS latency = 3	t _{OH}	3		ns	2
	CAS latency = 2		–			
CLK high pulse width		t _{CH}	2.5		ns	3
CLK low pulse width		t _{CL}	2.5		ns	3
Input setup time		t _{SS}	1.5		ns	3
Input hold time		t _{SH}	0.8		ns	3
CLK to output in Low-z		t _{SLZ}	1		ns	2
CLK to output in Hi-z	CAS latency = 3	t _{HZ}		5.4	ns	
	CAS latency = 2			–		

Notes: 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, $(t_r/2-0.5)$ ns should be added to the parameter.

3. Assumed input rise and fall time (t_r & t_f) = 1ns. If t_r & t_f is longer than 1ns, transient time compensation should be considered, i.e., $[(t_r = t_f)/2-1]$ ns should be added to the parameter.



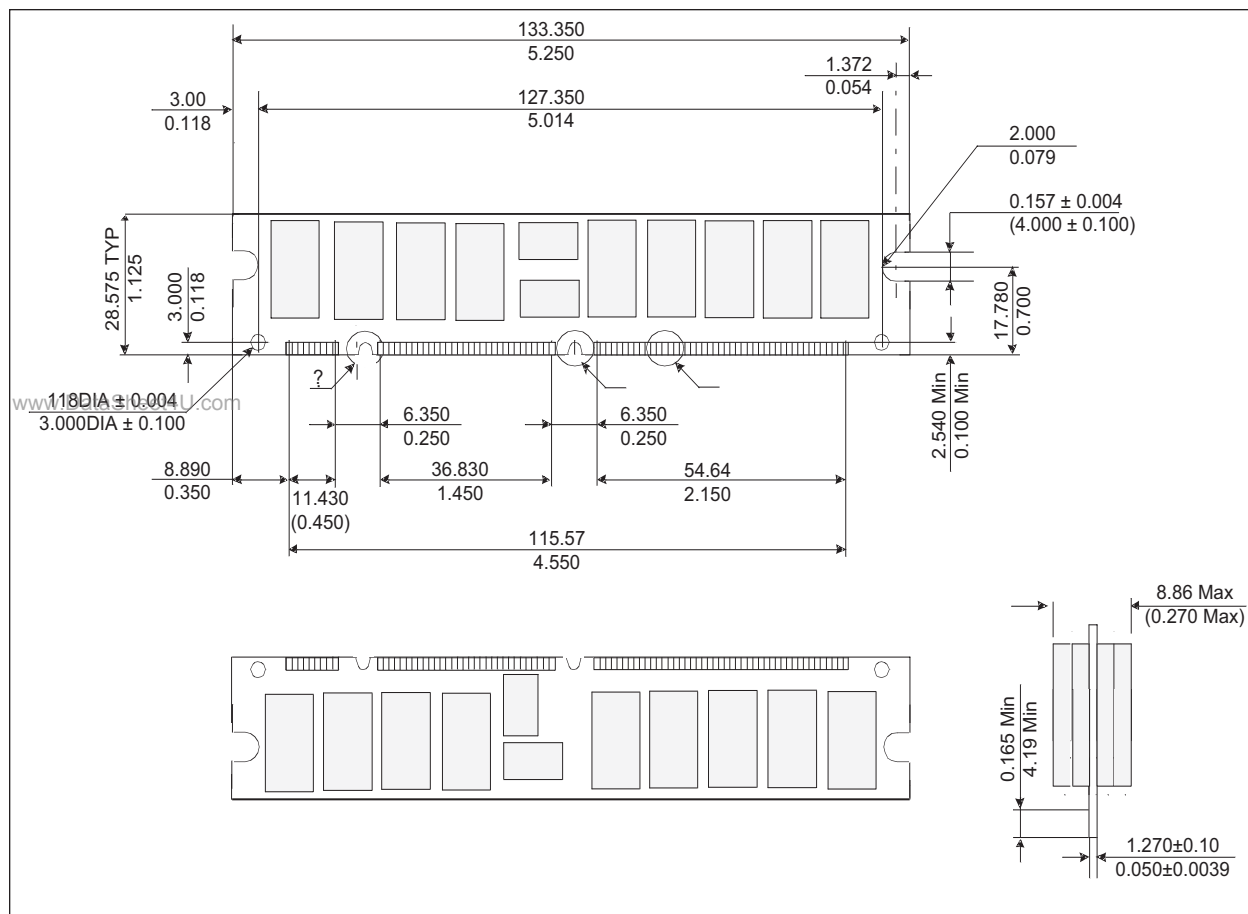
ORDERING INFORMATION FOR AD2

Part Number	Clock Speed	CAS Latency	Height*
WV3DG72256V10AD2xx	100MHz	CL=2	28.58 (1.25") TYP
WV3DG72256V7AD2xx	133MHz	CL=2	28.58 (1.25") TYP
WV3DG72256V75AD2xx	133MHz	CL=3	28.58 (1.25") TYP

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

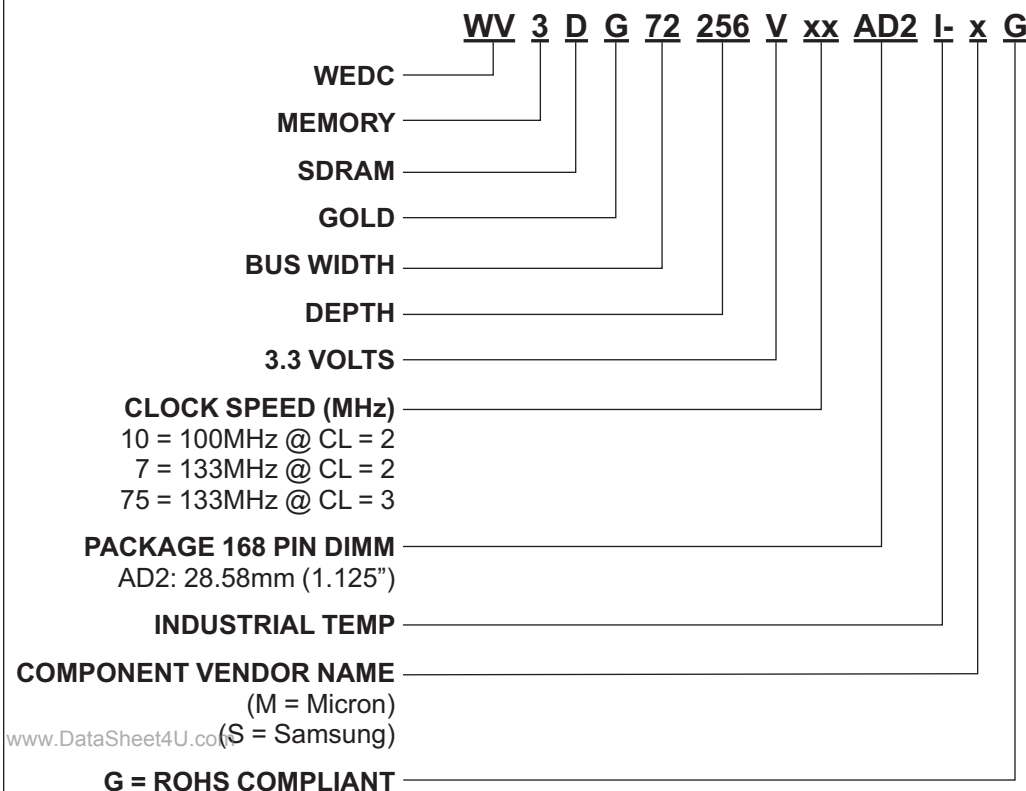
PACKAGE DIMENSIONS FOR AD2



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 0	Created Data sheet	January 2006	Advanced

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