256MB – 32Mx64 DDR SDRAM UNBUFFERED

FEATURES

- Double-data-rate architecture
- PC2700 @ CL 2.5
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect with EEPROM
- Power supply:
  - V_{CC} = V_{CCQ} = +2.5V ±0.2V
- 184 pin DIMM package
  - D3 PCB height: 28.58mm (1.125")

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The WV3EG32M64ETSU is a 32Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM components. The module consists of eight 32Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR333 @CL=2.5
Clock Speed	166MHz
CL-t_{RCD}-t_{RP}	2.5-3-3

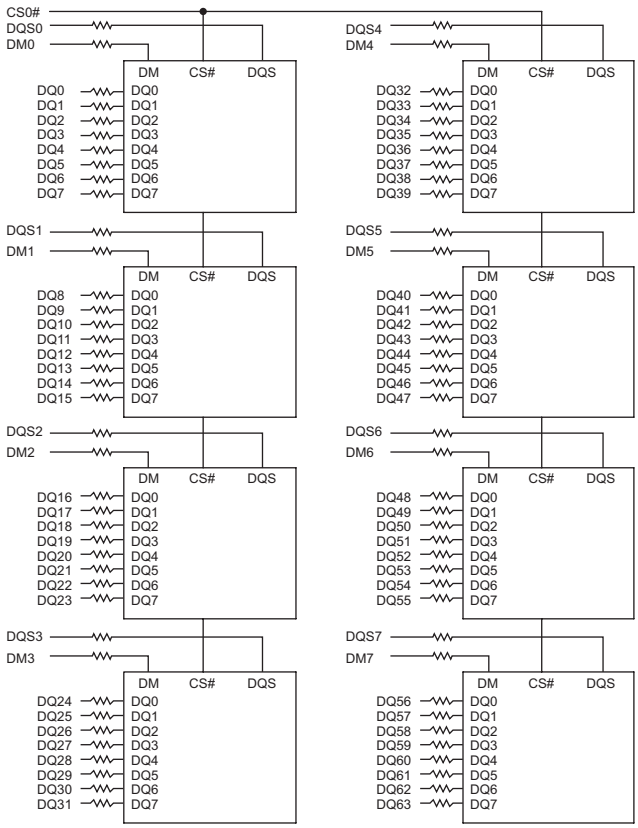
PIN CONFIGURATION

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	47	NC	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	NC
3	V_{SS}	49	NC	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	NC
5	DQS0	51	NC	97	DM0	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	NC
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DM4
12	DQ8	58	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DM1	153	DQ44
16	CK1	62	V_{CCQ}	108	V_{CC}	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	CAS#	111	NC	157	CS0#
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	V_{CCQ}	76	CK2	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DM6
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	NC	180	V_{CCQ}
43	A1	89	V_{SS}	135	NC	181	SA0
44	NC	90	NC	136	V_{CCQ}	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	CK0#	184	V_{CCSPD}

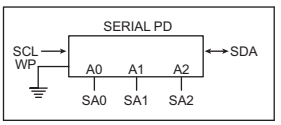
PIN NAMES

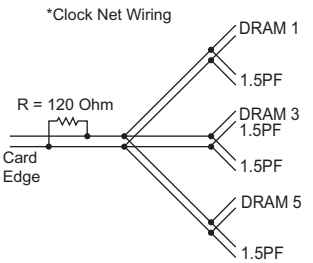
A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#, CK1#, CK2#	Clock Input
CKE0	Clock Enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-in-mask
V_{CC}	Power Supply
V_{CCQ}	Power Supply for DQS
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V_{CCID}	V_{CC} Indentification Flag
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM

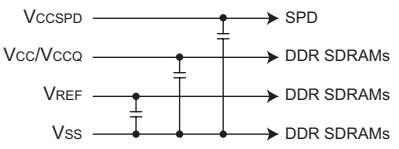


RAS# → RAS#: DDR SDRAMs
CAS# → CAS#: DDR SDRAMs
BA0-BA1 → BA0-BA1: DDR SDRAMs
WE# → WE#: DDR SDRAMs
A0-A12 → A0-A12: DDR SDRAMs
CKE0 → CKE0: DDR SDRAMs





CLOCK INPUT	
CK0, CK0#	2 SDRAMS
CK1, CK1#	3 SDRAMS
CK2, CK2#	3 SDRAMS



NOTE: All datalines are terminated through a 22 ohm series resistor.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to 3.6	V
Voltage on V_{CCQ} supply relative to V_{SS}	V_{CCQ}	-0.5 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	8	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS

$0°C \leq T_A \leq 70°C$, $V_{CC} = V_{CCQ} = 2.5V \pm 0.2V$

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal V_{CC} of 2.5V)	V_{CC}	2.3	2.7		
I/O Supply voltage	V_{CCQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	V_{CCQ}/2 -50mV	V_{CCQ}/2 +50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF} -0.04	V_{REF} +0.04	V	2
Input logic high voltage	$V_{IH(DC)}$	V_{REF} +0.15	V_{CCQ} +0.3	V	4
Input logic low voltage	$V_{IL(DC)}$	-0.3	V_{REF} -0.15	V	4
Input Voltage Level, CK and CK# inputs	$V_{IN(DC)}$	-0.3	V_{CCQ} +0.3	V	
Input Differential Voltage, CK and CK# inputs	$V_{ID(DC)}$	0.36	V_{CCQ} +0.6	V	3
Input crossing point voltage, CK and CK# inputs	$V_{IX(DC)}$	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current (Normal strengh driver); $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-16.8		mA	
Output High Current (Normal strengh driver); $V_{OUT} = V_{TT} + 0.84V$	I_{OL}	16.8		mA	
Output High Current (Half strengh driver); $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-9		mA	
Output High Current (Half strengh driver); $V_{OUT} = V_{TT} + 0.84V$	I_{OL}	9		mA	

Notes:
1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of 3nH.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*V_{CCQ} of the transmitting device and must track variations in the DC level of the same.

CAPACITANCE

$T_A = 25°C$, f = 1MHz, $V_{CC} = V_{CCQ} = 2.5V$

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#)	C_{IN1}	49	57	pF
Input Capacitance (CKE0)	C_{IN2}	42	50	pF
Input Capacitance (CS0#)	C_{IN3}	42	50	pF
Input Capacitance (CLK0, CLK1, CLK2)	C_{IN4}	25	30	pF
Input Capacitance (DM0-DM7)	C_{IN5}	6	7	pF
Data and DQS input/output capacitance (DQ0-DQ63)	C_{OUT1}	6	7	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

$0°C \leq T_A \leq 70°C$, $V_{CC} = V_{CCQ} = 2.5V \pm 0.2V$
Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR333@ CL = 2.5	Units
Operating one bank active-precharge current;	I_{DD0}	$t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS}min(I_{DD})$; CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	720	mA
Operating one bank active-read-precharge current;	I_{DD1}	I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS}min(I_{DD})$, $t_{RCD} = t_{RCD}(I_{DD})$; CKE is HIGH, CS is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as I_{DD4W}	920	mA
Precharge power-down current;	I_{DD2P}	All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	24	mA
Precharge quiet standby current;	I_{DD2Q}	All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING	160	mA
Precharge standby current;	I_{DD2F}	All banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	200	mA
Active power-down current;	I_{DD3P}	All banks open; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	280	mA
Active standby current;	I_{DD3N}	All banks open; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS}max(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS - is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	440	mA
Operating burst write current;	I_{DD4W}	All banks open, Continuous burst writes; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS}$-max(I_{DD}), $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1280	mA
Operating burst read current;	I_{DD4R}	All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS}max(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{DD4W}	1280	mA
Burst auto refresh current;	I_{DD5}	$t_{CK} = t_{CK}(I_{DD})$; Refresh command at every $t_{RFC}(I_{DD})$ interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1360	mA
Self refresh current;	I_{DD6}	CK and CK at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	24	mA
Operating bank interleave read current;	I_{DD7}	All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = $t_{RCD}(I_{DD})$-1*$t_{CK}(I_{DD})$; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RRD} = t_{RRD}(I_{DD})$, t_{RCD} = 1*$t_{CK}(I_{DD})$; CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I_{DD4R}; Refer to the following page for detailed timing conditions	2240	mA

Note: These specifications apply to modules built with Samsung components only.

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA
4. Timing Patterns :
   - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Parameter	Symbol	335		Unit	Note
		Min	Max		
Row cycle time	t_{RC}	60		ns	
Refresh row cycle time	t_{RFC}	72		ns	
Row active time	t_{RAS}	42	70K	ns	
RAS to CAS delay	t_{RCD}	18		ns	
Row precharge time	t_{RP}	18		ns	
Row active to Row active delay	t_{RRD}	12		ns	
Write recovery time	t_{WR}	15		ns	
Last data into Read command	t_{WTR}	1		t_{CK}	
Col. address to Col. address delay	t_{CCD}	1		t_{CK}	
Clock cycle time	t_{CK}	6	12	ns	
Clock high level width	t_{CH}	0.45	0.55	t_{CK}	
Clock low level width	t_{CL}	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK	t_{DQSCK}	-0.6	+0.6	ns	
Output data access time from CK/CK	t_{AC}	-0.7	+0.7	ns	
Data strobe edge to ouput data edge	t_{DQSQ}	—	0.45	ns	12
Read Preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read Postamble	t_{RPST}	0.4	0.6	t_{CK}	
CK to valid DQS-in	t_{DQSS}	0.75	1.25	t_{CK}	
DQS-in setup time	t_{WPRES}	0		ns	3
DQS-in hold time	t_{WPRE}	0.25		t_{CK}	
DQS falling edge to CK rising-setup time	t_{DSS}	0.2		t_{CK}	
DQS falling edge from CK rising-hold time	t_{DSH}	0.2		t_{CK}	
DQS-in high level width	t_{DQSH}	0.35		t_{CK}	
DQS-in low level width	t_{DQSL}	0.35		t_{CK}	
DQS-in cycle time	t_{DSC}	0.9	1.1	t_{CK}	
Address and Control Input setup time(fast)	t_{IS}	0.75		ns	5.7~9
Address and Control Input hold time(fast)	t_{IH}	0.75		ns	5.7~9
Address and Control Input setup time(slow)	t_{IS}	0.8		ns	6~9
Address and Control Input hold time(slow)	t_{IH}	0.8		ns	6~9
Data-out high impedence time from CK/CK	t_{HZ}		+0.7	ns	1
Data-out low impedence time from CK/CK	t_{LZ}	-0.7	+0.7	ns	1
Output Slew Rate Matching Ratio(rise to fall)	t_{SLMR}	0.67	1.5		

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

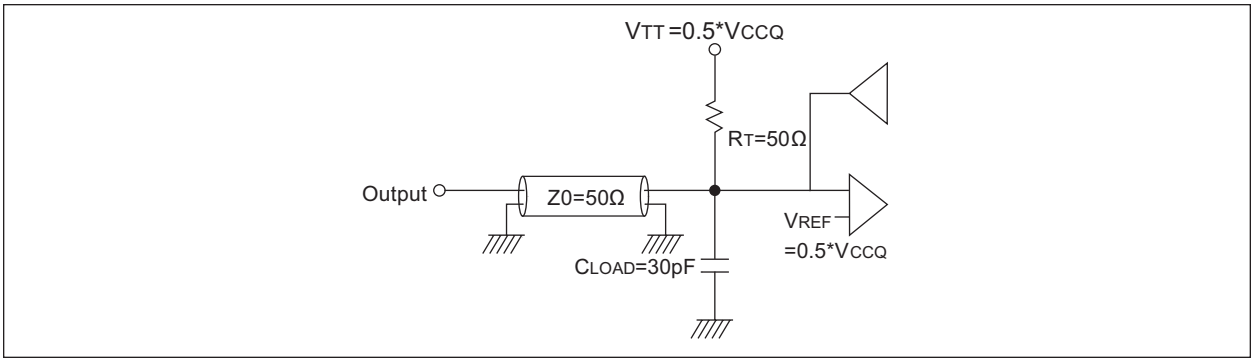
Parameter	Symbol	B3		Unit	Note
		Min	Max		
Mode register set cycle time	t_{MRD}	12		ns	
DQ & DM setup time to DQS	t_{DS}	0.45		ns	
DQ & DM hold time to DQS	t_{DH}	0.45		ns	
Control & Address input pulse width	t_{IPW}	2.2		ns	8
DQ & DM input pulse width	t_{DIPW}	1.75		ns	8
Power down exit time	t_{PDEX}	6		ns	
Exit self refresh to non-Read command	t_{XSNR}	75		ns	
Exit self refresh to read command	t_{XSRD}	200		t_{CK}	
Refresh interval time	t_{REFI}		7.8	us	4
Output DQS valid window	t_{QH}	t_{HP}-t_{QHS}	—	ns	11
Clock half period	t_{HP}	t_{CLmin} or t_{CHmin}	—	ns	10, 11
Data hold skew factor	t_{QHS}		0.55	ns	11
DQS write postamble time	t_{WPST}	0.4	0.6	t_{CK}	2
Active to Read with Auto precharge command	t_{RAP}	18			
Autoprecharge write recovery + Precharge time	t_{DAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}	13

AC OPERATING TEST CONDITIONS

V_{CC} = 2.5V, V_{CCQ} = 2.5V, 0°C ≤ T_A ≤ 70°C

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V_{CCQ}	V	
Input signal maximum peak swing	1.5	V	
Input Levels (V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}-0.31	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{TT}	V	
Output load condition	See Load Circuit		

OUTPUT LOAD CIRCUIT (SSTL_2)



Component Notes

1. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).
2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
5. For command/address input slew rate: 1.0 V/ns
6. For command/address input slew rate: 0.5 V/ns and 1.0 V/ns
7. For CK & CK# slew rate 1.0 V/ns
8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
9. Slew Rate is measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.
10. Min (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).....For example, t_{CL} and t_{CH} are = 50% of the period, less the half period jitter ($t_{JIT(HP)}$) of the clock source, and less the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) into the clock traces.
11. $t_{QH} = t_{HP} - t_{QHS}$, where:
t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CH}, t_{CL}). t_{QHS} accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and pchannel to n-channel variation of the output drivers.
12. t_{DQSQ}
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
13. $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and t_{CK}=7.5ns t_{DAL} = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3) t_{DAL} = 5 clocks

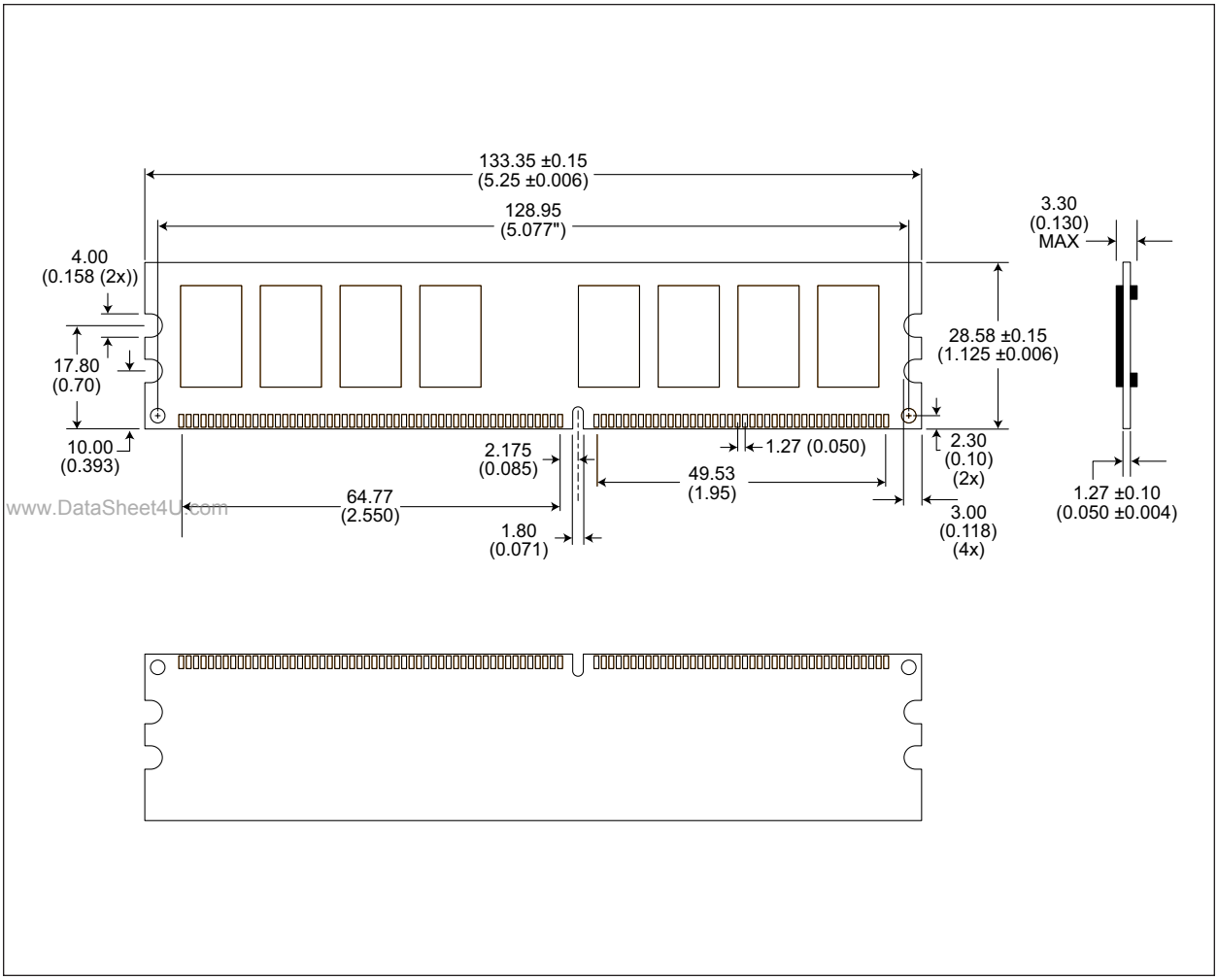
ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*	Temperature
WV3EG32M64ETSU335D3xG	166MHz/333Mb/s	2.5	3	3	28.58 (1.125")	0°C to 70°C

NOTES:

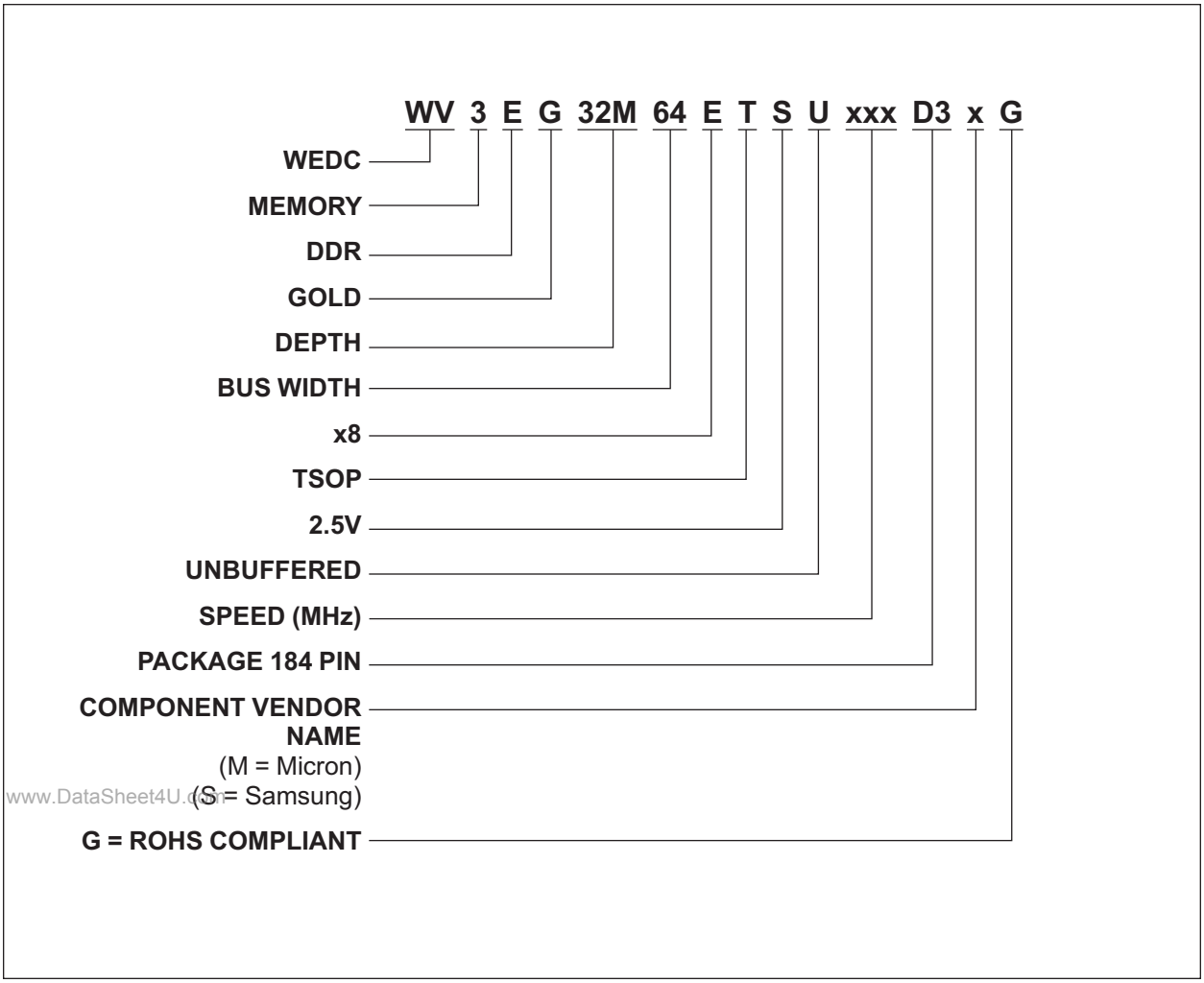
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

256MB – 32Mx64 DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	7-05	Advanced