



512MB – 64Mx64 DDR SDRAM UNBUFFERED

FEATURES

- Double-data-rate architecture
- PC2700 @ CL 2.5
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect with EEPROM
- Power supply:
 - $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$
- 184 pin DIMM package
 - D3 PCB height: 28.58mm (1.125")

DESCRIPTION

The WV3EG64M64ETSU is a 64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eight 64Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

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OPERATING FREQUENCIES

	DDR333 @CL=2.5
Clock Speed	166MHz
CL-t _{RCD} -t _{RP}	2.5-3-3



PIN CONFIGURATION

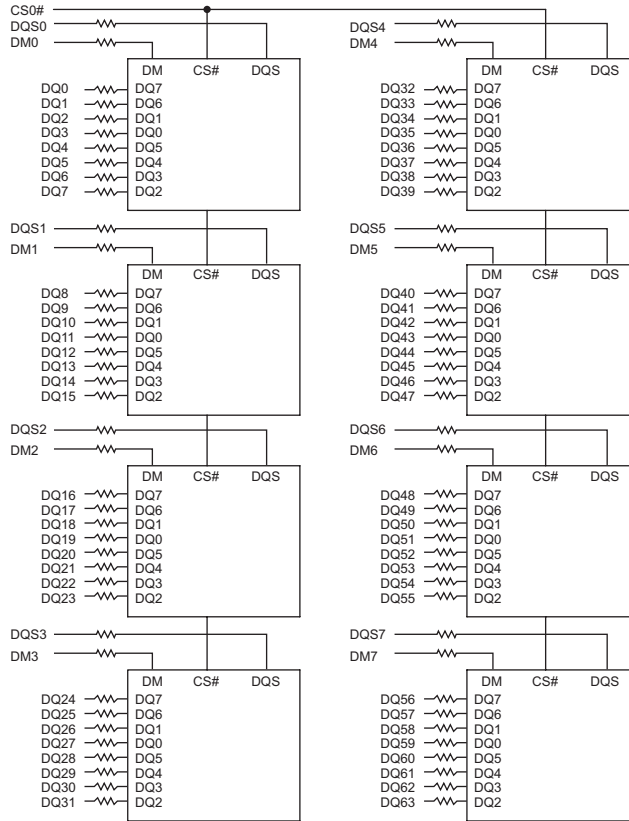
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	47	NC	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	NC
3	Vss	49	NC	95	DQ5	141	A10
4	DQ1	50	Vss	96	Vccq	142	NC
5	DQS0	51	NC	97	DM0	143	Vccq
6	DQ2	52	BA1	98	DQ6	144	NC
7	Vcc	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	Vccq	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	Vcc
11	Vss	57	DQ34	103	NC	149	DM4
12	DQ8	58	Vss	104	Vccq	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	Vccq	61	DQ40	107	DM1	153	DQ44
16	CK1	62	Vccq	108	Vcc	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	Vccq
19	DQ10	65	CAS#	111	NC	157	CS0#
20	DQ11	66	Vss	112	Vccq	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5
22	Vccq	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	Vcc	116	Vss	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	Vss	72	DQ48	118	A11	164	Vccq
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	Vss	120	Vcc	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	Vccq	76	CK2	122	A8	168	Vcc
31	DQ19	77	Vccq	123	DQ23	169	DM6
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	Vccq
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vccid	128	Vccq	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	Vcc	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vcc	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	NC	180	Vccq
43	A1	89	Vss	135	NC	181	SA0
44	NC	90	NC	136	Vccq	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	Vcc	92	SCL	138	CK0#	184	Vccspd

PIN NAMES

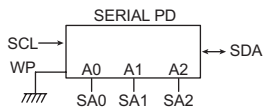
A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#, CK1#, CK2#	Clock Input
CKE0	Clock Enable input
CS0#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-in-mask
Vcc	Power Supply
Vccq	Power Supply for DQS
Vss	Ground
VREF	Power Supply for Reference
Vccspd	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
Vccid	Vcc Identification Flag
NC	No Connect



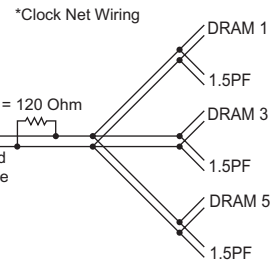
FUNCTIONAL BLOCK DIAGRAM



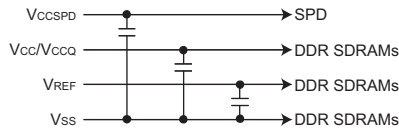
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Clock Wiring	
Clock Input	DDR SDRAMs
CK0, CK0#	2 DDR SDRAMs
CK1, CK1#	3 DDR SDRAMs
CK2, CK2#	3 DDR SDRAMs



- BA0-BA1 → BA0-BA1: DDR SDRAMs
- A0-A12 → A0-A12: DDR SDRAMs
- RAS# → RAS#: DDR SDRAMs
- CAS# → CAS#: DDR SDRAMs
- CKE0 → CKE: DDR SDRAMs
- WE# → WE#: DDR SDRAMs



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS# relationships must be maintained as shown.

NOTE: All datalines are terminated through a 22 ohm series resistor.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1.0 to 3.6	V
Voltage on V _{CCQ} supply relative to V _{SS}	V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Operating Temperature	T _A	0 to +70	°C
Power Dissipation	P _D	8	W
Short Circuit Current	I _{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_{CC} = V_{CCQ} = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V _{CC} of 2.5V)	V _{CC}	2.3	2.7		
I/O Supply voltage DDR266/DDR333 (nominal V _{CC} of 2.5V)	V _{CCQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	0.49*V _{CCQ}	0.51*V _{CCQ}	V	1
I/O Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{CCQ} +0.30	V	
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	
Input voltage level, CK and CK#	V _{IN} (DC)	-0.3	V _{CCQ} +0.30	V	
Input differential voltage, CK and CK#	V _{ID} (DC)	0.36	V _{CCQ} +0.60	V	3
Input crossing point voltage, CK and CK#	V _{IX} (DC)	0.3	V _{CCQ} +0.60	V	
Input leakage current	Addr, CAS#, RAS#, WE#	I _I	-16	16	uA
	CS#, CKE		-16	16	uA
	CK, CK#		-6	6	uA
	DM		-2	2	uA
Output leakage current	I _{OZ}	-5	5	uA	
Output high current (normal strength); V _{OUT} = V + 0.84V	I _{OH}	-16.8	—	mA	
Output high current (normal strength); V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8	—	mA	
Output high current (half strength); V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9	—	mA	
Output high current (half strength); V _{OUT} = V _{TT} - 0.45V	I _{OL}	9	—	mA	

- NOTES:
- V_{REF} is expected to be equal to 0.5*V_{CCQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed ±2% of the DC value
 - V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
 - V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = V_{CCQ} = 2.5V

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#)	C _{IN1}	20	28	pF
Input Capacitance (CKE0)	C _{IN2}	20	28	pF
Input Capacitance (CS0#)	C _{IN3}	20	28	pF
Input Capacitance (CK0 to CK2, CK0# to CK2#)	C _{IN4}	10	13	pF
Input Capacitance (DM0-DM7)	C _{IN5}	8	9	pF
Data and DQS input/output capacitance (DQ0-DQ63)	C _{OUT1}	8	9	pF



I_{DD} SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CC} = V_{CCQ} = 2.5V ± 0.2V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR333 @ CL = 2.5	Unit
Operating current	I _{DD0} *	One device bank active; Active-Precharge; t _{RC} = t _{RC(MIN)} ; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	1000	mA
Operating current	I _{DD1} *	One device bank; Active-Read-Precharge; BL = 4; t _{RC} = t _{RC(MIN)} ; t _{CK} = t _{CK(MIN)} ; I _{OUT} = 0mA; Address and control inputs change once per clock cycle	1200	mA
Percharge power-down standby current	I _{DD2P} **	All device banks are idle; Power-down mode; t _{CK} = t _{CK(MIN)} ; CKE = LOW	40	mA
Idle standby current	I _{DD2F} **	CS# = HIGH; All device banks are idle; t _{CK} = t _{CK(MIN)} ; CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS and DM	240	mA
Active power-down standby current	I _{DD3P} **	One device bank active; Power-down mode; t _{CK} = t _{CK(MIN)} ; CKE = LOW	240	mA
Active standby current	I _{DD3N} **	CS# = HIGH; CKE = HIGH; One device bank active; t _{RC} = t _{RAS(MAX)} ; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	400	mA
Operating current	I _{DD4R} *	Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t _{CK} = t _{CK(MIN)} ; I _{OUT} = 0mA	1440	mA
Operating current	I _{DD4W} *	Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t _{CK} = t _{CK(MIN)} ; DQ, DM and DQS inputs change twice per clock cycle	1480	mA
Auto refresh current	I _{DD5} **	t _{RC} = t _{RFC(MIN)}	2000	mA
Self refresh current	I _{DD6} **	CKE < 0.2V	40	mA
Operating current	I _{DD7} *	Four device bank interleaving Reads Burst = 4 with auto precharge; t _{RC} = t _{RFC(MIN)} ; t _{CK} = t _{CK(MIN)} ; Address and control inputs change only during Active READ, or WRITE commands	3120	mA

Note: These specifications apply to modules built with Samsung components only.

* Value calculated as one module rank in this operation condition and other module rank in I_{DD2P} (CKE low) mode.

** Value calculated as all module ranks in this operation condition.



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Parameter	Symbol	335		Unit
		Min	Max	
Row cycle time	t _{RC}	60		ns
Refresh row cycle time	t _{RFC}	72		ns
Row active time	t _{RAS}	42	70K	ns
RAS to CAS delay	t _{RCD}	18		ns
Row precharge time	t _{RP}	18		ns
Row active to Row active delay	t _{RRD}	12		ns
Write recovery time	t _{WR}	15		ns
Last data into Read command	t _{WTR}	1		t _{CK}
Clock cycle time	t _{CK}	6	12	ns
Clock high level width	t _{CH}	0.45	0.55	t _{CK}
Clock low level width	t _{CL}	0.45	0.55	t _{CK}
DQS-out access time from CK/CK	t _{DQSQ}	-0.6	+0.6	ns
Output data access time from CK/CK	t _{AC}	-0.7	+0.7	ns
Data strobe edge to output data edge	t _{DQSQ}	—	0.45	ns
Read Preamble	t _{RPRE}	0.9	1.1	t _{CK}
Read Postamble	t _{RPST}	0.4	0.6	t _{CK}
CK to valid DQS-in	t _{DQSS}	0.75	1.25	t _{CK}
DQS-in setup time	t _{WPRES}	0		ns
DQS-in hold time	t _{WPRE}	0.25		t _{CK}
DQS falling edge to CK rising-setup time	t _{DSS}	0.2		t _{CK}
DQS falling edge from CK rising-hold time	t _{DSH}	0.2		t _{CK}
DQS-in high level width	t _{DQSH}	0.35		t _{CK}
DQS-in low level width	t _{DQSL}	0.35		t _{CK}
Address and Control Input setup time (fast)	t _{IS}	0.75		ns
Address and Control Input hold time (fast)	t _{IH}	0.75		ns
Address and Control Input setup time (slow)	t _{ISF}	0.8		ns
Address and Control Input hold time (slow)	t _{IHF}	0.8		ns
Data-out high impedance time from CK/CK	t _{HZS}	-0.7	+0.7	ns
Data-out low impedance time from CK/CK	t _{LZS}	-0.7	+0.7	ns
Output Slew Rate Matching Ratio (rise to fall)	t _{SLMR}	0.67	1.5	

Note: These specifications apply to modules built with Samsung components only.



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (continued)

Parameter	Symbol	335		Unit
		Min	Max	
Mode register set cycle time	tMRD	12		ns
DQ & DM setup time to DQS	tDS	0.45		ns
DQ & DM hold time to DQS	tDH	0.45		ns
Control & Address input pulse width	tIPW	2.2		ns
DQ & DM input pulse width	tDIPW	1.75		ns
Exit self refresh to non-Read command	tXSNR	75		ns
Exit self refresh to read command	tXSRD	200		tck
Refresh interval time	tREFI		7.8	us
Output DQS valid window	tQH	tHP-tQHS	—	ns
Clock half period	tHP	tCLmin or tCHmin	—	ns
Data hold skew factor	tQHS		0.55	ns
DQS write postamble time	tWPST	0.4	0.6	ns
Active to Read with Auto precharge command	tRAP	18		
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tck) + (tRP/tck)		tck

AC OPERATING TEST CONDITIONS

VCC = 2.5V, VCCQ = 2.5V, 0°C ≤ TA ≤ 70°C

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} +0.31		V	1
Input Low (Logic 0) Voltage	V _{IL(AC)}		V _{REF} -0.31	V	1
Input Differential Voltage, CK and CK# inputs	V _{ID(AC)}	0.7	V _{CCQ} +0.6	V	
Input Crossing Point Voltage, CK and CK# inputs	V _{IX(AC)}	0.5*V _{CCQ} -0.2	0.5*V _{CCQ} +0.2	V	

NOTES:

- V_{IH} overshoot: V_{IH} = V_{CCQ} +1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.
V_{IL} undershoot: V_{IL} = -1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.

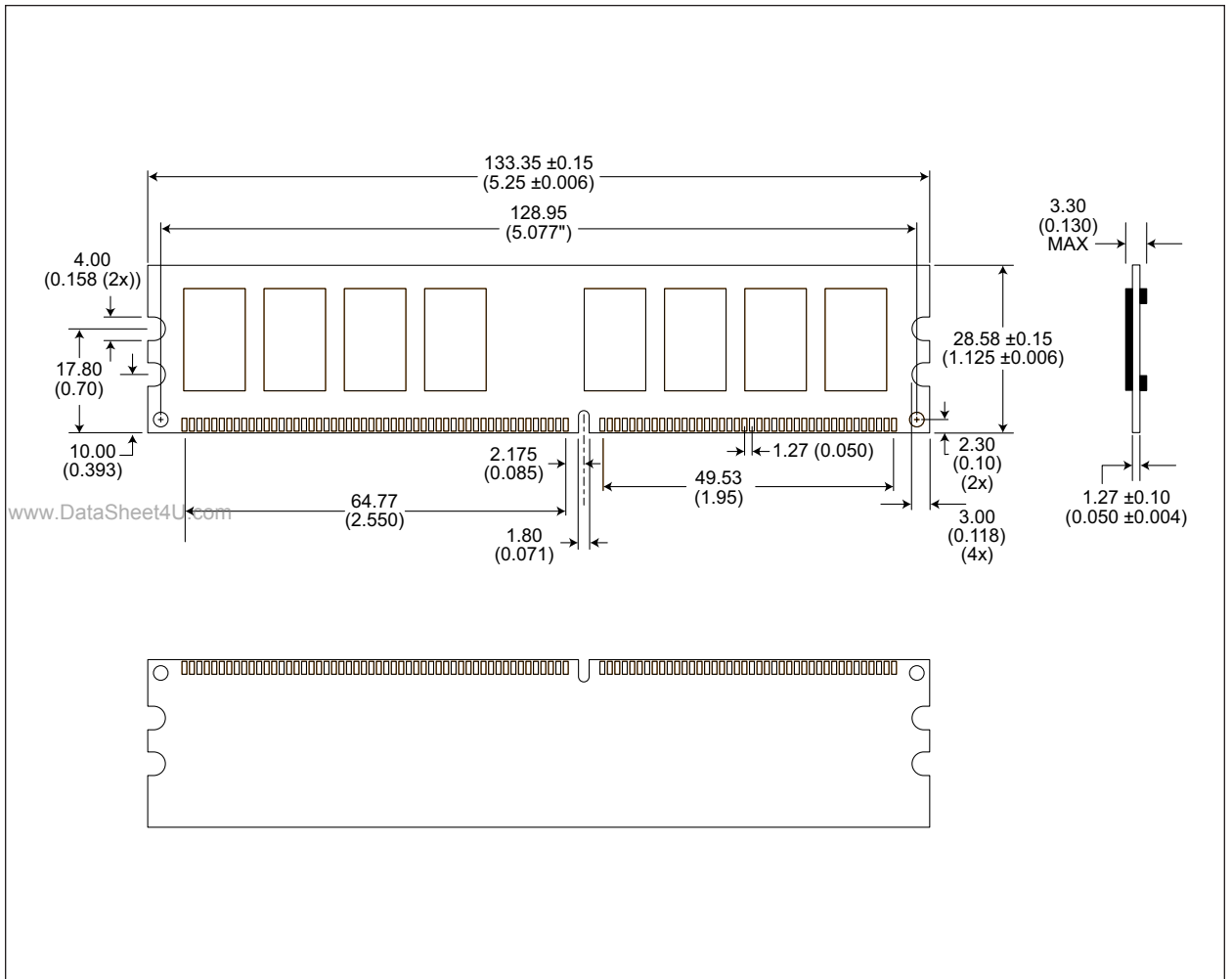


ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*	Temperature
WV3EG64M64ETSU335D3xG	166MHz/333Mb/s	2.5	3	3	28.58 (1.125")	0°C to 70°C

- NOTES:
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

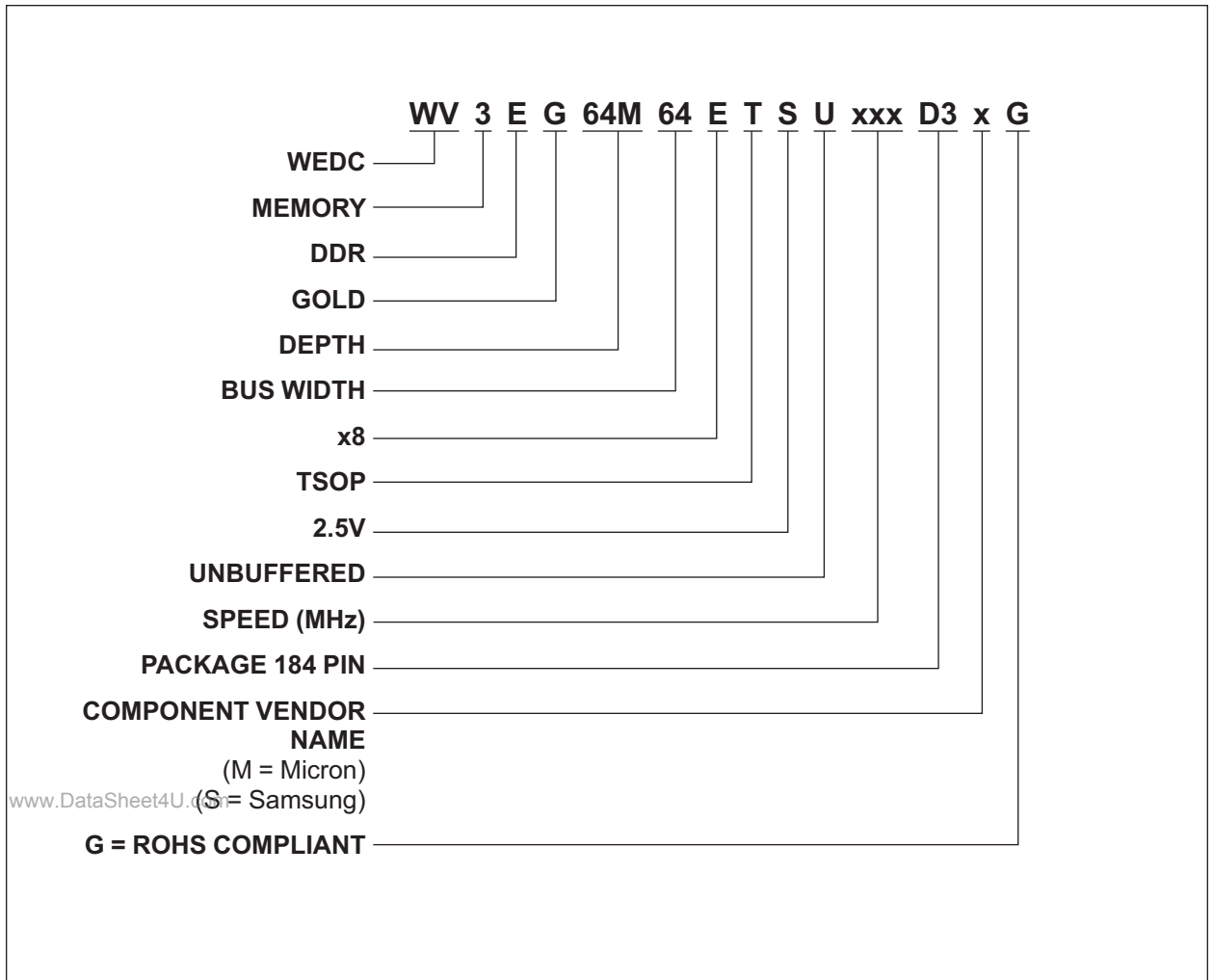
PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 0	Created	7-05	Advanced
Rev 1	1.1 Update to DC, I _{DD} and AC specifications 1.2 Changed from Advanced to Preliminary	8-05	Preliminary

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