



2GB – 2x128Mx72 DDR2 SDRAM UNBUFFERED, ECC w/PLL

FEATURES

- 200-pin, dual in-line memory module (SO-DIMM)
- Support ECC error detection and correction
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- Package option
 - 200 Pin SO-DIMM
 - PCB – 30.00mm (1.181") Max

DESCRIPTION

The WV3HG2128M72EEU is a 2x128Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eighteen 128Mx8 bit stacked BGA with 8 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-6400*	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	400MHz	333MHz	266MHz	200MHz
CL-tRCD-tRP	6-6-6	5-5-5	4-4-4	3-3-3



PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	51	DQ18	101	Vcc	151	Vss
2	Vss	52	Vss	102	A6	152	Vss
3	DQ0	53	DQ19	103	A5	153	DQS5#
4	DQ4	54	DQ28	104	A4	154	DM5
5	Vss	55	Vss	105	A3	155	DQS5
6	DQ5	56	DQ29	106	Vcc	156	Vss
7	DQ1	57	DQ24	107	A2	157	Vss
8	Vss	58	Vss	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	Vcc	159	DQ42
10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	Vss	111	A10/AP	161	DQ43
12	Vss	62	Vss	112	BA1	162	Vss
13	Vss	63	DQS3#	113	BA0	163	Vss
14	DQ6	64	DQ30	114	Vcc	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48
16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	Vss	117	Vcc	167	DQ49
18	Vss	68	Vss	118	CS0#	168	Vss
19	Vss	69	DQ26	119	CAS#	169	Vss
20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	CS1#	171	DQS6#
22	DQ13	72	CB5	122	A13	172	Vss
23	DQ9	73	Vss	123	Vcc	173	DQS6
24	Vss	74	Vss	124	Vcc	174	DQ54
25	Vss	75	CB0	125	ODT1	175	Vss
26	DM1	76	DM8	126	CK	176	DQ55
27	DQS1#	77	CB1	127	NC/CS3#	177	DQ50
28	Vss	78	Vss	128	CK#	178	Vss
29	DQS1	79	Vss	129	DQ32	179	DQ51
30	DQ14	80	CB6	130	Vss	180	DQ60
31	Vss	81	DQS8#	131	Vss	181	Vss
32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56
34	Vss	84	Vcc	134	DQ37	184	Vss
35	DQ11	85	Vss	135	DQS4#	185	DQ57
36	DQ20	86	CB2	136	Vss	186	DM7
37	Vss	87	CKE0	137	DQS4	187	Vss
38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	CKE1	139	Vss	189	DQS7#
40	Vss	90	Vss	140	Vss	190	Vss
41	DQ17	91	NC/CS2#	141	DQ34	191	DQS7
42	NC	92	BA2	142	DQ38	192	DQ63
43	Vss	93	Vcc	143	DQ35	193	DQ58
44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	Vss	195	Vss
46	Vss	96	A11	146	Vss	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59
48	DQ22	98	Vcc	148	DQ44	198	SA1
49	Vss	99	A7	149	DQ41	199	VccSPD
50	DQ23	100	A8	150	DQ45	200	SA0

PIN NAMES

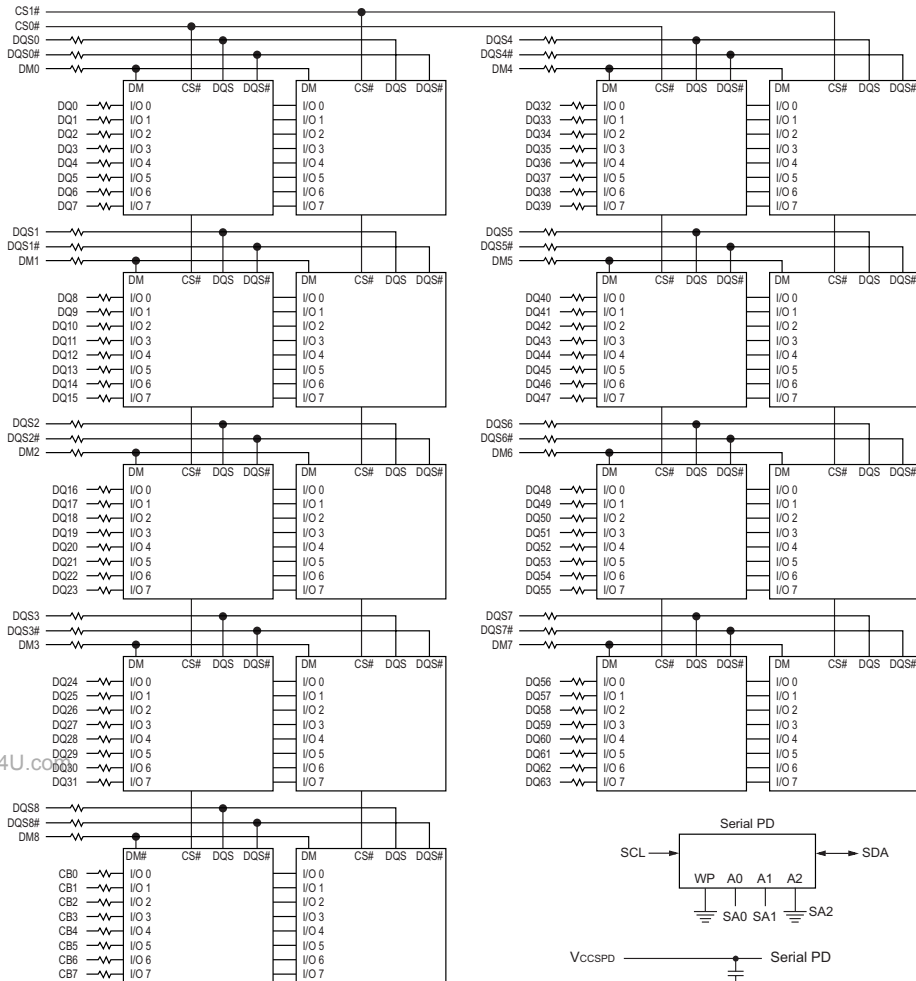
Pin Name	Function
A0-A13	Address Inputs
A10/AP	Address Input/Auto Precharge
BA0 - BA2	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes negative
ODT0, ODT1	On-die termination control
CK,CK#	Clock inputs, positive/negative
CKE0, CKE1	Clock enable input
CS0#, CS1#	Chip select input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
Vcc	Core Power (1.8V)
Vss	Ground
SA0-SA1	SPD address
SDA	Serial Data Input/Output
VREF	Input/Output Reference
DM0-DM8	Data-in mask
VccSPD	Serial EEPROM power supply
SCL	Serial Presence Detect (SPD) Clock Input
NC	No Connect

NOTES:

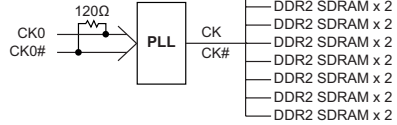
SA2 does NOT connect to memory connector and is shown ONLY on Block Diagram
SA2 is tied LOW on memory module for all memory configurations



FUNCTIONAL BLOCK DIAGRAM



- CS0# → CS0#: DDR2 SDRAMs
- CS1# → CS1#: DDR2 SDRAMs
- BA0 - BA2 → BA0 - BA2: DDR2 SDRAMs
- A0 - A13 → A0 - A13: DDR2 SDRAMs
- RAS# → RAS#: DDR2 SDRAMs
- CAS# → CAS#: DDR2 SDRAMs
- WE# → WE#: DDR2 SDRAMs
- CKE0 → CKE0: DDR2 SDRAMs
- CKE1 → CKE1: DDR2 SDRAMs
- ODT0 → ODT0: DDR2 SDRAMs
- ODT1 → ODT1: DDR2 SDRAMs



NOTE: All resistor values are 22 ohms unless otherwise specified.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-1.0	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
T _{CASE}	Device operating Temperature	0	85	°C	
I _L	Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V<V _{IN} <0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-90	90	μA
		CKE, CS#, ODT	-45	45	μA
		CK,CK#	-10	10	μA
		DM	-10	10	
I _{oz}	Output leakage current; 0V<V _{IN} <V _{CC} ; DQs and ODT are disable				
		DQ, DQS, DQS#	-10	10	μA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-36	36	μA	

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2

Notes:

- V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.



OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0° to 85°	°C	1, 2

- Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
 2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{CC} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IH} (AC)	V _{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V _{IH} (AC)	V _{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (AC)	-	V _{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667	V _{IL} (AC)	-	V _{REF} - 0.200	V

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INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	C _{IN1}	22	40	pF
Input Capacitance (CKE0, CKE1), (ODT0, ODT1)	C _{IN2}	13	22	pF
Input Capacitance (CS0# ~ CS1#)	C _{IN3}	13	22	pF
Input Capacitance (CK, CK#)	C _{IN4}	6	7	pF
Input Capacitance (DM0 ~ DM8), (DQS0 ~ DQS8)	C _{IN5} (665)	9	11	pF
	C _{IN5} (534, 403)	9	12	pF
Input Capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	C _{OUT1} (665)	9	11	pF
	C _{OUT1} (534, 403)	9	12	pF



DDR2 Icc SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only
 $0^{\circ}\text{C} \leq T_{\text{CASE}} < +70^{\circ}\text{C}$; $V_{\text{CCQ}} = +1.8\text{V} \pm 0.1\text{V}$, $V_{\text{CC}} = +1.8\text{V} \pm 0.1\text{V}$

Symbol	Proposed Conditions	806	665	534	403	Units	
Icc0*	Operating one bank active-precharge current; tck = tck(Icc), trc = trc(Icc), tras = trasmin(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,218	1,173	1,128	mA	
Icc1*	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(Icc), AL = 0; tck = tck(Icc), trc = trc(Icc), tras = trasmin(Icc), trcd = trcd(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as Icc4W	TBD	1,308	1,263	1,218	mA	
Icc2P**	Precharge power-down current; All banks idle; tck = tck(Icc); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	516	516	516	mA	
Icc2Q**	Precharge quiet standby current; All banks idle; tck = tck(Icc); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	1,020	930	930	mA	
Icc2N**	Precharge standby current; All banks idle; tck = tck(Icc); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,110	1,020	1,020	mA	
Icc3P**	Active power-down current; All banks open; tck = tck(Icc); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	840	750	750	mA
		Slow PDN Exit MRS(12) = 1	TBD	516	516	516	mA
Icc3N**	Active standby current; All banks open; tck = tck(Icc), tras = trasmax(Icc), trp = trp(Icc); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,200	1,110	1,110	mA	
Icc4W*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(Icc), AL = 0; tck = tck(Icc), tras = trasmax(Icc), trp = trp(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	1,803	1,578	1,443	mA	
Icc4R*	Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(Icc), AL = 0; tck = tck(Icc), tras = trasmax(Icc), trp = trp(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as Icc4W	TBD	1,803	1,578	1,443	mA	
Icc5**	Burst auto refresh current; tck = tck(Icc); Refresh command at every trfc(Icc) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	4,260	4,170	4,080	mA	
Icc6**	Self refresh current; CK and CK1 at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	TBD	108	108	108	mA	
Icc7*	Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(Icc), AL = trcd(Icc)-1*tck(Icc); tck = tck(Icc), trc = trc(Icc), trrd = trrd(Icc), trcd = 1*tck(Icc); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as Icc4R; Refer to the following page for detailed timing conditions	TBD	3,108	2,928	2,748	mA	

Note: Icc specification is based on **SAMSUNG** components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition, and all other module ranks in Icc2P (CKE LOW) mode.

** Value calculated reflects all module ranks in the operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			806		665		534		403		UNIT	
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock	Clock cycle time	CL = 6	t _{CK (6)}	TBD	TBD						ps	
		CL = 5	t _{CK (5)}	TBD	TBD	3,000	8,000				ps	
		CL = 4	t _{CK (4)}	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK (3)}	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width	t _{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	CK low-level width	t _{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	Half clock period	t _{HP}	TBD	TBD	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps	
Clock jitter	t _{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps		
Data	DQ output access time from CK/CK#	t _{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#	t _{HZ}	TBD	TBD		t _{AC} MAX		t _{AC} MAX		t _{AC} MAX	ps	
	Data-out low-impedance window from CK/CK#	t _{LZ}	TBD	TBD	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	ps	
	DQ and DM input setup time relative to DQS	t _{DS}	TBD	TBD	100		100		150		ps	
	DQ and DM input hold time relative to DQS	t _{DH}	TBD	TBD	175		225		275		ps	
	DQ and DM input pulse width (for each input)	t _{DLPW}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	Data hold skew factor	t _{QHS}	TBD	TBD		340		400		450	ps	
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access	t _{QH}	TBD	TBD	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps	
	Data valid output window (DVW)	t _{DVW}	TBD	TBD	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns	
Data Strobe	DQS input high pulse width	t _{DQSH}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS input low pulse width	t _{DQSL}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS output access time from CK/CK#	t _{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising ... setup time	t _{DSS}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS falling edge from CK rising ... hold time	t _{DSH}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS...DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}	TBD	TBD		240		300		350	ps	
	DQS read preamble	t _{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
	DQS read postamble	t _{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
	DQS write preamble setup time	t _{WPRES}	TBD	TBD	0		0		0		ps	
	DQS write preamble	t _{WPRE}	TBD	TBD	0.25		0.25		0.25		t _{CK}	
	DQS write postamble	t _{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
	Write command to first DQS latching transition	t _{DQSS}	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t _{CK}	
Address and control	Address and control input pulse width for each input	t _{IPW}	TBD	TBD	0.6		0.6		0.6		t _{CK}	
	Address and control input setup time	t _{IS}	TBD	TBD	200		250		350		ps	
	Address and control input hold time	t _{IH}	TBD	TBD	275		375		475		ps	
	Address and control input hold time	t _{CCD}	TBD	TBD	2		2		2		t _{CK}	

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page



AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}	TBD	TBD	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCd}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t _{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t _{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	TBD	TBD	t _{WR} + t _{RP}		t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	TBD	TBD	7.5		7.5		10		ns
	PRECHARGE command period	t _{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t _{RPA}	TBD	TBD	t _{RP} +t _{CK}		t _{RP} +t _{CK}		t _{RP} +t _{CK}		ns
LOAD MODE command cycle time	t _{MRD}	TBD	TBD	2		2		2		tck	
CKE low to CK,CK# uncertainty	t _{DELAY}	TBD	TBD	t _{IS} +t _{CK} +t _{IH}		t _{IS} +t _{CK} +t _{IH}		t _{IS} +t _{CK} +t _{IH}		ns	
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t _{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}	TBD	TBD		7.8		7.8		7.8	μs
	Exit self refresh to non-READ command	t _{XS_{NR}}	TBD	TBD	t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t _{XS_{RD}}	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t _{IS_{XR}}	TBD	TBD	t _{IS}		t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AOND}	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t _{AON}	TBD	TBD	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	ps
	ODT turn-off delay	t _{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t _{AOF}	TBD	TBD	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t _{AONPD}	TBD	TBD	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t _{AOFFPD}	TBD	TBD	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t _{ANPD}	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t _{AXPD}	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	TBD	TBD	6 - AL		6 - AL		6 - AL		tck
	A Exit precharge power-down to any non-READ command.	t _{XP}	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t _{CKE}	TBD	TBD	3		3		3		tck

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.



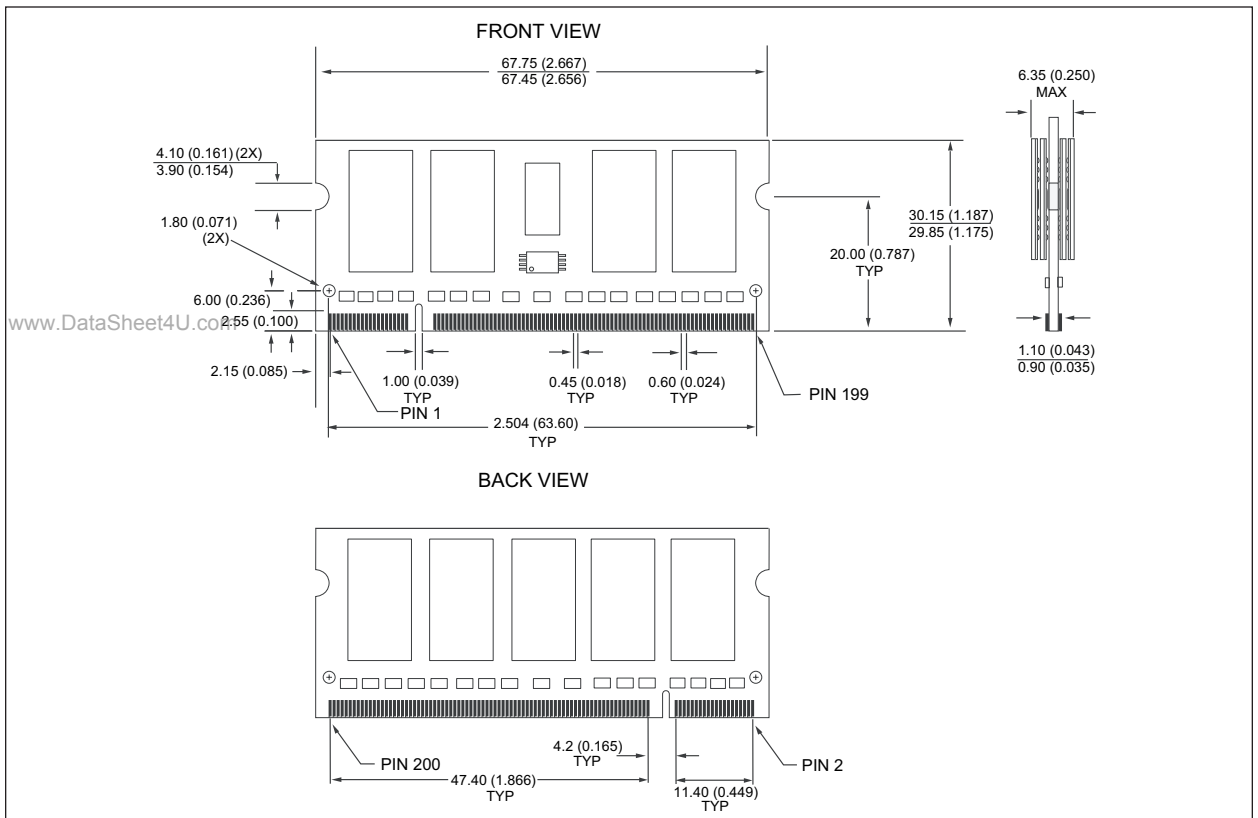
ORDERING INFORMATION FOR D4

Part Number	Clock/Data Rate Speed	CAS Latency	t _{RCD}	t _{RP}	Height*
WV3HG2128M72EEU806AD4-xG	400MHz/800Mb/s	6	6	6	30.00mm (1.181")
WV3HG2128M72EEU665AD4-xG	333MHz/667Mb/s	5	5	5	30.00mm (1.181")
WV3HG2128M72EEU534AD4-xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181")
WV3HG2128M72EEU403AD4-xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181")

NOTES:

- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "-x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

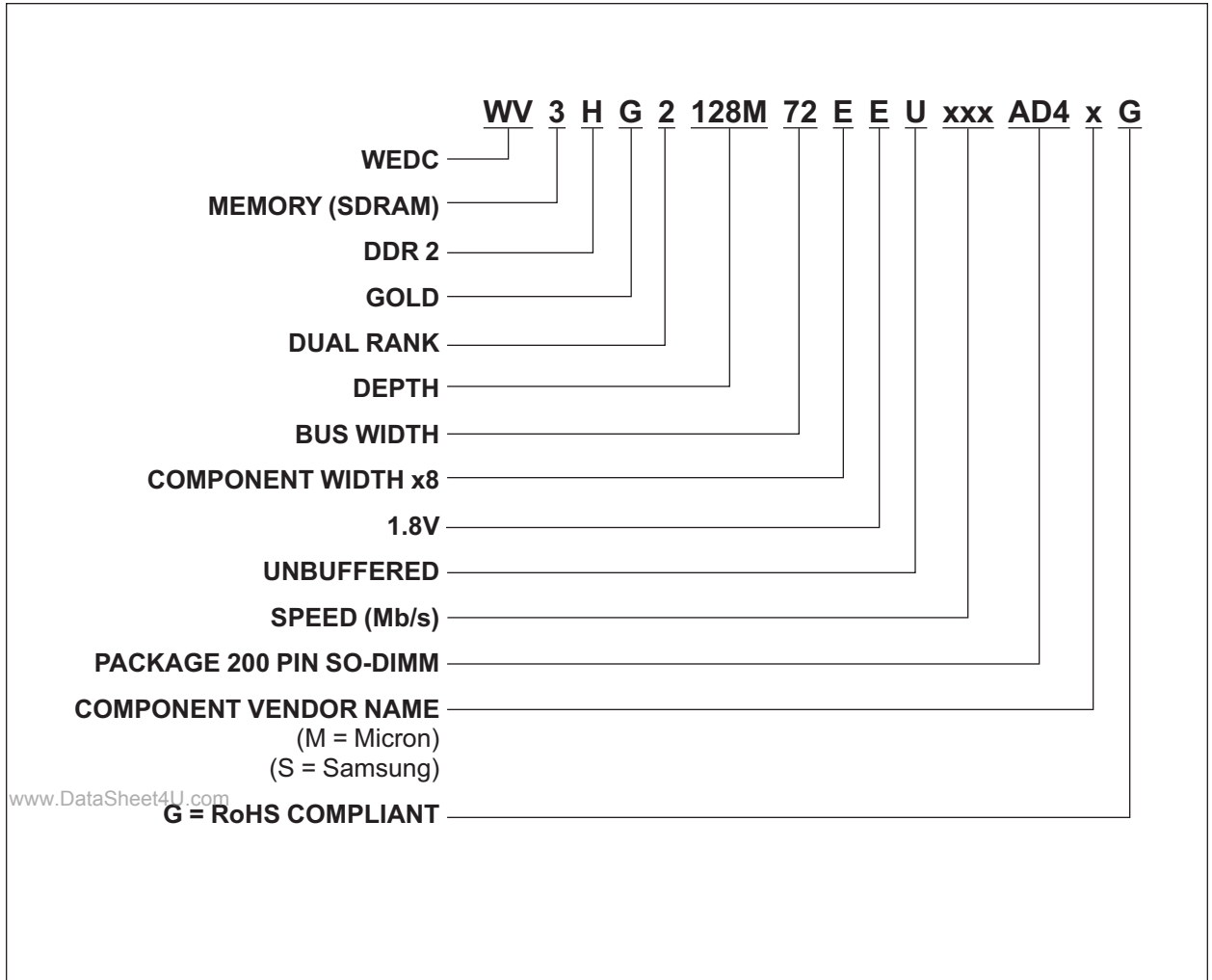
PACKAGE DIMENSIONS FOR AD4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
Tolerances: ±0.13 (0.005) unless otherwise specified



PART NUMBERING GUIDE



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Document Title

2GB – 2x128Mx72 DDR2 SDRAM UNBUFFERED, ECC w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	February 2006	Advanced

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