1GB – 2x64Mx64 DDR2 SDRAM UNBUFFERED

FEATURES

- 200-pin, dual in-line memory module (SO-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 Mb/s DDR2 SDRAM components
- V_{CC} = 1.8V ±0.1V
- V_{CCSPD} = 1.7V to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- JEDEC Package option
  - 200 Pin (SO-DIMM)
  - PCB – 30.00mm (1.181") TYP.

DESCRIPTION

The WV3HG264M64EEU is a 2x64Mx64 Double Data Rate DDR2 SDRAM high density SO-DIMM. This memory module consists of sixteen 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability

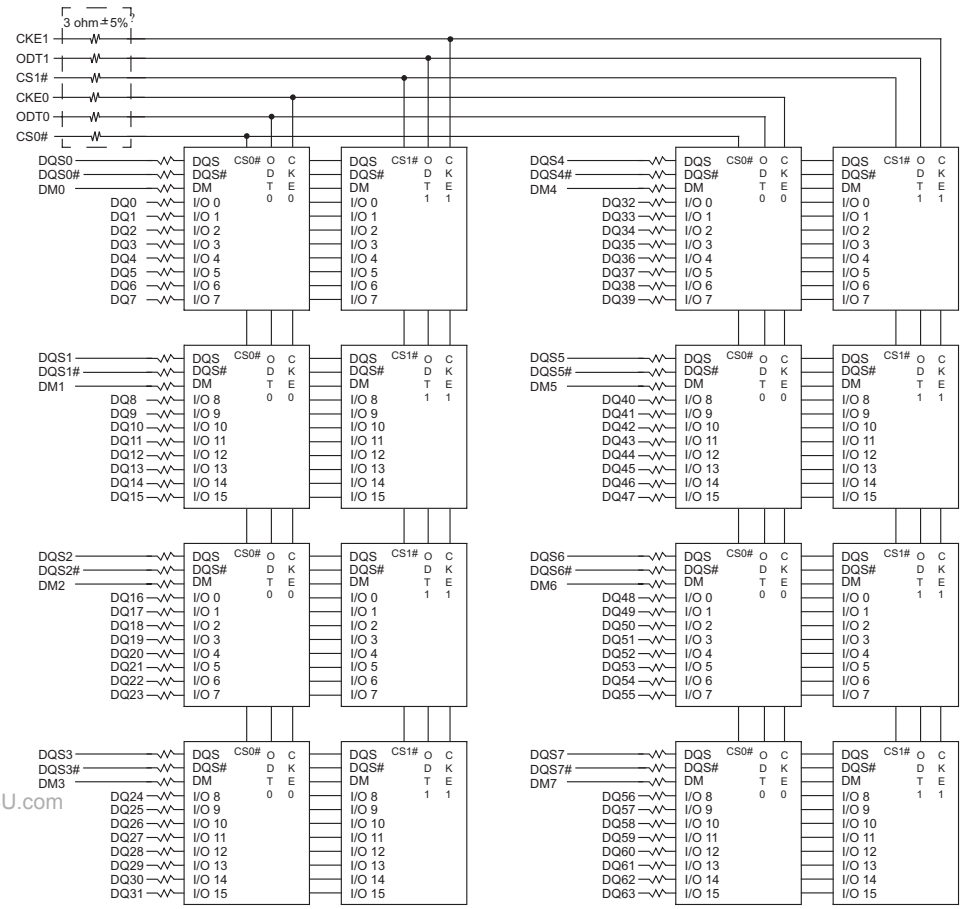
PIN CONFIGURATION

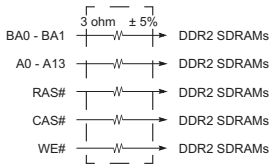
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	DQS2	101	A1	151	DQ42
2	V_{SS}	52	DM2	102	A0	152	DQ46
3	V_{SS}	53	V_{SS}	103	V_{CC}	153	DQ43
4	DQ4	54	V_{SS}	104	V_{CC}	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	V_{SS}
6	DQ5	56	DQ22	106	BA1	156	V_{SS}
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	V_{SS}	58	DQ23	108	RAS#	158	DQ52
9	V_{SS}	59	V_{SS}	109	WE#	159	DQ49
10	DM0	60	V_{SS}	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	V_{CC}	161	V_{SS}
12	V_{SS}	62	DQ28	112	V_{CC}	162	V_{SS}
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	V_{SS}	65	V_{SS}	115	CS1#	165	V_{SS}
16	DQ7	66	V_{SS}	116	A13	166	CK1#
17	DQ2	67	DM3	117	V_{CC}	167	DQS6#
18	V_{SS}	68	DQS3#	118	V_{CC}	168	V_{SS}
19	DQ3	69	NC	119	ODT1	169	DQS6
20	DQ12	70	DQS3	120	NC	170	DM6
21	V_{SS}	71	V_{SS}	121	V_{SS}	171	V_{SS}
22	DQ13	72	V_{SS}	122	V_{SS}	172	V_{SS}
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	V_{SS}	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V_{SS}	77	V_{SS}	127	V_{SS}	177	V_{SS}
28	V_{SS}	78	V_{SS}	128	V_{SS}	178	V_{SS}
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	V_{CC}	131	DQS4	181	DQ57
32	CK0#	82	V_{CC}	132	V_{SS}	182	DQ61
33	V_{SS}	83	NC	133	V_{SS}	183	V_{SS}
34	V_{SS}	84	NC	134	DQ38	184	V_{SS}
35	DQ10	85	NC	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	V_{CC}	137	DQ35	187	V_{SS}
38	DQ15	88	V_{CC}	138	V_{SS}	188	DQS7
39	V_{SS}	89	A12	139	V_{SS}	189	DQ58
40	V_{SS}	90	A11	140	DQ44	190	V_{SS}
41	V_{SS}	91	A9	141	DQ40	191	DQ59
42	V_{SS}	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V_{SS}
44	DQ20	94	A6	144	V_{SS}	194	DQ63
45	DQ17	95	V_{CC}	145	V_{SS}	195	SDA
46	DQ21	96	V_{CC}	146	DQS5#	196	V_{SS}
47	V_{SS}	97	A5	147	DM5	197	SCL
48	V_{SS}	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	V_{SS}	199	V_{CCSPD}
50	NC	100	A2	150	V_{SS}	200	SA1

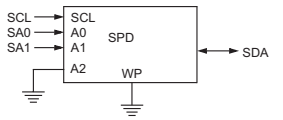
PIN NAMES

Pin Name	Function
CK0,CK1	Clock Inputs, positive line
CK0#, CK1#	Clock Inputs, negative line
CKE0, CKE1	Clock Enables
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CS0#, CS1#	Chip Selects
A0-A9, A11-A13	Address Inputs
A10/AP	Address Input/Auto precharge
BA0,BA1	SDRAM Bank Address
ODT0,ODT1	On-die termination control
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input/Output
SA1,SA0	SPD address
DQ0-DQ63	Data Input/Output
DM0-DM7	Data Masks
DQS0-DQS7	Data strobes
DQS0#-DQS7#	Data strobes complement
V_{CC}	Core and I/O Power
V_{SS}	Ground
V_{REF}	Input/Output Reference
V_{CC}SPD	SPD Power
NC	Spare pins, No connect

FUNCTIONAL BLOCK DIAGRAM

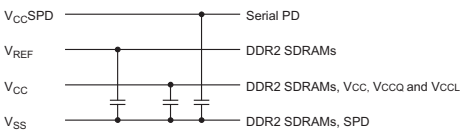






* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0#	8 DDR2 SDRAMs
*CK1/CK1#	8 DDR2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams



Notes :
1. All resistor values are 22 ohms ± 5% unless otherwise specified
2. BAx, Ax, RAS#, CAS#, WE# resistors : 3.0 Ohms ±5%.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.50 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	2

Notes:

1. V_{REF} is expected to equal $V_{CC/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
2. V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	˚C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-80	80	µA
		CS#, CKE	-40	40	µA
		CK, CK#	-40	40	µA
		DM	-10	10	µA
I_{OZ}	Output leakage current; 0V<V_{IN}<V_{CC}; DQs and ODT are disable	DQ, DQS, DQS#	-10	10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-32	32	µA

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	20	36	pF
Input Capacitance (CKE0, CKE1), (ODT0, ODT1)	C_{IN2}	12	20	pF
Input Capacitance (CS0#, CS1#)	C_{IN3}	12	20	pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C_{IN4}	12	20	pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C_{IN5} (667)	9	11	pF
	C_{IN5} (534)	9	12	pF
Input Capacitance (DQ0 ~ DQ63)	C_{OUT1} (667)	9	11	pF
	C_{OUT1} (534)	9	12	pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0° to 85°	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(DC)	V_{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V_{IH}(DC)	V_{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(DC)	-	V_{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667, DDR2-800 TBD	V_{IL}(DC)	-	V_{REF} - 0.200	V

I_{CC} SPECIFICATION

Symbol	Proposed Conditions		806	665	534	403	Units
I_{CC0}*	Operating one bank active-precharge; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	744	704	704	mA
I_{CC1}*	Operating one bank active-read-precharge; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	864	824	824	mA
I_{CC2P}**	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	128	128	128	mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		TBD	560	480	480	mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		TBD	640	560	560	mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	480	480	480	mA
		Slow PDN Exit MRS(12) = 1	TBD	192	192	192	mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC}$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	880	800	800	mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	1184	1024	944	mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		TBD	1224	1064	944	mA
I_{CC5}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		TBD	2400	2240	2240	mA
I_{CC6}**	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	128	128	128	mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = $t_{RC}D(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		TBD	1824	1824	1824	mA

I_{CC} specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Note:

* Value calculated as one module rank in this operating condition, and all other module ranks in ICC2P (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				806		665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	$t_{CK\ (6)}$	TBD	TBD							ps
		CL = 5	$t_{CK\ (5)}$	TBD	TBD	3,000	8,000					ps
		CL = 4	$t_{CK\ (4)}$	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	TBD	TBD	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t_{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}	TBD	TBD		t_{AC} MAX		t_{AC} MAX		t_{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	TBD	TBD	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t_{DS}	TBD	TBD	100		100		150		ps
	DQ and DM input hold time relative to DQS		t_{DH}	TBD	TBD	225		225		275		ps
	DQ and DM input pulse width (for each input)		t_{DIPW}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}	TBD	TBD		340		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	TBD	TBD	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	TBD	TBD	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising … setup time		t_{DSS}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}	TBD	TBD	0.2		0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	TBD	TBD		240		300		350	ps
	DQS read preamble		t_{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	TBD	TBD	0		0		0		p s
	DQS write preamble		t_{WPRE}	TBD	TBD	0.35		0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}
	Address and control input pulse width for each input		t_{IPW}	TBD	TBD	0.6		0.6		0.6		t_{CK}
	Address and control input setup time		t_{IS}	TBD	TBD	200		250		350		ps
	Address and control input hold time		t_{IH}	TBD	TBD	275		375		475		ps
	Address and control input hold time		t_{CCD}	TBD	TBD	2		2		2		t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page

AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			800		665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}	TBD	TBD	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t_{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	TBD	TBD	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	TBD	TBD	t_{WR} + t_{RP}		t_{WR} + t_{RP}		t_{WR} + t_{RP}		ns
	Internal WRITE to READ command delay	t_{WTR}	TBD	TBD	7.5		7.5		10		ns
	PRECHARGE command period	t_{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t_{RPA}	TBD	TBD	t_{RP}+t_{CK}		t_{RP}+t_{CK}		t_{RP}+t_{CK}		ns
	LOAD MODE command cycle time	t_{MRD}	TBD	TBD	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	TBD	TBD	t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		t_{IS} + t_{CK} + t_{IH}		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command internal	t_{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t_{REFI}	TBD	TBD		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	TBD	TBD	t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t_{XSRD}	TBD	TBD	200		200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	TBD	TBD	t_{IS}		t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	TBD	TBD	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	ps
	ODT turn-off delay	t_{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	TBD	TBD	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	TBD	TBD	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	TBD	TBD	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	TBD	TBD	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	TBD	TBD	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	TBD	TBD	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	TBD	TBD	7 - AL		6 - AL		6 - AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	TBD	TBD	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	TBD	TBD	3		3		3		t_{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

ORDERING INFORMATION FOR D4

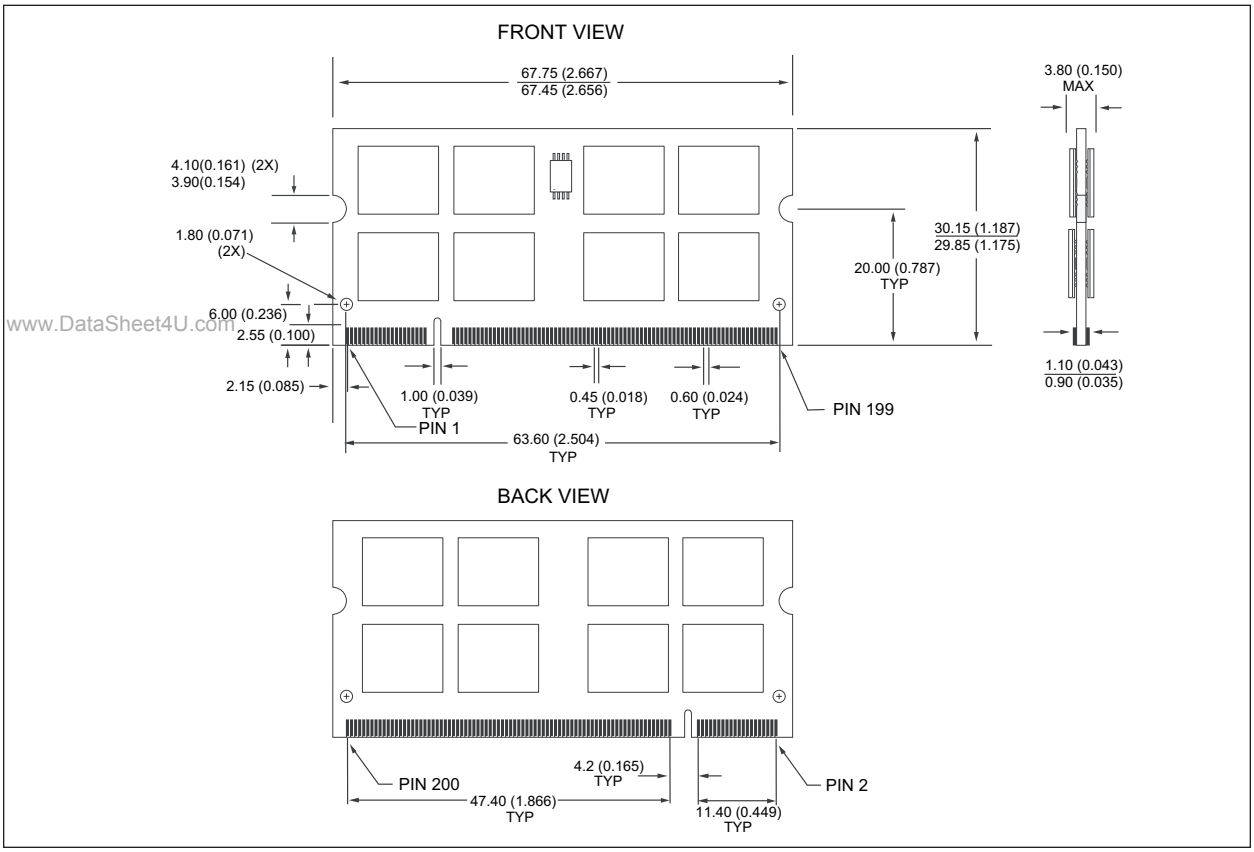
Part Number	Clock/Data Rate Speed	CAS Latency	t_{RCD}	t_{RP}	Height**
WV3HG264M64EEU806D4xG*	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG264M64EEU665D4xG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG264M64EEU534D4xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG264M64EEU403D4xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Consult factory for availability

NOTES:

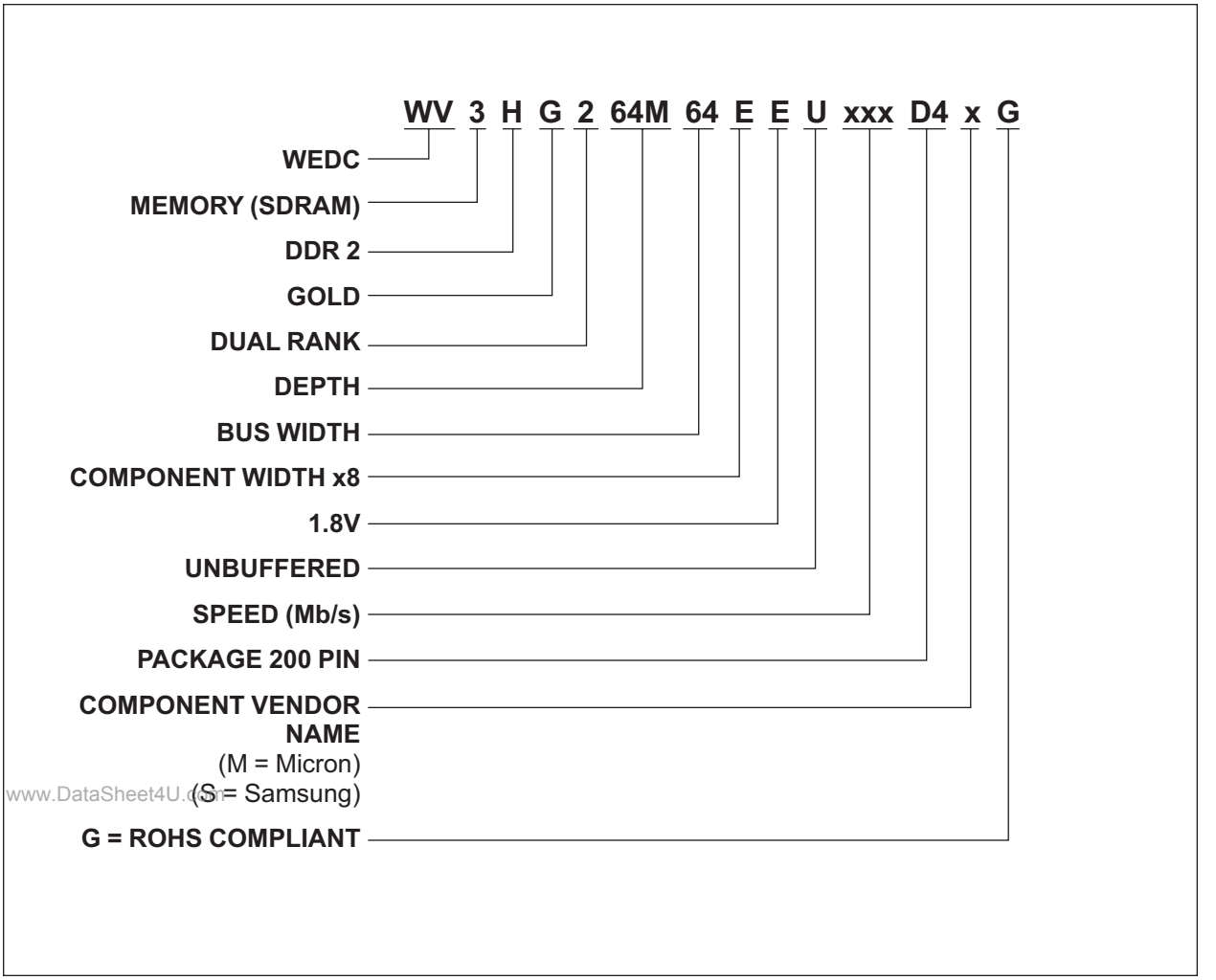
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

1GB – 2x64Mx64 DDR2 SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	February 2005	Advanced
Rev 1	1.1 Updated AC specifications	November 2005	Advanced
Rev 2	2.1 Update Specifications • V_{CC} • Maximum Rating	Febraury 2006	Advanced