CUSTOMER APPROVAL SHEET

Company Name

MODEL IEX139BLB01.0

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☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**

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Product Specification

1.39" COLOR AMOLED MODULE

MODEL NAME: X139BLB01

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	Dec. 2, 2014		First Draft
0.0	Jan 20, 2015		Increase IC initial code

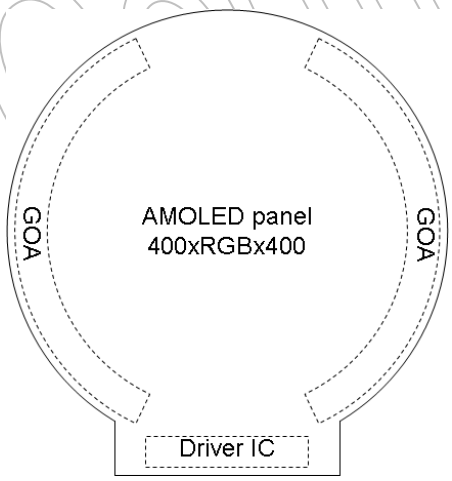
Contents

A. General Specification

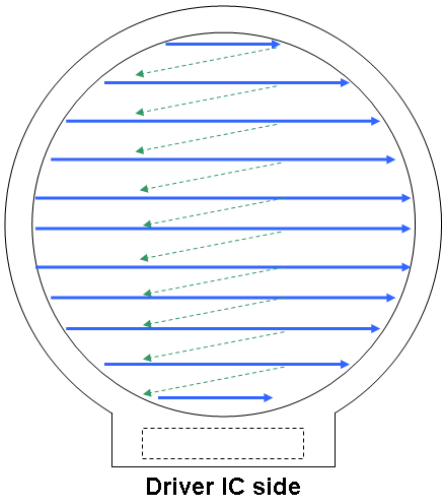
1. Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.39”	
2	Display Mode	AMOLED	
3	Display Resolution (dot)	400xRGBx400	
4	Active Area (mm*mm)	35.4 (H)×35.4(V)	
5	Pixel Configuration	Hyper R.G.B	
6	Display Color (M)	16.7	
7	Brightness (nits)	350	
8	Interface	MIPI DSI	
9	Outline Dimension (mm*mm*mm)	38.6 (H) × 40.5(V) × 0.7(T)	cell+foam

2. Module Block Diagram



3. Panel Scan direction



B. Electrical Specifications

1. Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

FPCA recommended connector: 504248-2410 (Molex)

Main board recommended connector: 504208-2410 (Molex)

FPC	Pin_name	I/O	Description
1	**GND**	P	Ground
2	**XRES**	I	Device reset signal (0 : Enable ; 1: Disable)
3	**DSI_D0N**	I/O	MIPI negative data signal
4	**SWIRE**	O	SWIRE signal for PWR IC control
5	**DSI_D0P**	I/O	MIPI positive data signal
6	**NC**	-	Flaoting
7	**GND**	P	Ground
8	**TE**	I	Vsync(vertical sync)signal output from panel to avoid tearing effect
9	**DSI_CLKN**	I	MIPI negative clock signal
10	**GND**	P	Ground
11	**DSI_CLKP**	I	MIPI positive clock signal
12	**GND**	P	Ground
13	**GND**	P	Ground
14	**GND**	P	Ground
15	**VDDIO**	P	Power supply for Interface system excep MIPI interface
16	**VCI**	P	Driver analog power supply
17	**GND**	P	Ground
18	**GND**	P	Ground
19	**ELVSS**	P	AMOLED negative power supply
20	**ELVDD**	P	AMOLED positive power supply
21	**ELVSS**	P	AMOLED negative power supply
22	**ELVDD**	P	AMOLED positive power supply
23	**ELVSS**	P	AMOLED negative power supply
24	**ELVDD**	P	AMOLED positive power supply

Note: I = input ; O = output ; P = Power ; I/O = input / Output

2. Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power supply	VDDIO	-0.3	5.5	V	
Analog Power supply	VCI	-0.3	5.5	V	
ELVDD power supply	ELVDD	-	5.0	V	
ELVSS power supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

C. Electrical Characteristics

1. DC Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power supply		VDDIO	1.65	1.8	3.3	V	Note1
Analog Power supply		VCI	2.7	2.8	3.6	V	Note1
ELVDD power supply		ELVDD	4.55	4.60	4.65	V	Note1,2
ELVSS power supply		ELVSS	-2.35	-2.40	-2.45	V	Note1
Input Signal Voltage	H Level	V_{IH}	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	V_{IL}	0	-	0.2* VDDIO	V	
Output Signal Voltage	H Level	V_{OH}	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	V_{OL}	0	-	0.2* VDDIO	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2 : RT4723 Positive output voltage = 4.6V ± 0.8% at -40℃ ≦ Ta ≦ +85 ℃

2. Display Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD:4.6V ELVSS:-2.4V	--	--	163.8	mW	Note1,2,
		I_{NL}		--	--	23.4	mA	Note1,2,
IC	**Normal**	P_{VCI}	VCI : 2.8V	--	9.2	--	mW	Note2,
		I_{VCI}		--	3.3	--	mA	Note2,
		P_{VDDIO}	VDDIO :1.8V	--	7.9	--	mW	Note2,
		I_{VDDIO}		--	4.4	--	mA	Note2,
	Idle	P_{VCI}	VCI : 2.8V	--	3.6		mW	Note3,
		I_{VCI}		--	1.3		mA	Note3,
		P_{VDDIO}	VDDIO :1.8V	--	2.5		mW	Note3,
		I_{VDDIO}		--	1.4		mA	Note3,

Note 1: Based on L255 (350nits) full white pattern

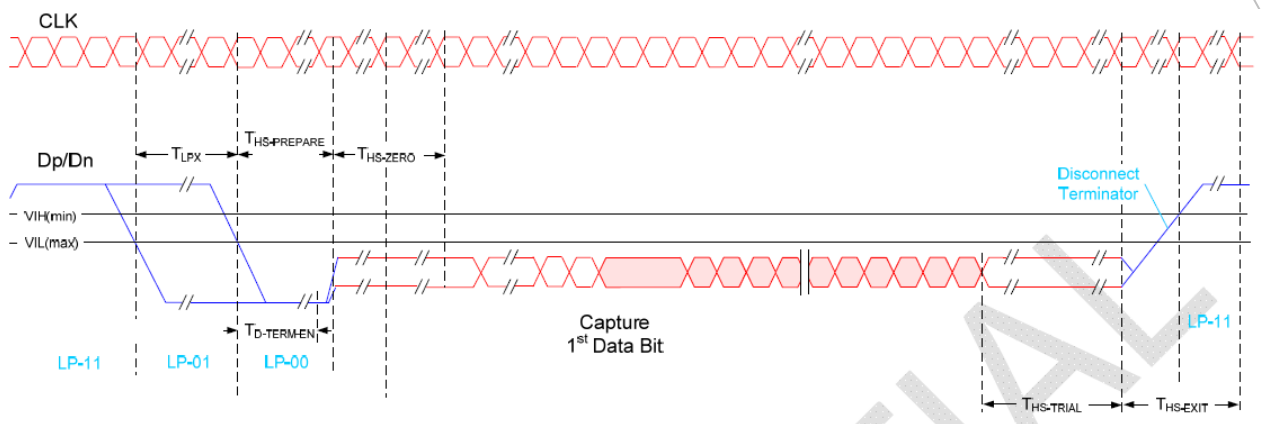
Note 2: Testing in MIPI-DSI frame rate 60Hz command mode.

Note 3: Testing in MIPI-DSI frame rate 5Hz command mode.

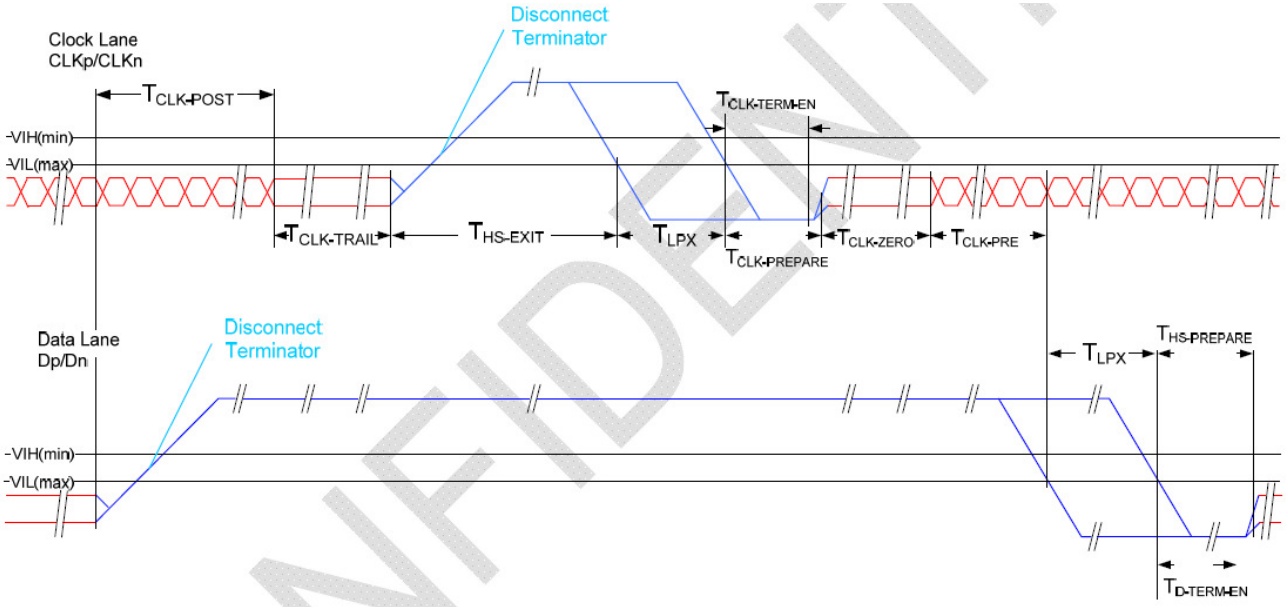
D. AC Characteristics

1. MIPI Interface Characteristics

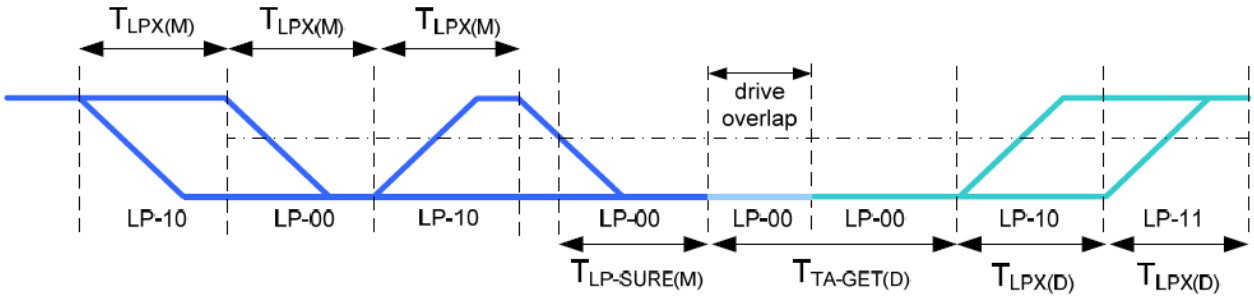
HS Data Transmission Burst



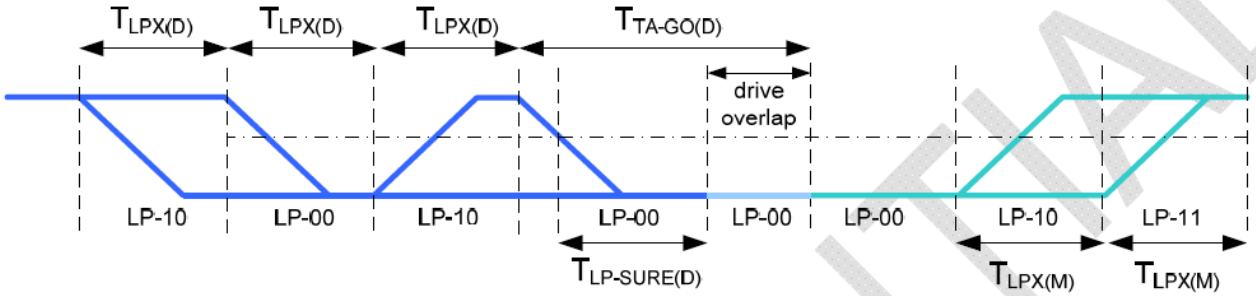
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



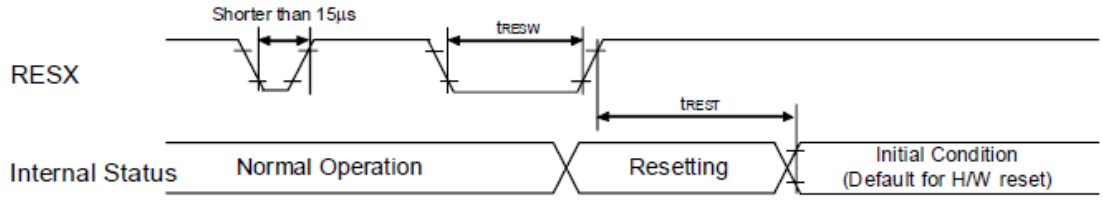
Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock	38		95	ns

	Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.				
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

2. Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

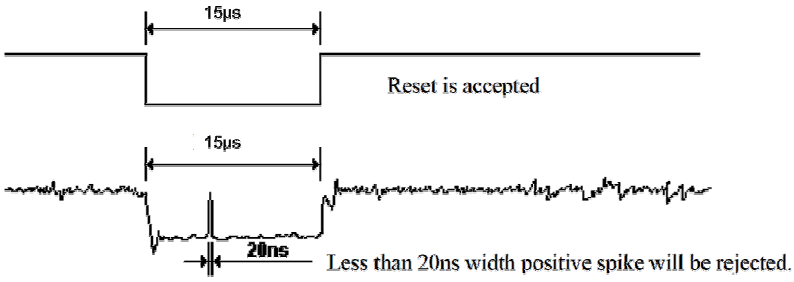
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 15µs	Reset
Between 5µs and 15µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

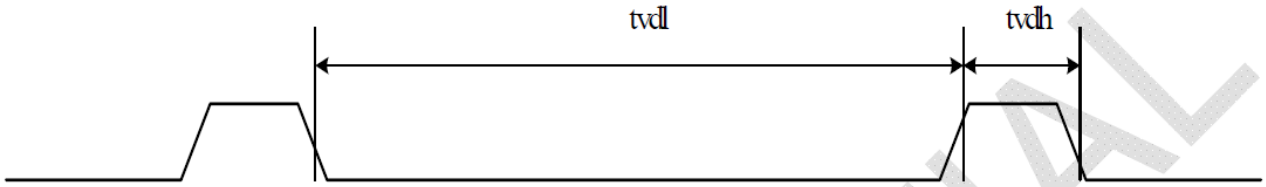
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3. TE Timing Characteristics

Mode 1, the tearing effect output signal consist of V-sync information only:

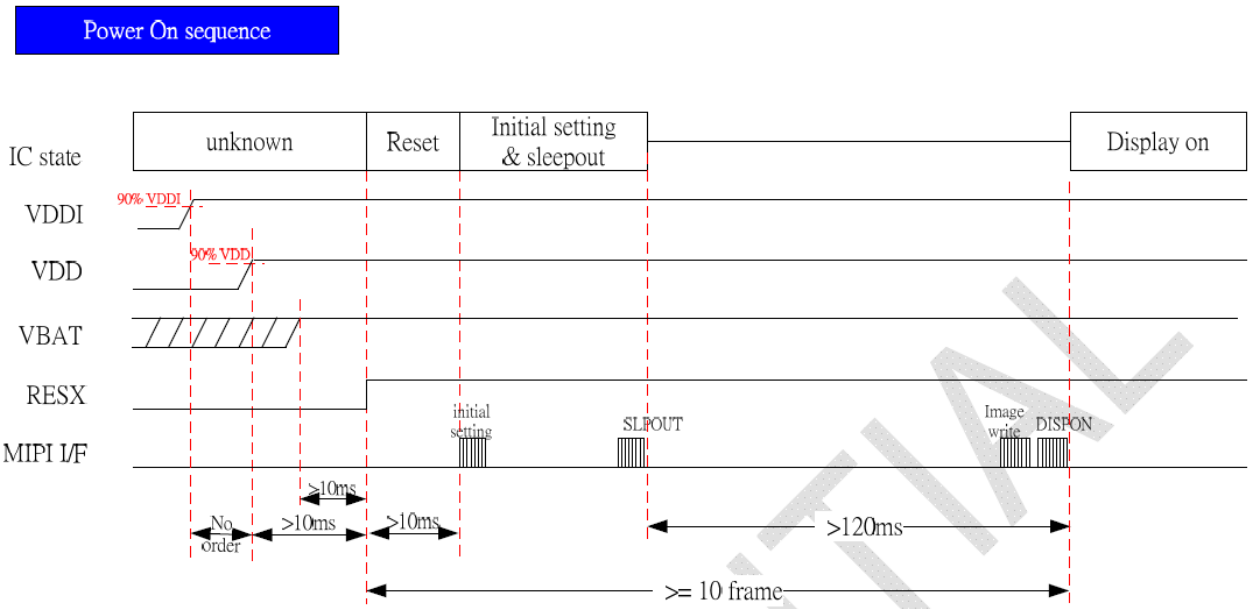


tvdh = The LCD display is not updated from the frame memory.
tvdl = The LCD display is updated from the frame memory.

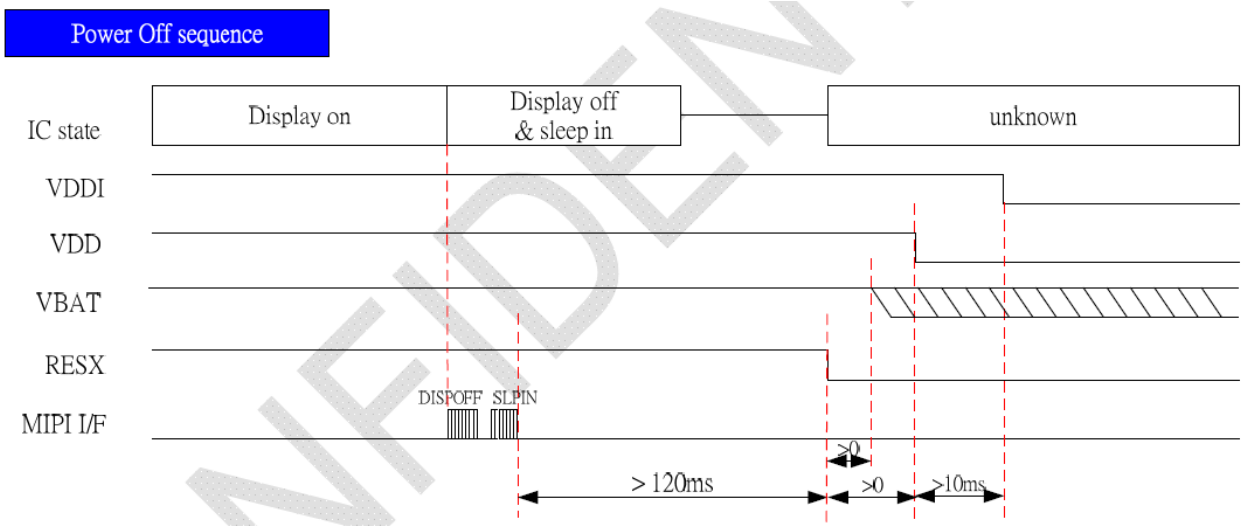
E. Recommended Operating Sequence

1. Display Power on / off Sequence

Power on sequence



Power off sequence



Display Initial code

Recommended Power on Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Turn on V_{CI}							VCI=2.8V
2	Turn on V_{DDIO}							VDDIO=1.8V
3	Delay	no limit						
4	REST pin low	20us						
5	REST pin high							
6	Delay	5 ms						
7			W	0x15	FE	FE00	05	
8			W	0x15	50	5080	01	
9			W	0x15	4F	4F80	09	
10			W	0x15	BF	BF80	06	
11			W	0x15	C0	C080	04	
12			W	0x15	C1	C180	60	
13			W	0x15	2A	2A80	00	
14			W	0x15	05	0580	15	
15			W	0x15	FE	FE00	07	
16			W	0x15	07	07A0	4F	
17			W	0x15	FE	FE00	00	
18			W	0x15	35	3500	00	
19	Sleep out		W	0x05	11	1100	00	
20	Turn on peripheral packet			0x32				Video Turn On
21	Delay	300 ms						
22	Display on		W	0x05	29	2900	00	

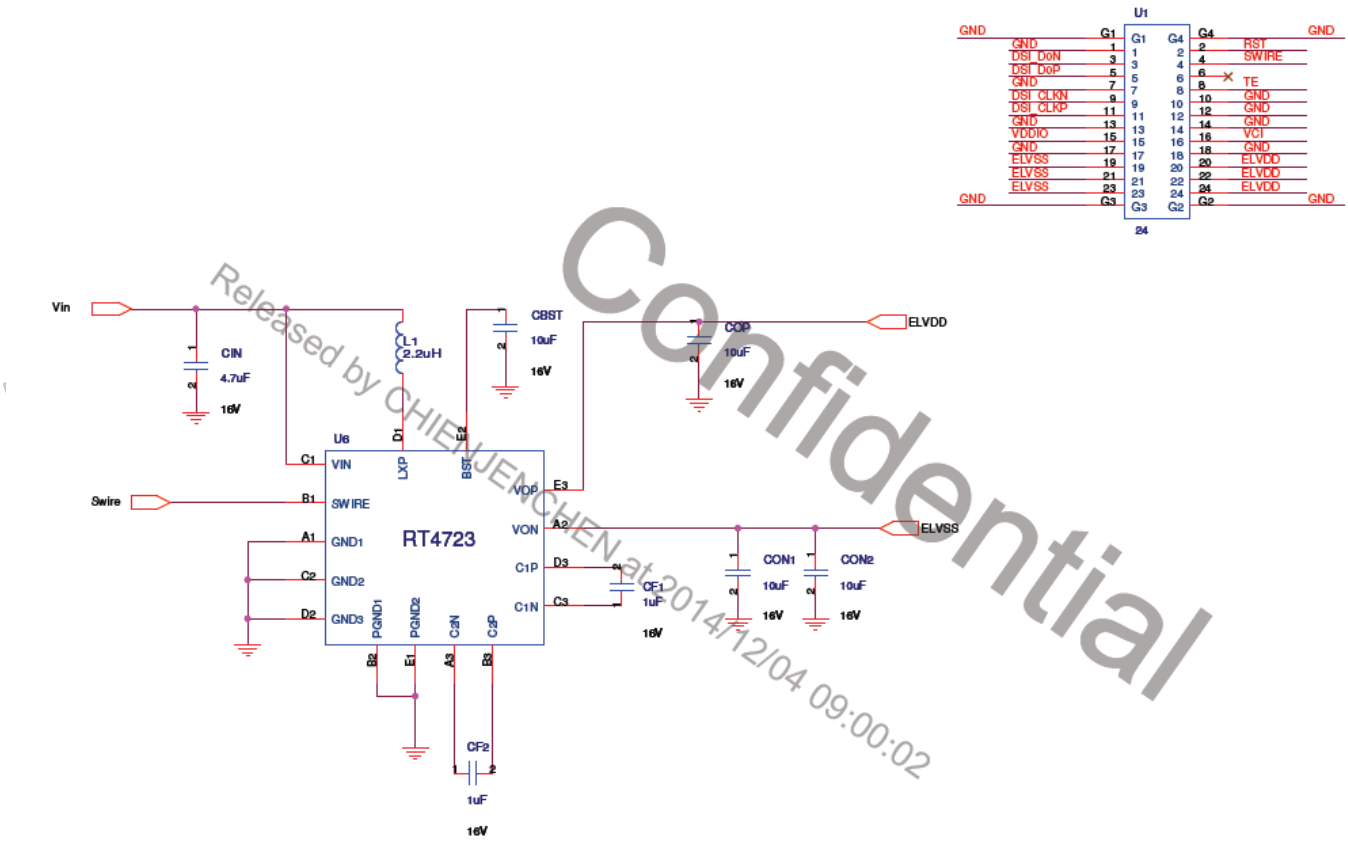
Recommended Power off Mode Sequence

Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	DIPOFF		W	0x05	28	2800	00	
2	SLPIN		W	0x05	10	1000	00	
3	delay	120ms						
4	Power off							

F. Brightness Control

Recommended Brightness Control							
Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
				MIPI	Others		
DIPOFF		W	0x05	51	5100	Value	Value form 0~255(FF)

G. Application Circuit



1. Recommed power IC RT4723, **Richtek**
2. Recommend power inductor L1
   a. [TOKO – DFE252010C (1269AS-H-2R2N=P2)] 2.2uH 2.5mm*2.0mm*1.0mm
   b. [Taiyo – MDKK2020T2R2MM] 2.2uH 2.0mm*2.0mm*1.0mm

3. 24pin Connector
   FPCA recommended connector: 504248-2410 (Molex)
   Main board recommended connector: 504208-2410 (Molex)

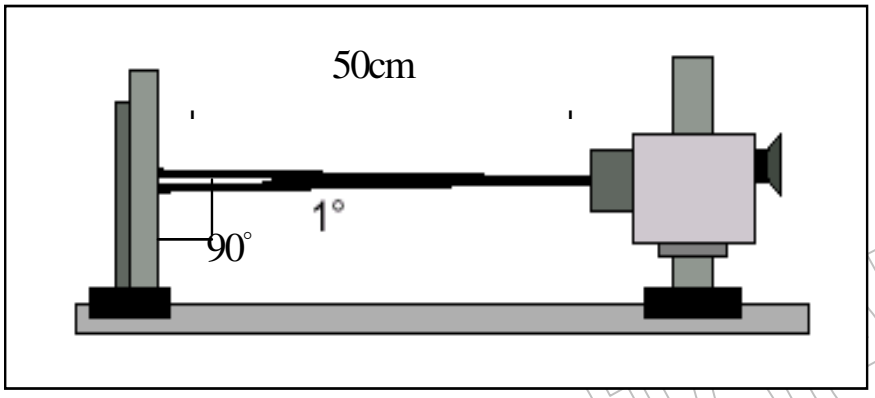
H. Specifications

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Optical Characteristic (w/o Cover Lens)		Brightness	315	350	--	nits	Note 3
		Wx	0.28	0.30	0.32		
		Wy	0.29	0.31	0.33		
Contrast ratio		@25deg	10000		--		Note 4
Brightness Uniformity		350nits	85		--		Note 5
Viewing angle CR>1600		Top	80°		--	deg	Note 6
		Bottom	80°		--	deg	
		Left	80°		--	deg	
		Right	80°		--	deg	
Color	Red	CIE1931 x	0.645	0.675	0.705	Red	Note 7
	Red	CIE1931 y	0.295	0.325	0.355	Red	
	Green	CIE1931 x	0.186	0.236	0.286	Green	
	Green	CIE1931 y	0.661	0.711	0.761	Green	
	Blue	CIE1931 x	0.090	0.130	0.170	Blue	
	Blue	CIE1931 y	0.025	0.065	0.105	Blue	
NTSC		CIE x , y	100	--	--	%	
Life time	T95	25℃	--	100	--	hrs	Note 8
Crosstalk	L128△CT	Vertical	--	--	1.1		Note 9
Flicker			--	-30	--	db	Note 10
Optical Switching Time		+25℃B/W(Tr+Tf)/2	--	--	1	ms	Note 11
Gamma		γ	1.9	2.2	2.5		

Note 1: Ambient temperature =25 ºC±2 ºC

Note 2: To be measured in the dark room.

Note 3: The brightness measurement shall be done at the center of the display with a full white image. The brightness shall meet the following spec, at 100% check.

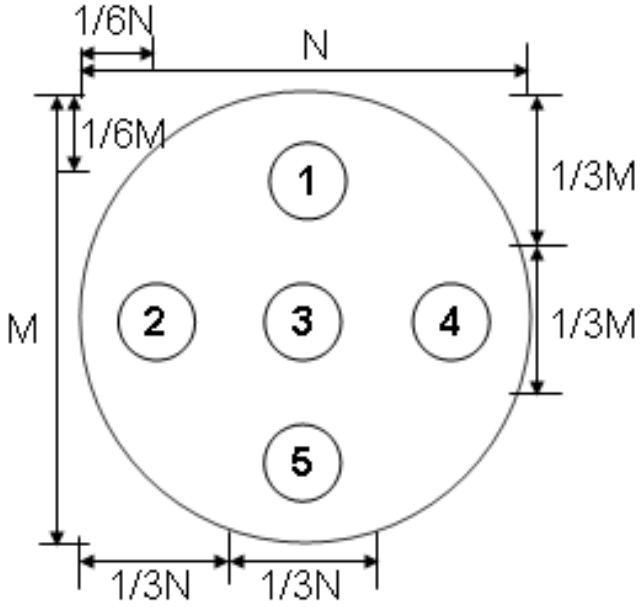


Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” state}}{\text{Photo detector output when OLED is at “Black}}$$

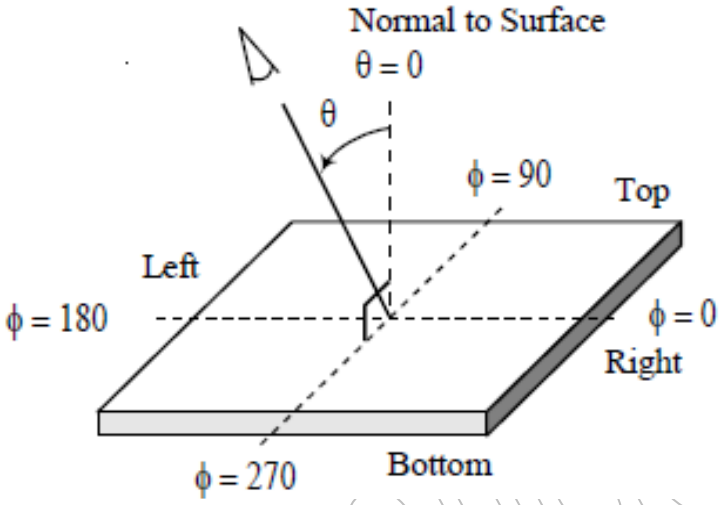
Note 5: Uniformity. Refer to figure as below



- △Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 5 measured spots
- Bp (Min.) = Minimum brightness in 5 measured spots.

Note 6: Definition of viewing angle :

The optical performance is specified as the driver IC located at =270°



Note 7: The color chromaticity should be based on sample performance because new OLED material should be verified later.

Note 8: Time to 95% Luminance

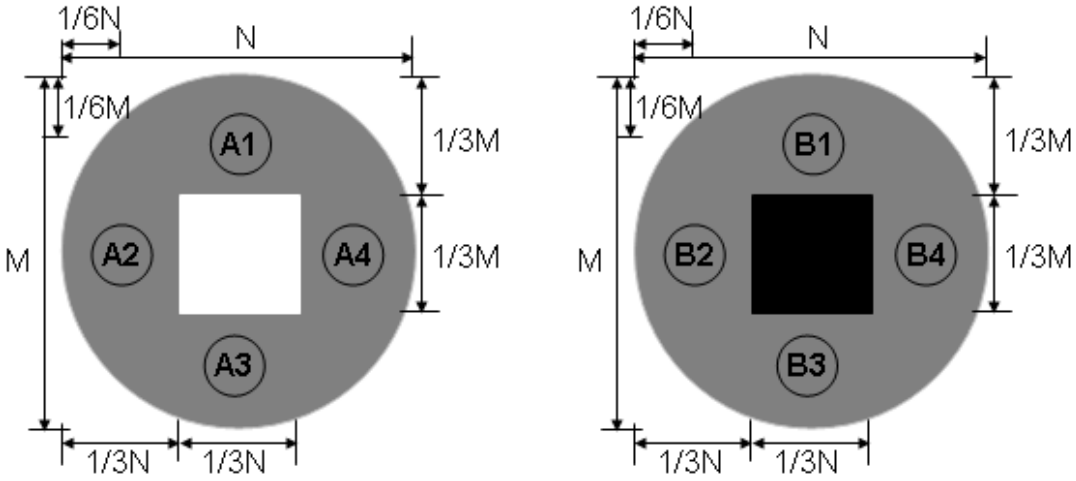
To measure the burn-in effect, a test pattern with white background applied to the AMOLED display at 30% loading

Note 9: Cross-talk

- There should be no visible cross-talk in normal direction of the display when the two ”Cross-talk Test Patterns ” below are loaded.
- Measurement equipment: CS2000 or similar equipments
- The point should be marked is, the background of Cross-talk Test Pattern-“gray “ are defined as middle gray scale . For example, RGB 24bit “gray” defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- △Bpn = Bpn (gray) / Bpn (white)
  Which n means the dot No. In the Cross-talk Test Pattern ;
  Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern;
  Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;
- △Bp (Max.) = Maximum value in △Bp1~△Bp4
- △Bp (Min.) = Minimum value in △Bp1~△Bp4.
- △CT=△Bp (Max.)/ △Bp(Min.).
- △CT must be less than 1.10



Note 10: Flicker

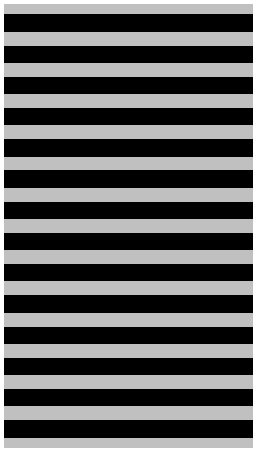
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flic\ker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

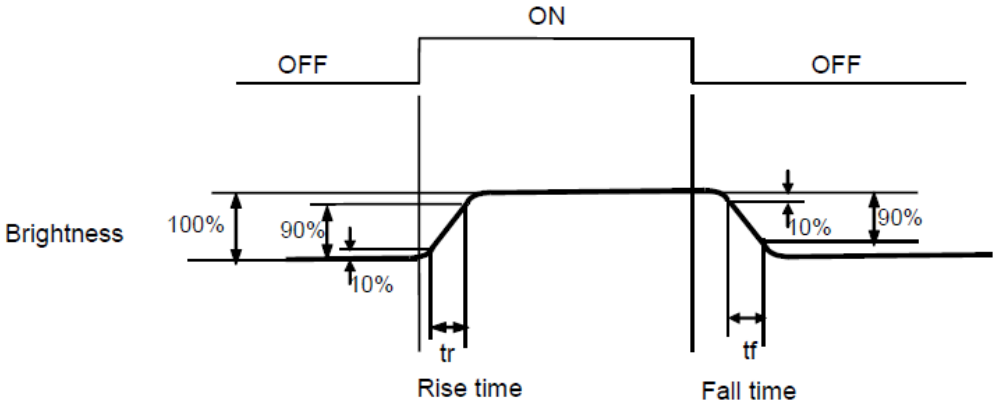
The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.



Note 11: Optical Switching Time:

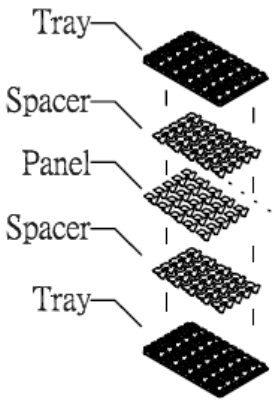
The optical switching time measurements should be performed at driven BLACK and driven WHITE at typ. brightness setting by the driving techniques specified. The luminance should be measured with the emitting display and the detector at θ=0°and ψ=90°. The rise time tr is the time between a 10% optically response of the display and a 90% optically response of the display. The fall time tf is the time between a 10% optically response of the display and a 90% optically response to the display. The response time is defined as the average of the rise time and the fall time.



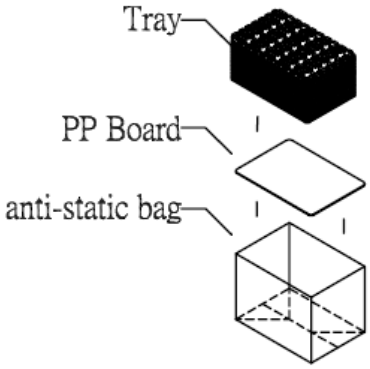
I. Reliability Test Items

Category	No.	Test items	Conditions	Remark
Reliability (Environment)	1	High Temp. Operation	Ta= 60ºC 240 hrs	Reliability (Environment)
	2	High Temp. Storage	Ta= 80 ºC 240 hrs	
	3	Low Temp. Operation	Ta= -20 ºC 240 hrs	
	4	Low Temp. Storage	Ta= -30 ºC 240 hrs	
	5	High Temp./Humi. Operation	Ta= 60 ºC. 90% RH 240 hrs	
	6	Thermal Shock	-40 ºC ~ 80 ºC, Dwell for 30 min. 100 cycles.	Non-operation

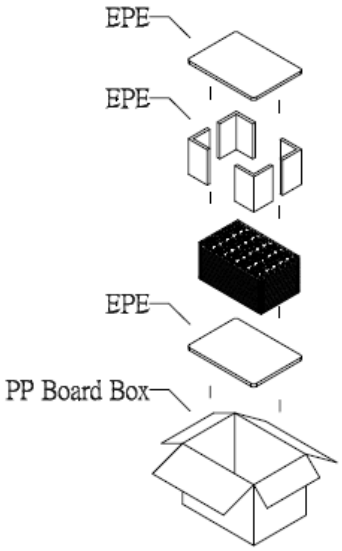
J. Packing



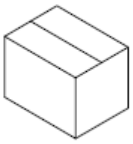
1 tray for 25 pcs Panels



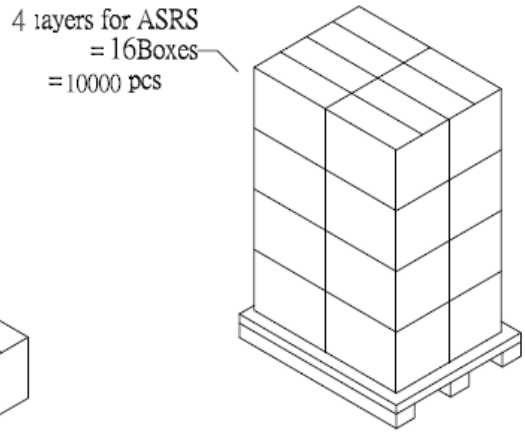
1 set for 25+1 pcs trays =625 pcs



X139BLB01 包材包裝示意圖



Carton DIM：
590*390*326mm



Pallet DIM：
1200*800*132mm

K. Outline Demension (Tentative)