64K X24645 8192 x 8 Bit

Advanced 2-Wire Serial E²PROM with Block Lock™ Protection

FEATURES

- **2.7V to 5.5V Power Supply**
- **Low Power CMOS**
  - **—Active Read Current Less Than 1mA**
  - **—Active Write Current Less Than 3mA**
  - **—Standby Current Less Than 1μA**
- **Internally Organized 8192 x 8**
- **New Programmable Block Lock Protection**
  - **—Software Write Protection**
  - **—Programmable hardware Write Protect**
- **Block Lock (0, 1/4, 1/2, or all of the E²PROM array)**
- **2 Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **32 Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5ms**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**
- **Available Packages**
  - **—8-Lead PDIP**
  - **—8-Lead SOIC (JEDEC)**
  - **—14-Lead SOIC (JEDEC)**
  - **—20-Lead TSSOP**

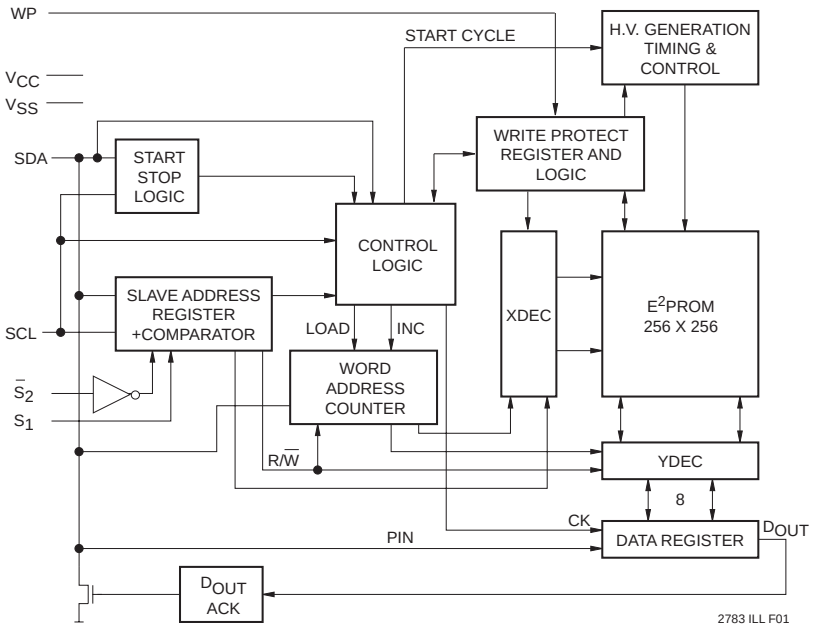
DESCRIPTION

The X24645 is a CMOS 65,536-bit serial E²PROM, internally organized 8192 x 8. The X24645 features a serial interface and software protocol allowing operation on a simple two wire bus.

Two device select inputs (S_1, $\overline{S}_2$) allow up to four devices to share a common two wire bus.

A Write Protect Register at the highest address location, 1FFFh, provides three new write protection features: Software Write Protect, Block Write Protect, and Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the X24645 until the WEL bit in the write protect register is set. The Block Write Protection feature allows the user to individually write protect four blocks of the array by programming two bits in the write protect register. The Programmable Hardware Write Protect feature allows the user to install the X24645 with WP tied to V_{CC}, program the entire memory array in place, and then enable the hardware write protection by programming a WPEN bit in the write protect register. After this, selected blocks of the array, including the write protect register itself, are permanently write protected, as long as WP remains HIGH.

FUNCTIONAL DIAGRAM



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Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_1, $\overline{S}_2$)

The device select inputs (S_1, $\overline{S}_2$) are used to set the first and second bits of the 8-bit slave address. This allows up to four X24645 devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}).

Write Protect (WP)

The write protect input controls the hardware write protect feature. When held LOW, hardware write protection is disabled and the X24645 can be written normally. When this input is held HIGH, and the WPEN bit in the write protect register is set HIGH, write protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the write protect register itself.

PIN NAMES

Symbol	Description
S_1, $\overline{S}_2$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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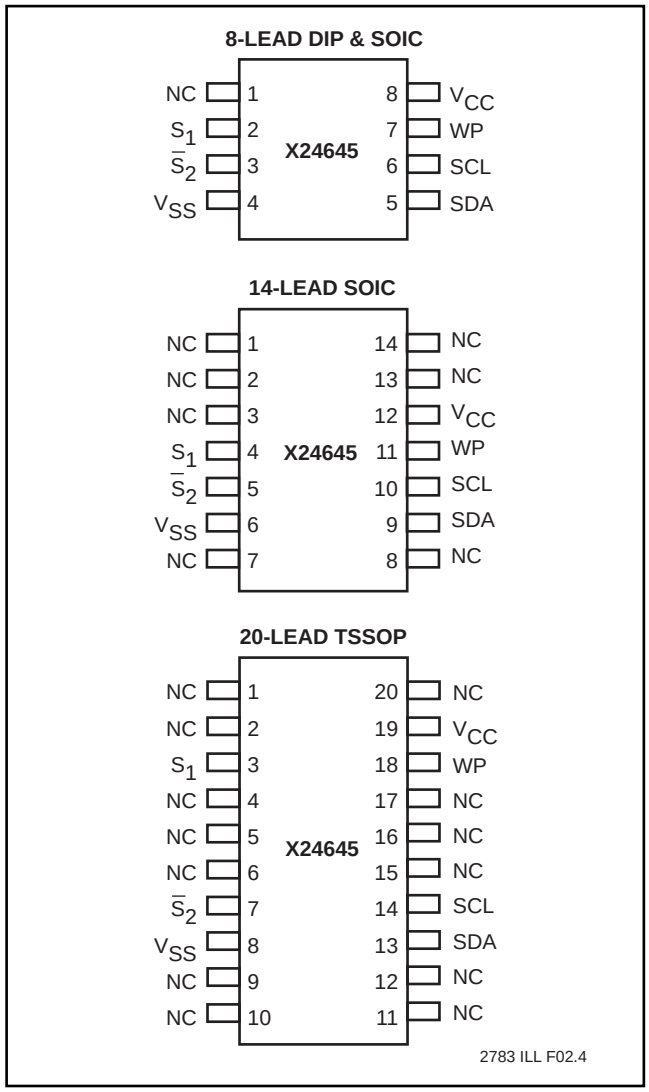
PIN CONFIGURATIONS



DEVICE OPERATION

The X24645 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24645 will be considered a slave in all applications.

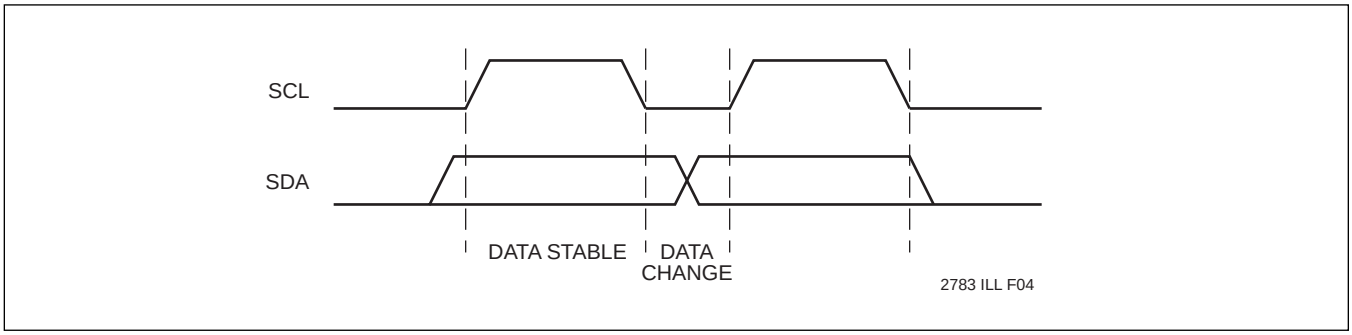
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

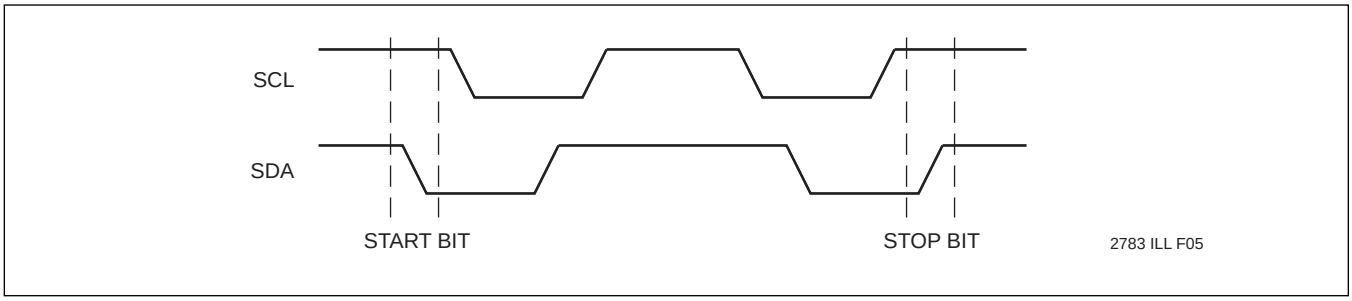
All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24645 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V)
(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

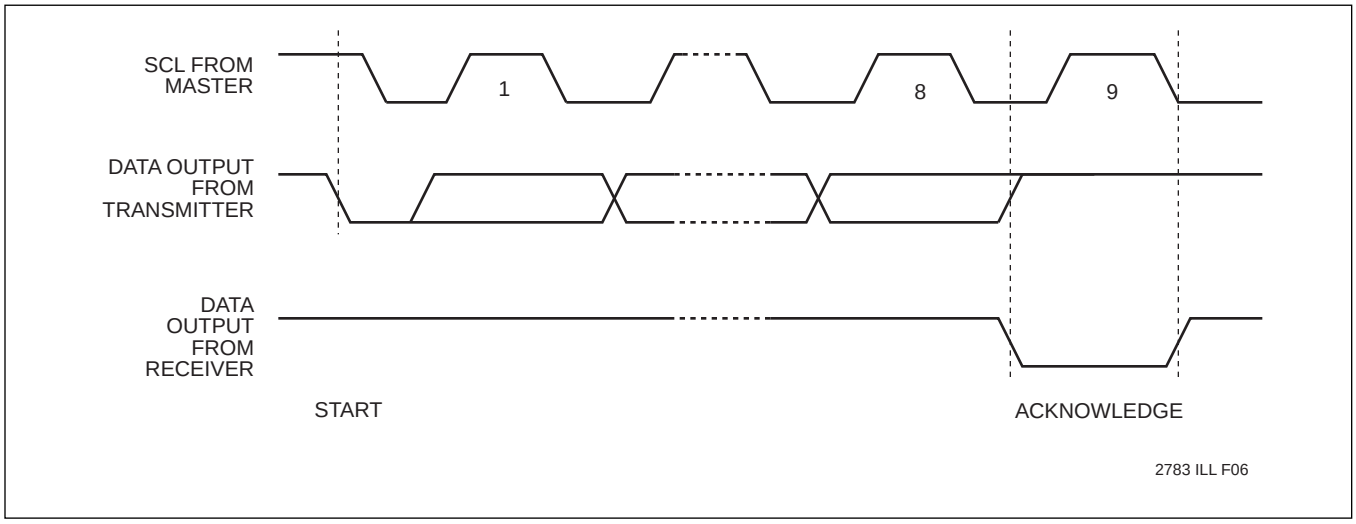
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24645 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24645 will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode the X24645 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24645 will continue to transmit data. If an acknowledge is not detected, the X24645 will terminate further data transmissions. The master must then issue a stop condition to return the X24645 to the standby power mode and place the device into a known state.

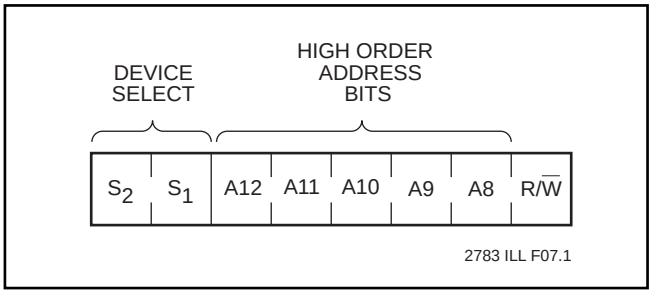
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing (see Figure 4). The next two bits are the device select bits. A system could have up to four X24645's on the bus. The four addresses are defined by the state of the S_1 and $\overline{S}_2$ inputs. S_2 of the slave address must be the inverse of the $\overline{S}_2$ input pin.

Figure 4. Slave Address



The next five bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the byte address field, providing direct access to the whole 8192 x 8 array.

The last bit of the slave address defines the operation to be performed. When set HIGH a read operation is selected, when set LOW, a write operation is selected.

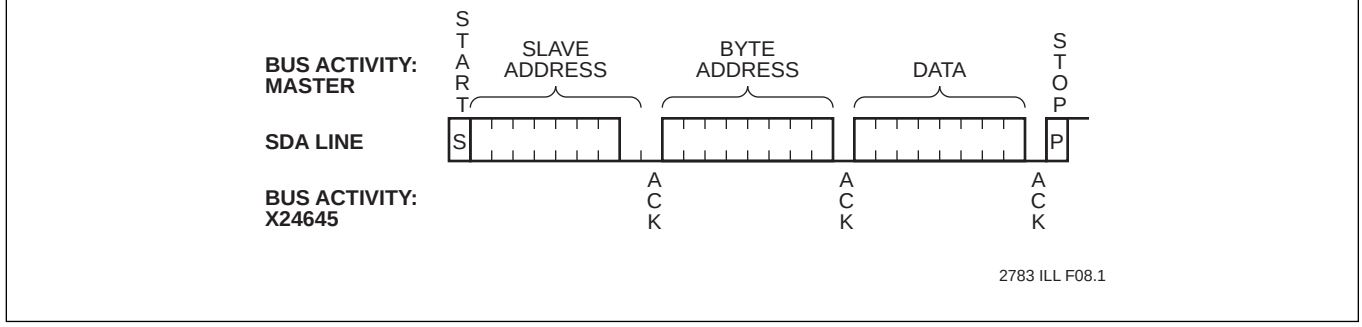
Following the start condition, the X24645 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24645 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24645 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24645 requires a second address field. This address field is the byte address, comprised of eight bits, providing access to any one of 8192 words in the array. Upon receipt of the byte address, the X24645 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24645 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24645 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



Page Write

The X24645 is capable of a 32-byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to thirty-one more bytes. After the receipt of each byte, the X24645 will respond with an acknowledge.

After the receipt of each byte, the five low order address bits are internally incremented by one. The high order eight bits of the address remain constant. If the master should transmit more than 32 bytes prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge, and data transfer sequence.

Acknowledge Polling

The Max Write Cycle Time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle, then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

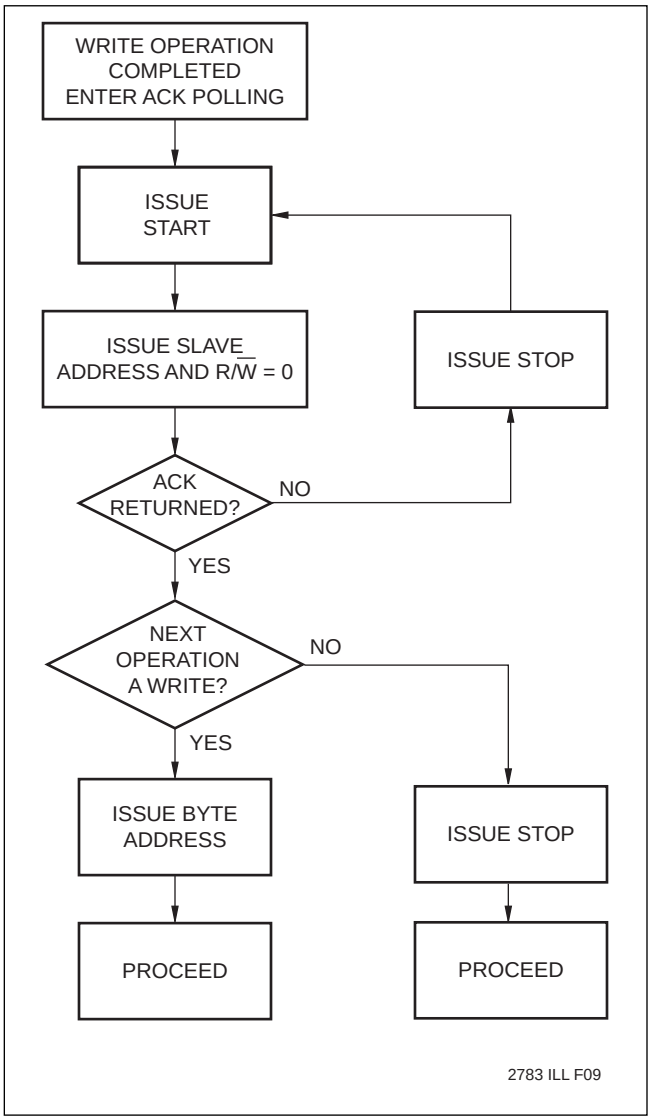
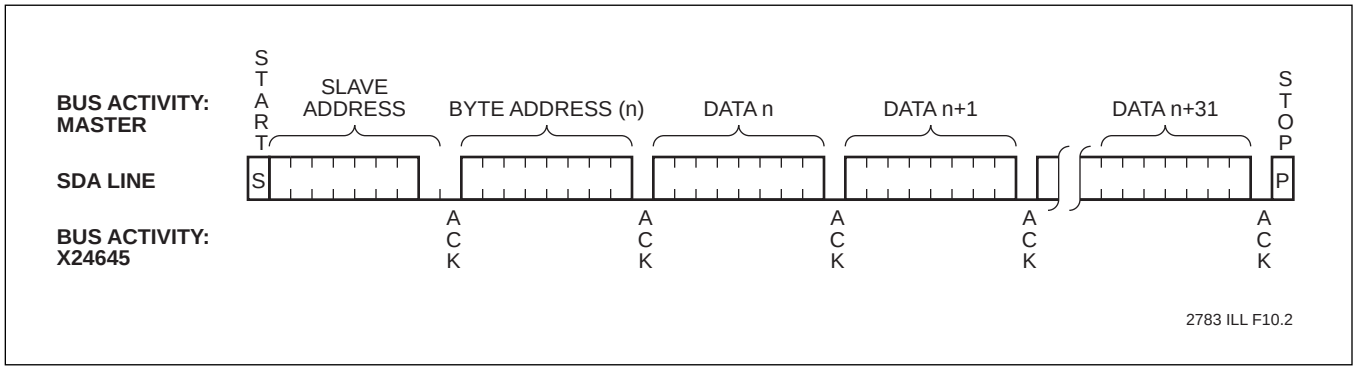


Figure 6. Page Write



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set HIGH. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24645 contains an address counter that maintains the address of the last byte read, incremented by one or the exact address of the last byte written. Therefore, if the last access read was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ set HIGH, the X24645 issues an acknowledge and transmits the byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set HIGH, the master must first perform a “dummy” write operation. The master issues the start condition, and the slave address with the R/$\overline{W}$ bit set LOW, followed by the byte address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set HIGH. This will be followed by an acknowledge from the X24645 and then by the data byte. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

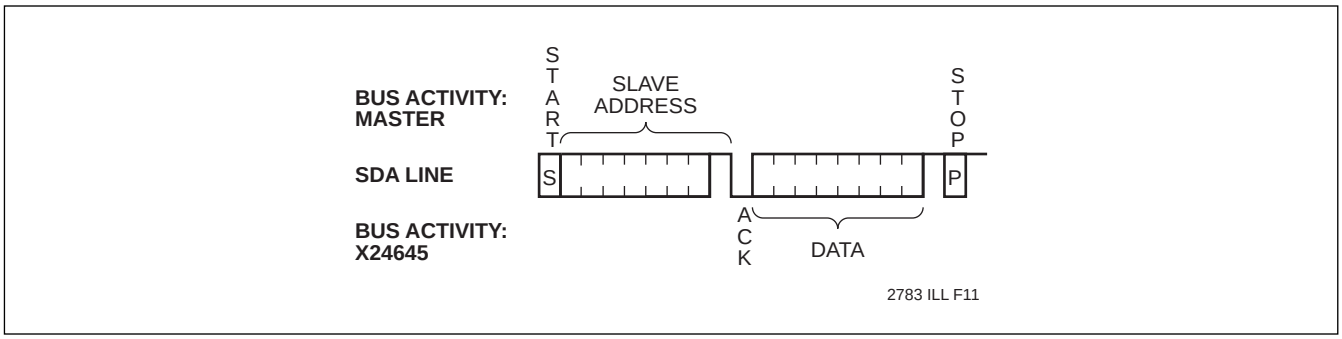
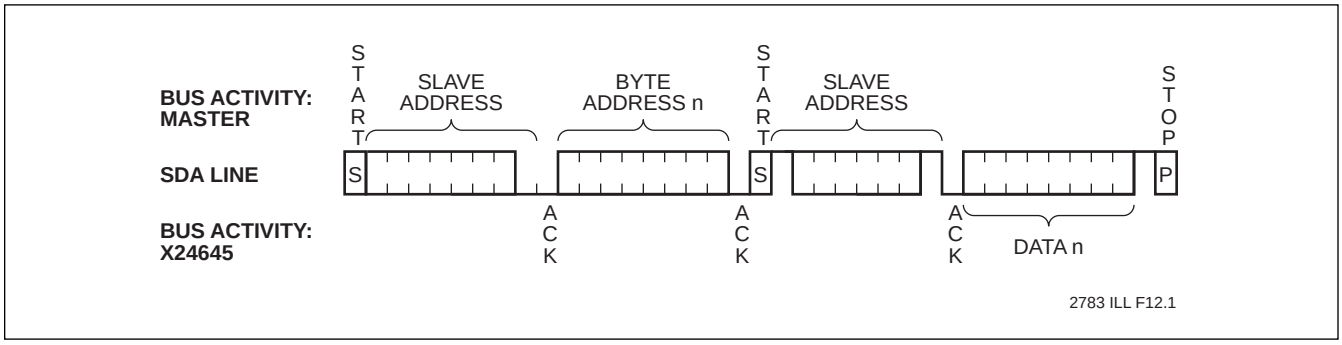


Figure 8. Random Read



Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first byte is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24645 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 8191), the counter “rolls over” to 0 and the X24645 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

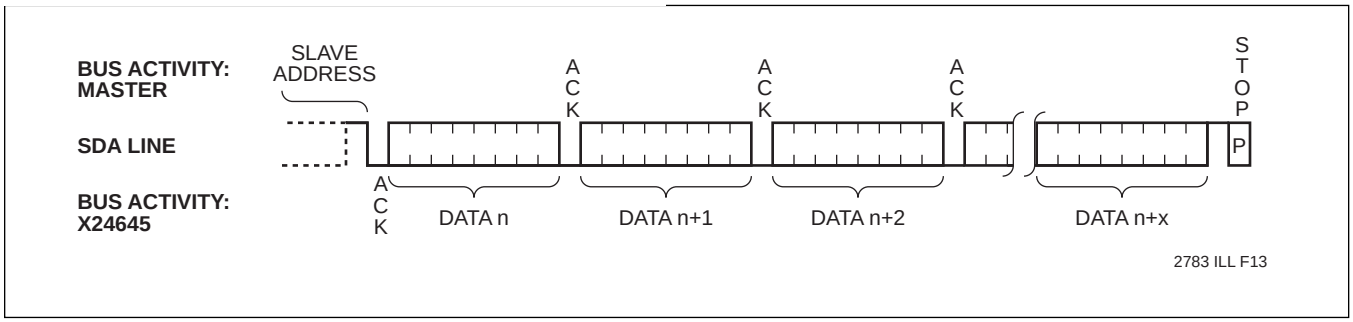
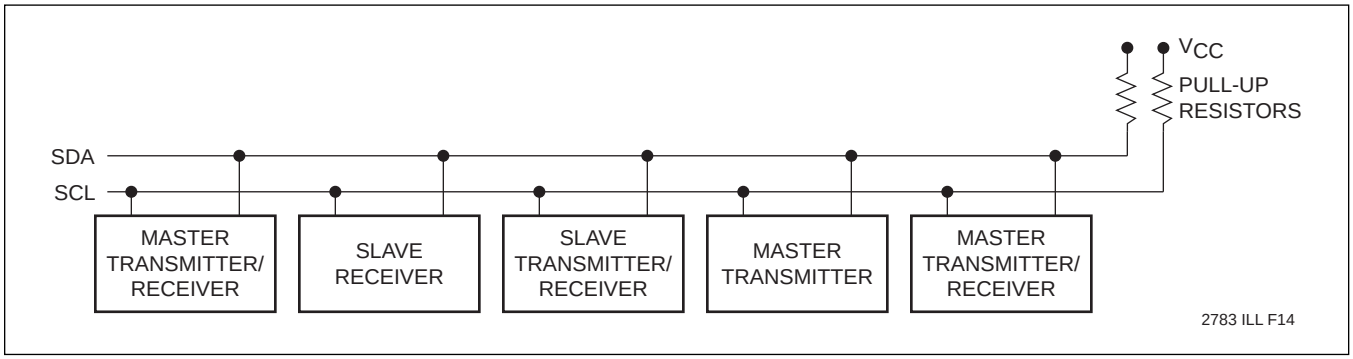


Figure 10. Typical System Configuration



WRITE PROTECT REGISTER

The Write Protect Register (WPR) is located at the highest address, 1FFFh.

Figure 11. Write Protect Register

WPR (ADDR = 1FFFh)

7	6	5	4	3	2	1	0
WPEN	0	0	BP1	BP0	RWEL	WEL	0

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WPR.1 = WEL
– "Write Enable" Latch (Volatile)
0 = Write enable latch reset, writes disabled
1 = Write enable latch set, writes enabled

If WEL = "0" then "no ACK" after first byte of input data.

WPR.2 = RWEL
– "Register Write Enable" Latch (Volatile)
0 = Register write enable latch reset, writes disabled
1 = Register write enable latch set, writes enabled

WPR.3, WPR.4 = BP0, BP1
– Block Protect Bits (Nonvolatile)
(See Block Protect section for definition)

WPR.7 = WPEN
– Write Protect Enable Bit (Nonvolatile)
(See Hardware Write Protect section for definition)

Writing to the Write Protect Register

The Write Protect Register is written by performing a random write of one byte directly to address, 1FFFh. If a page write is performed starting with any address other than 1FFF, the byte in the array at address 1FFFh will be written instead of the Write Protect Register (assuming writes are not disabled by the block protect register).

The state of the Write Protect Register can be read by performing a random read at address 1FFFh at any time. If a sequential read starting at any other address than 1FFFh is performed, the contents of the byte in the array at 1FFFh is read out instead of the Write Protect Register.

WEL and RWEL are volatile latches that power-up in the LOW (disabled) state. A write to any address other than 1FFFh, where the Write Protect Register is located, will be ignored (no ack) until the WEL bit is set HIGH. The WEL bit is set by writing 0000001x to address 1FFFh. Once set, WEL remains HIGH until either reset (by writing 00000000 to 1FFFh) or until the part powers-up again. The RWEL bit controls writes to the block protect bits. RWEL is set by first setting WEL to "1" and then writing 0000011x to address 1FFFh. RWEL must be set in order to change the block protect bits, BP0 and BP1, or the WPEN bit. RWEL is reset when the block protect or WPEN bits are changed, or when the part powers-up again.

Programming the BP or WPEN Bits

A three step sequence is required to change the nonvolatile Block Protect or Write Protect Enable:

1) Set WEL = 1 (write 00000010 to address 1FFFh, volatile write cycle)

(Start)

2) Set RWEL = 1 (write 00000110 to address 1FFFh, volatile write cycle)

(Start)

3) Set BP1, BP0, and/or WPEN bits (Write w00yz010 to address 1FFFh)

w = WPEN, y = BP1, Z = BP0,

(Stop)

Step 3 is a nonvolatile write cycle, requiring 10ms to complete. RWEL is reset to "0" by this write cycle, requiring another write cycle to set RWEL again before the block protect bits can be changed. RWEL must be "0" in step 3; if w00yz110 is written to address 1FFFh, RWEL is set but WPEN, BP1 and BP0 are not changed (the device remains at step 2).

Block Protect Bits

The Block Protect Bits BP0 and BP1 determine which blocks of the memory are write-protected:

Table 1. Block Protect Bits

BP1	BP0	Protected Addresses	
0	0	None	
0	1	1800h–1FFFh	Upper 1/4
1	0	1000h–1FFFh	Upper 1/2
1	1	0000h–1FFFh	Full Array (WPR not included)

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Programmable Hardware Write Protect

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Write Protect Register control the programmable hardware write protect feature. Hardware write protection is enabled when the WP pin is HIGH and the WPEN bit is “1”, and disabled when either the WP pin is LOW or the WPEN bit is “0”. When the chip is hardware write-protected, nonvolatile writes are disabled to the Write Protect Register, including the BP bits and the WPEN bit itself, as well as to block-protected sections in the memory array. Only the sections of the memory array that are not block-protected can be written. Note that since the WPEN bit is write-protected, it cannot be changed back to a LOW state, and write protection is disabled as long as the the WP pin is held HIGH. Table 2 defines the write protection status for each state of WPEN and WP.

Table 2. Write Protect Status Table

WP	WPEN	Memory Array (Not Block Protected)	Memory Array (Block Protected)	BP Bits	WPEN Bit
L	X	Writable	Protected	Writable	Writable
X	0	Writable	Protected	Writable	Writable
H	1	Writable	Protected	Protected	Protected

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ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X24645 ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X24645	4.5V to 5.5V
X24645-2.7	2.7V to 5.5V

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D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		50	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 2.7V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA, V_{CC} = 4.5V

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_1, $\overline{S}_2$, SCL)	6	pF	V_{IN} = 0V

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Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5

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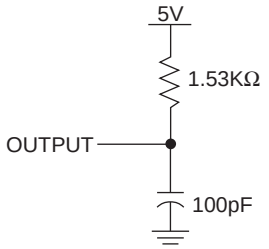
EQUIVALENT A.C. LOAD CIRCUIT



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A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

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POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

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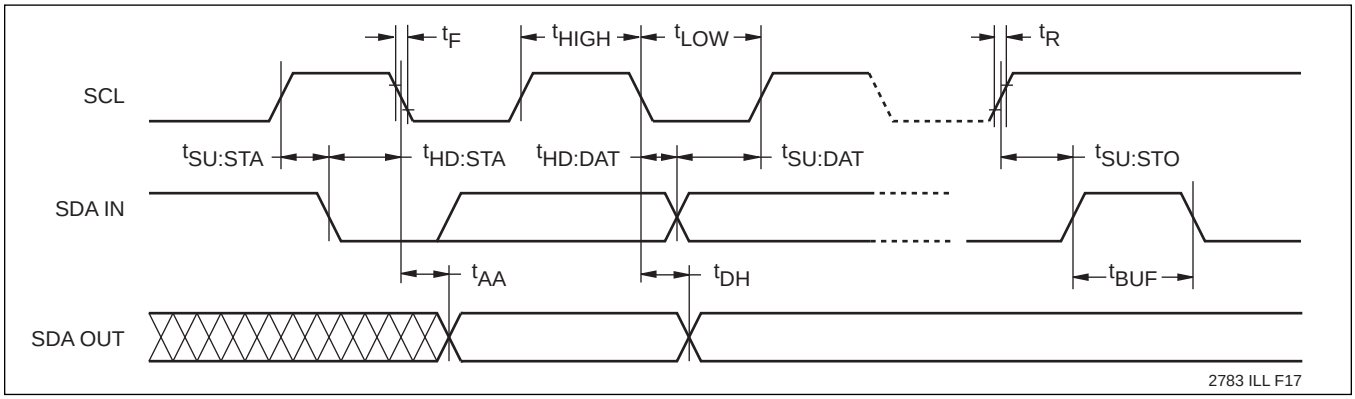
Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
T_{WR}(6)	Write Cycle Time		5	10	ms

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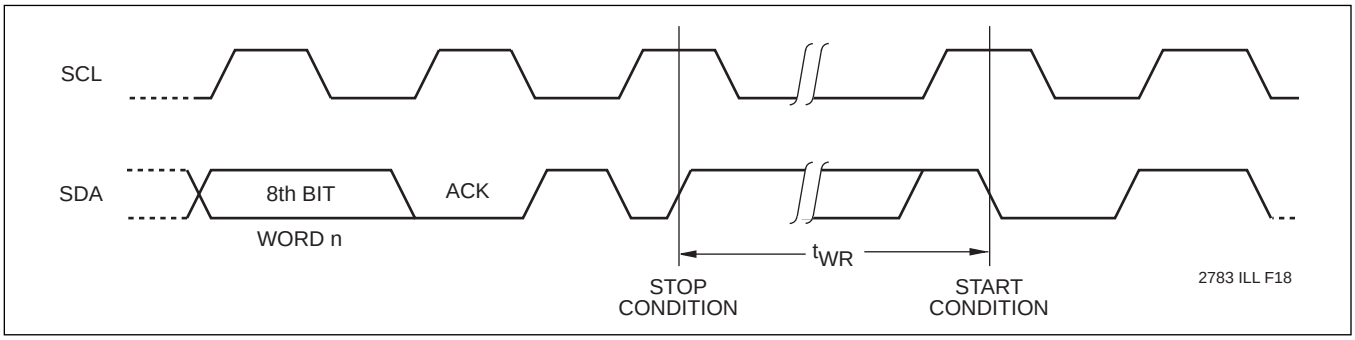
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24645 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

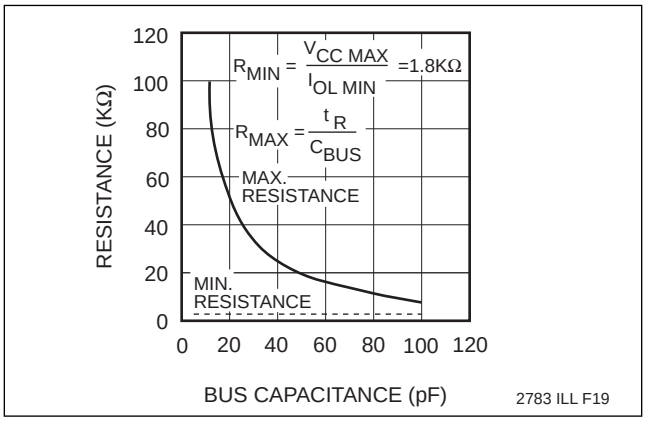
Bus Timing



Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

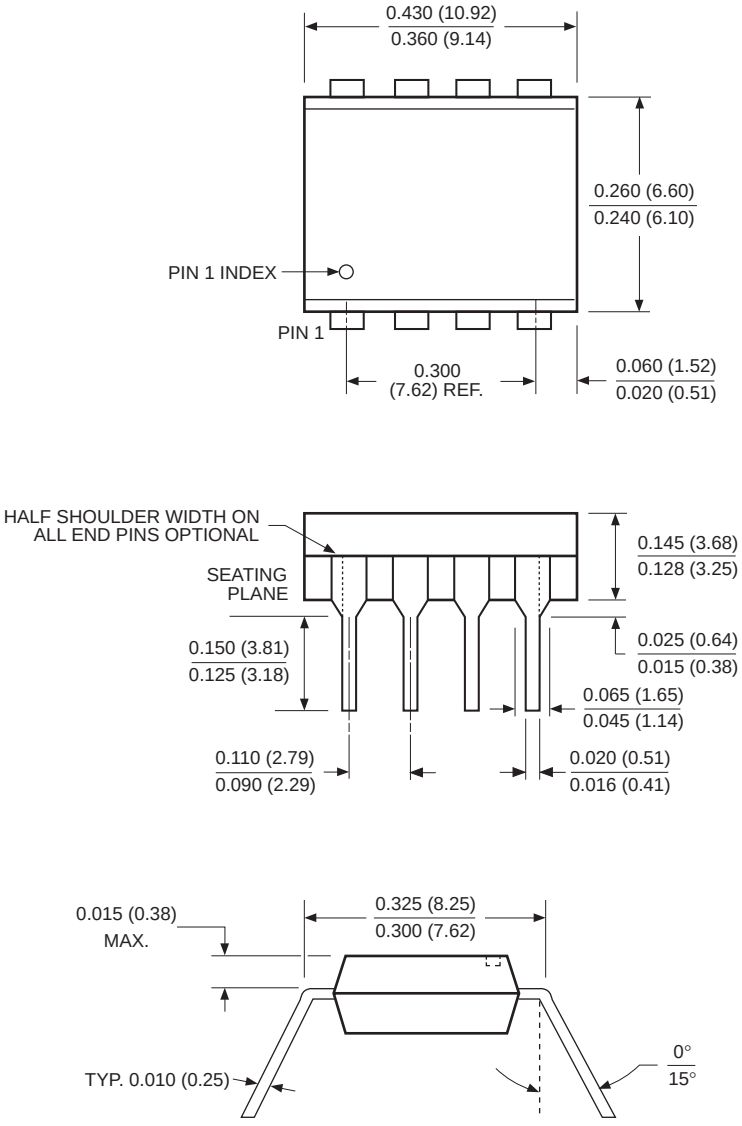


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



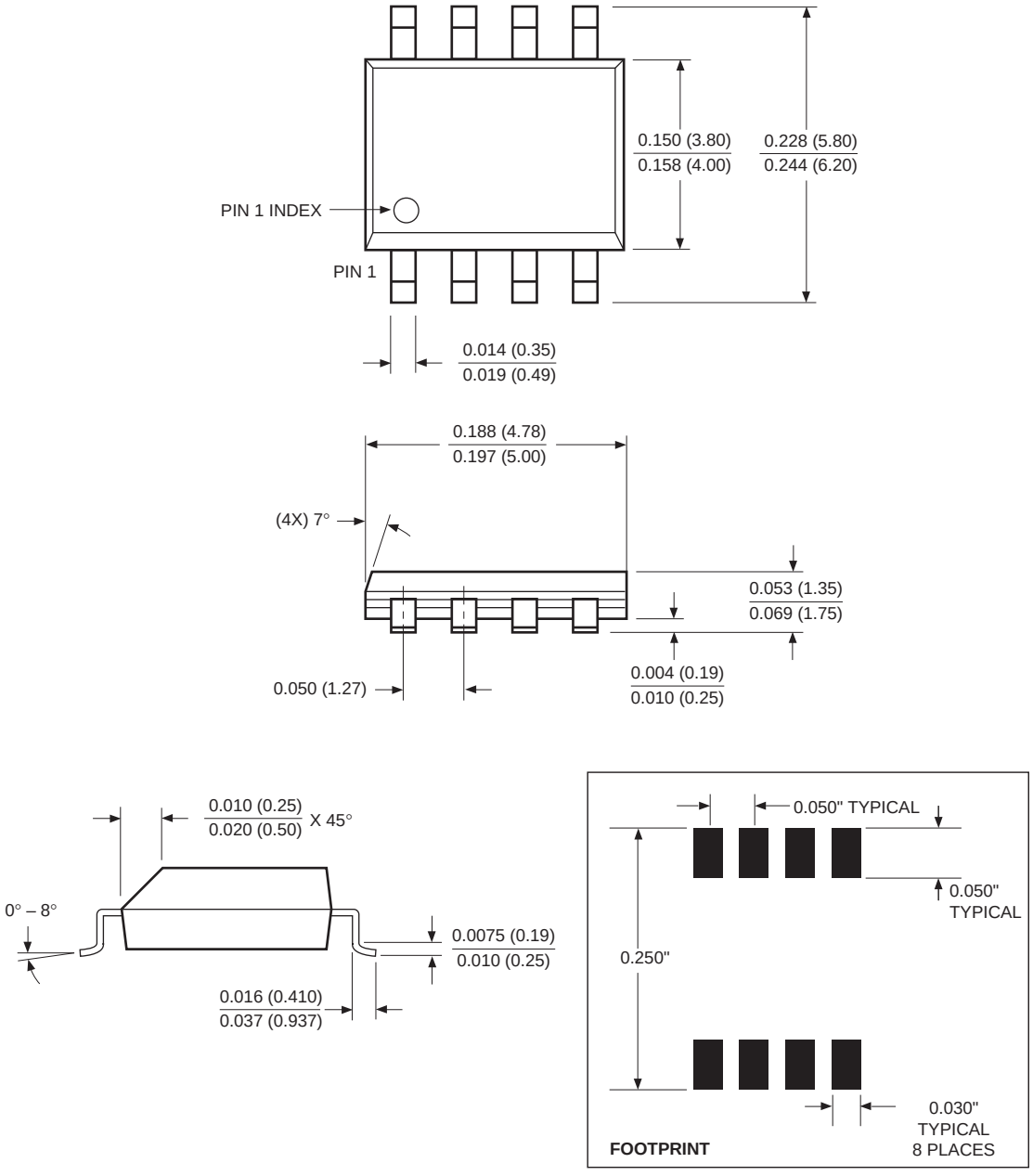
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F01

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

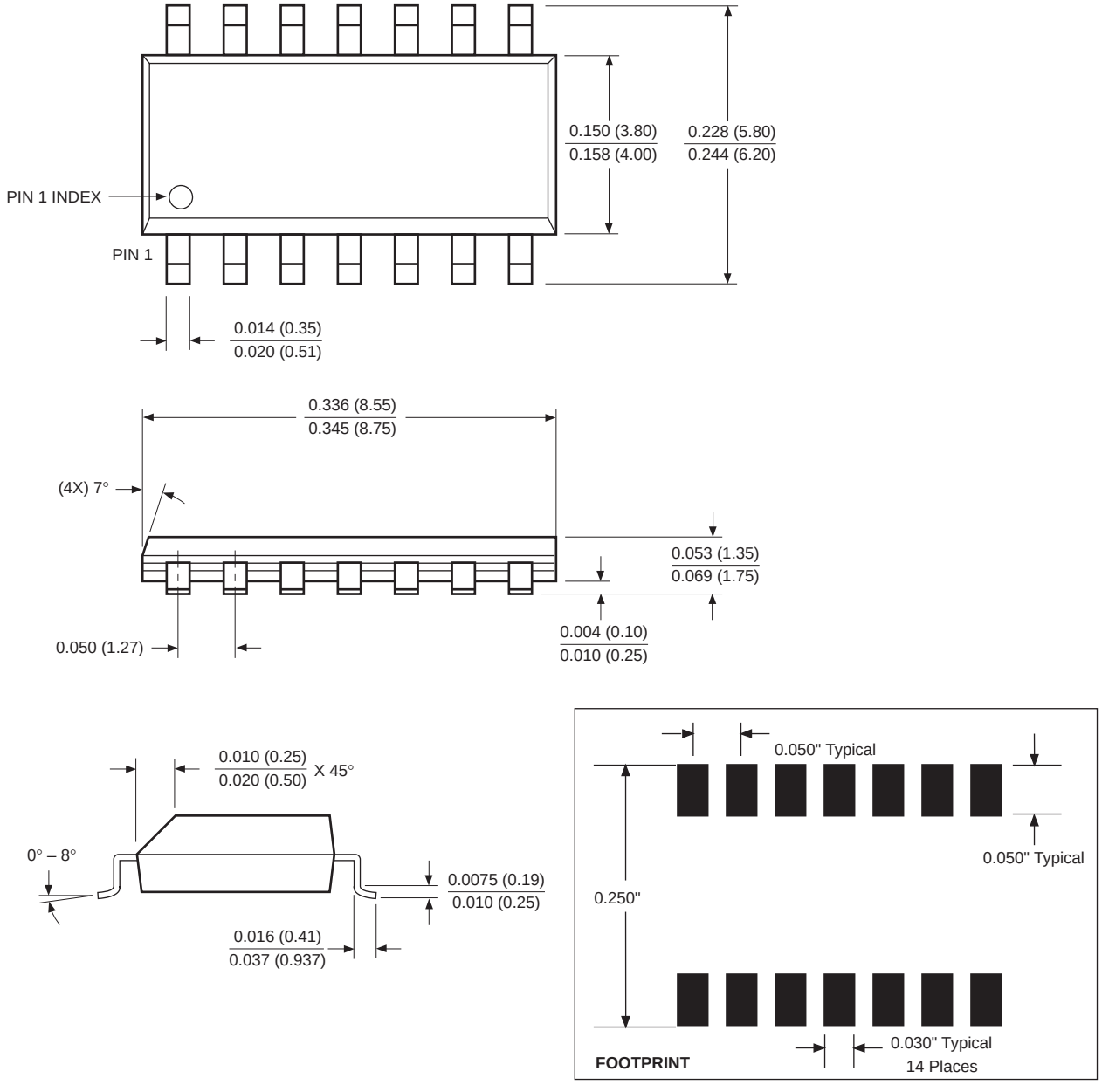


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F22.1

PACKAGING INFORMATION

14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

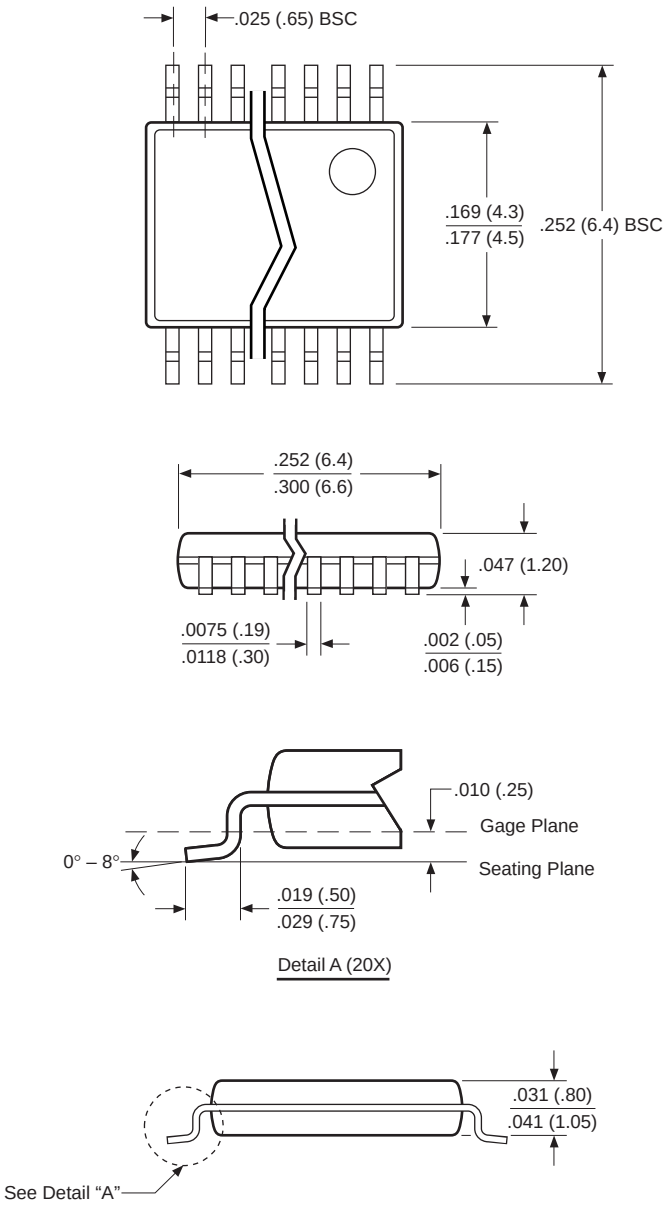


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F10.1

PACKAGING INFORMATION

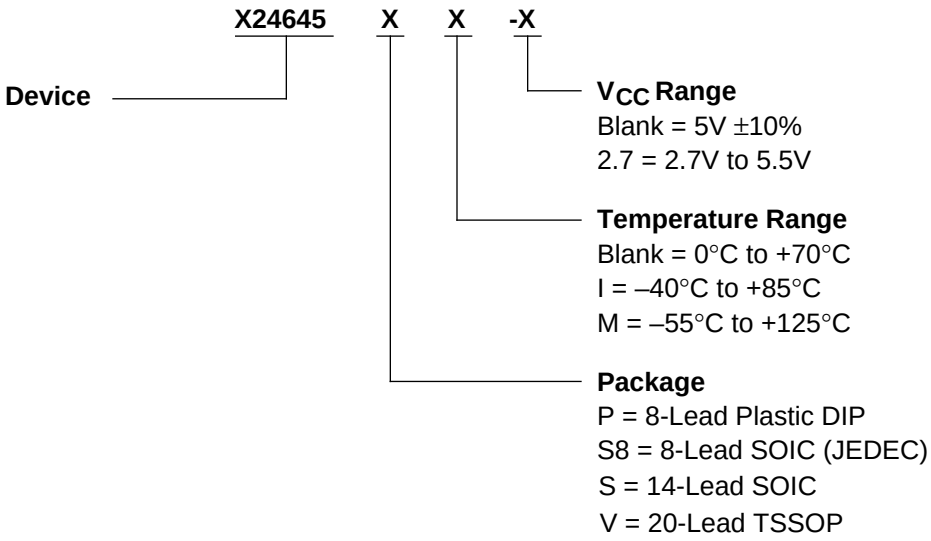
20-LEAD PLASTIC, TSSOP PACKAGE TYPE V



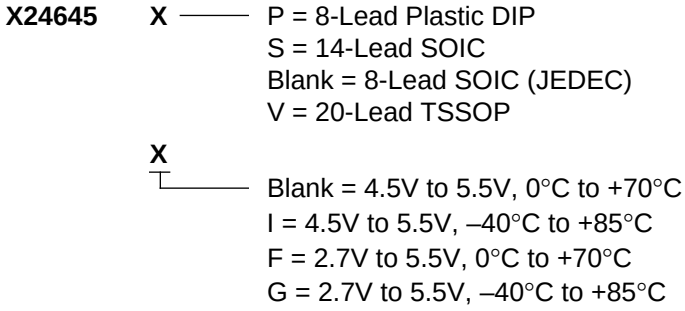
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F45

ORDERING INFORMATION



Part Mark Convention



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