64K	Commercial Industrial	X2864B X2864BI	8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- 120 ns Access Time
- High Performance Scaled NMOS Technology
- Fast Write Cycle Times
  - —32-Byte Page Write Operation
  - —Byte or Page Write Cycle: 3 ms Typical
  - —Complete Memory Rewrite: 750 ms Typical
  - —Effective Byte Write Cycle Time of 95 μs Typical
- $\overline{DATA}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{WE}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

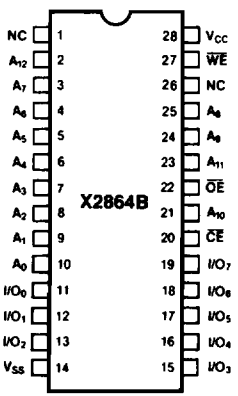
The Xicor X2864B is a 8K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

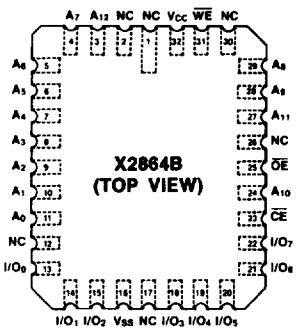
PIN CONFIGURATIONS

PLASTIC CERDIP FLAT PACK



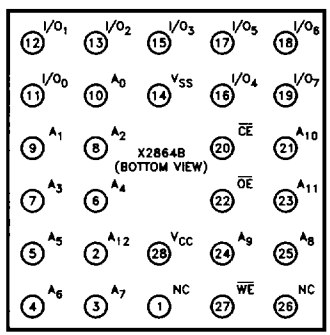
0031-1

PLCC LCC



0031-2

PGA



0031-11

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864B ..... −10°C to +85°C
X2864BI ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864B T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

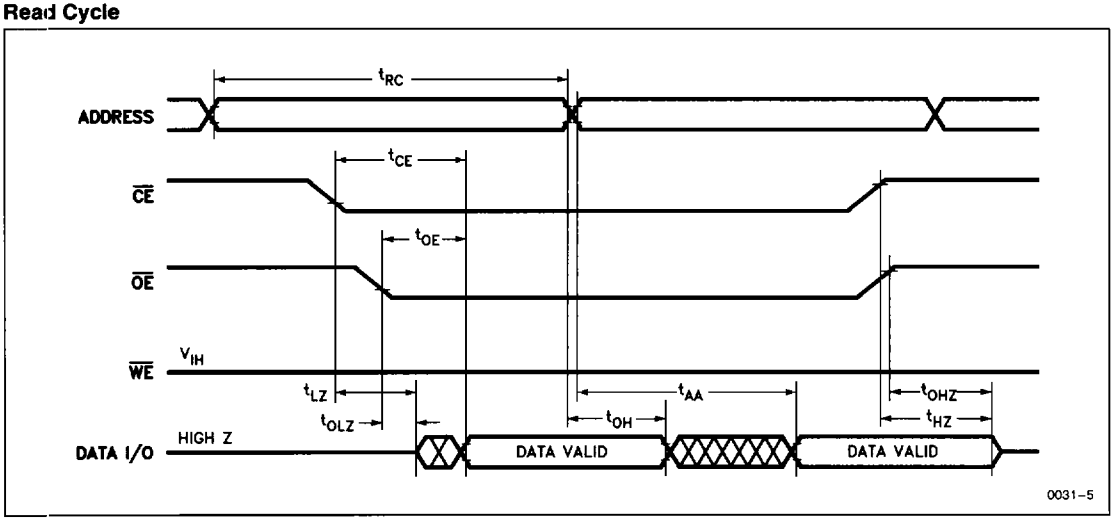
A.C. CHARACTERISTICS

X2864B T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864B-12 X2864BI-12		X2864B-15 X2864BI-15		X2864B-18 X2864BI-18		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		180		ns
t_{CE}	Chip Enable Access Time		120		150		180	ns
t_{AA}	Address Access Time		120		150		180	ns
t_{OE}	Output Enable Access Time		50		70		100	ns
t_{LZ}[4]	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}[4]	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}[5]	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OHZ}[5]	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle



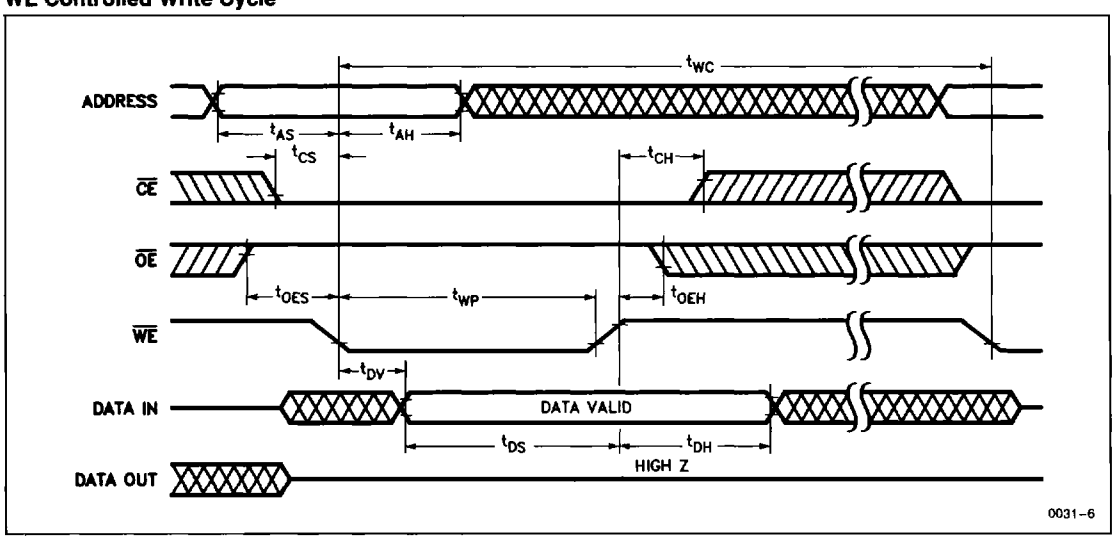
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

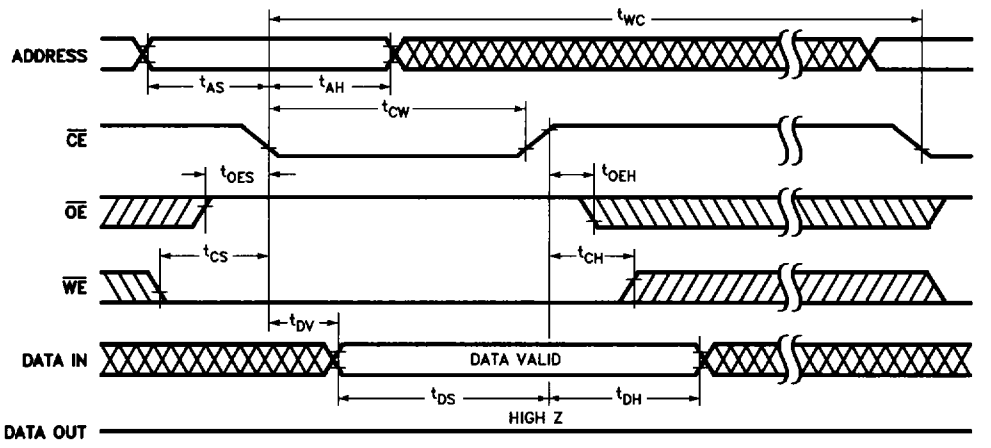
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	5			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			100	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	5			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

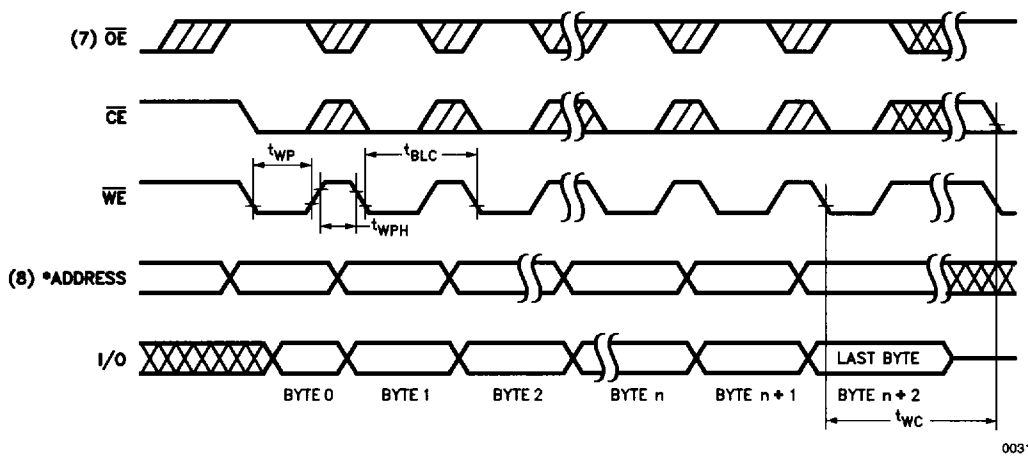


Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

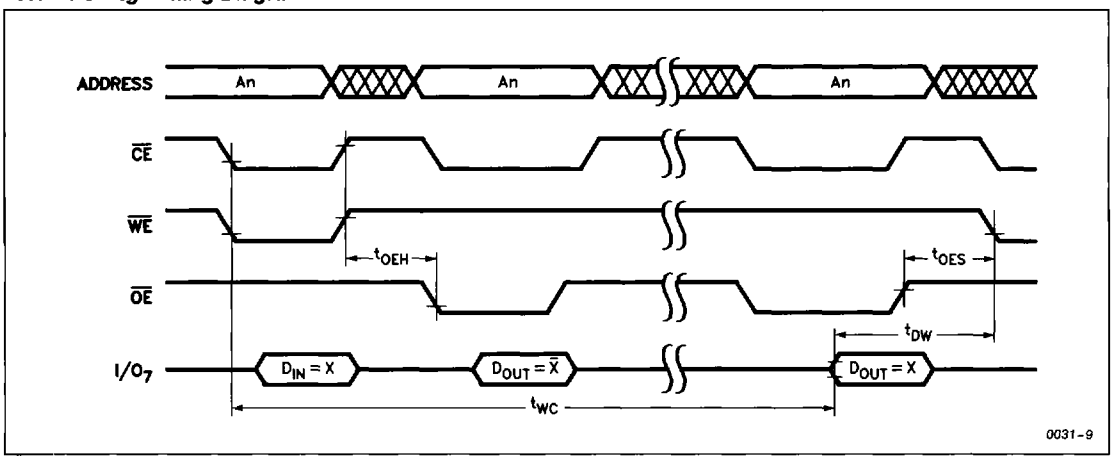


*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864B through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide so long as the host continues to access the device within the byte load cycle time of 100 μs.

$\overline{DATA}$ Polling

The X2864B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3.5V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

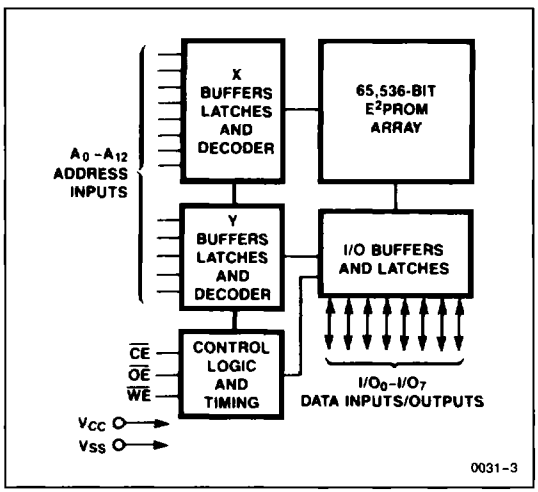
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BP-12	8192 x 8		•									†	120 ns	NMOS	Standard
X2864BP-15	8192 x 8		•									†	150 ns	NMOS	Standard
X2864BP-18	8192 x 8		•									†	180 ns	NMOS	Standard
X2864BPI-12	8192 x 8		•									I	120 ns	NMOS	Standard
X2864BPI-15	8192 x 8		•									I	150 ns	NMOS	Standard
X2864BPI-18	8192 x 8		•									I	180 ns	NMOS	Standard
X2864BD-12	8192 x 8			•								†	120 ns	NMOS	Standard
X2864BD-15	8192 x 8			•								†	150 ns	NMOS	Standard
X2864BD-18	8192 x 8			•								†	180 ns	NMOS	Standard
X2864BDI-12	8192 x 8			•								I	120 ns	NMOS	Standard
X2864BDI-15	8192 x 8			•								I	150 ns	NMOS	Standard
X2864BDI-18	8192 x 8			•								I	180 ns	NMOS	Standard
X2864BF-12	8192 x 8					•						†	120 ns	NMOS	Standard
X2864BF-15	8192 x 8					•						†	150 ns	NMOS	Standard
X2864BF-18	8192 x 8					•						†	180 ns	NMOS	Standard
X2864BFI-12	8192 x 8					•						I	120 ns	NMOS	Standard
X2864BFI-15	8192 x 8					•						I	150 ns	NMOS	Standard
X2864BFI-18	8192 x 8					•						I	180 ns	NMOS	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BK-12	8192 x 8							•				†	120 ns	NMOS	Standard
X2864BK-15	8192 x 8							•				†	150 ns	NMOS	Standard
X2864BK-18	8192 x 8							•				†	180 ns	NMOS	Standard
X2864BKI-12	8192 x 8							•				I	120 ns	NMOS	Standard
X2864BKI-15	8192 x 8							•				I	150 ns	NMOS	Standard
X2864BKI-18	8192 x 8							•				I	180 ns	NMOS	Standard
X2864BJ-12	8192 x 8								•			†	120 ns	NMOS	Standard
X2864BJ-15	8192 x 8								•			†	150 ns	NMOS	Standard
X2864BJ-18	8192 x 8								•			†	180 ns	NMOS	Standard
X2864BJI-12	8192 x 8								•			I	120 ns	NMOS	Standard
X2864BJI-15	8192 x 8								•			I	150 ns	NMOS	Standard
X2864BJI-18	8192 x 8								•			I	180 ns	NMOS	Standard
X2864BE-12	8192 x 8									•		†	120 ns	NMOS	Standard
X2864BE-15	8192 x 8									•		†	150 ns	NMOS	Standard
X2864BE-18	8192 x 8									•		†	180 ns	NMOS	Standard
X2864BEI-12	8192 x 8									•		I	120 ns	NMOS	Standard
X2864BEI-15	8192 x 8									•		I	150 ns	NMOS	Standard
X2864BEI-18	8192 x 8									•		I	180 ns	NMOS	Standard

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ORDERING INFORMATION

64K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BG-12	8192 x 8										•	†	120 ns	NMOS	Standard
X2864BG-15	8192 x 8										•	†	150 ns	NMOS	Standard
X2864BG-18	8192 x 8										•	†	180 ns	NMOS	Standard
X2864BGI-12	8192 x 8										•	I	120 ns	NMOS	Standard
X2864BGI-15	8192 x 8										•	I	150 ns	NMOS	Standard
X2864BGI-18	8192 x 8										•	I	180 ns	NMOS	Standard

Key:

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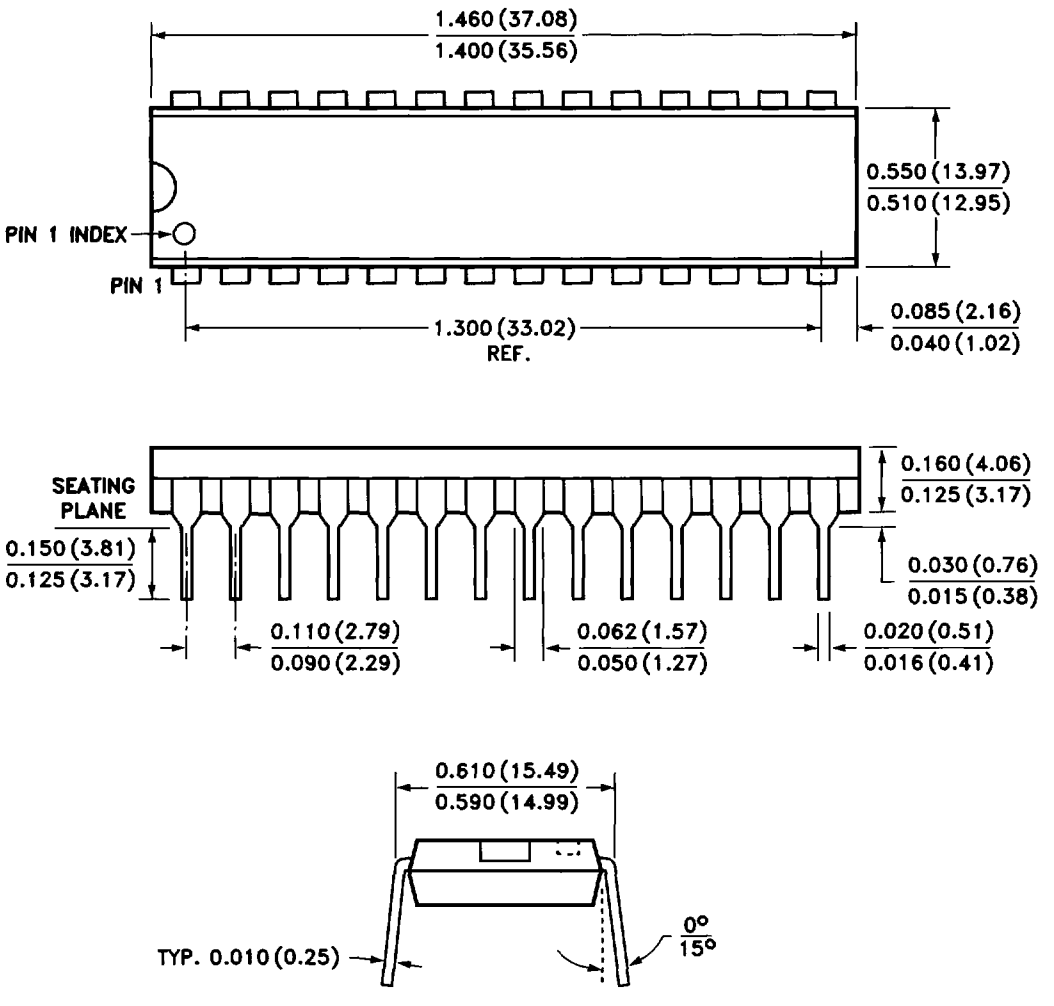
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

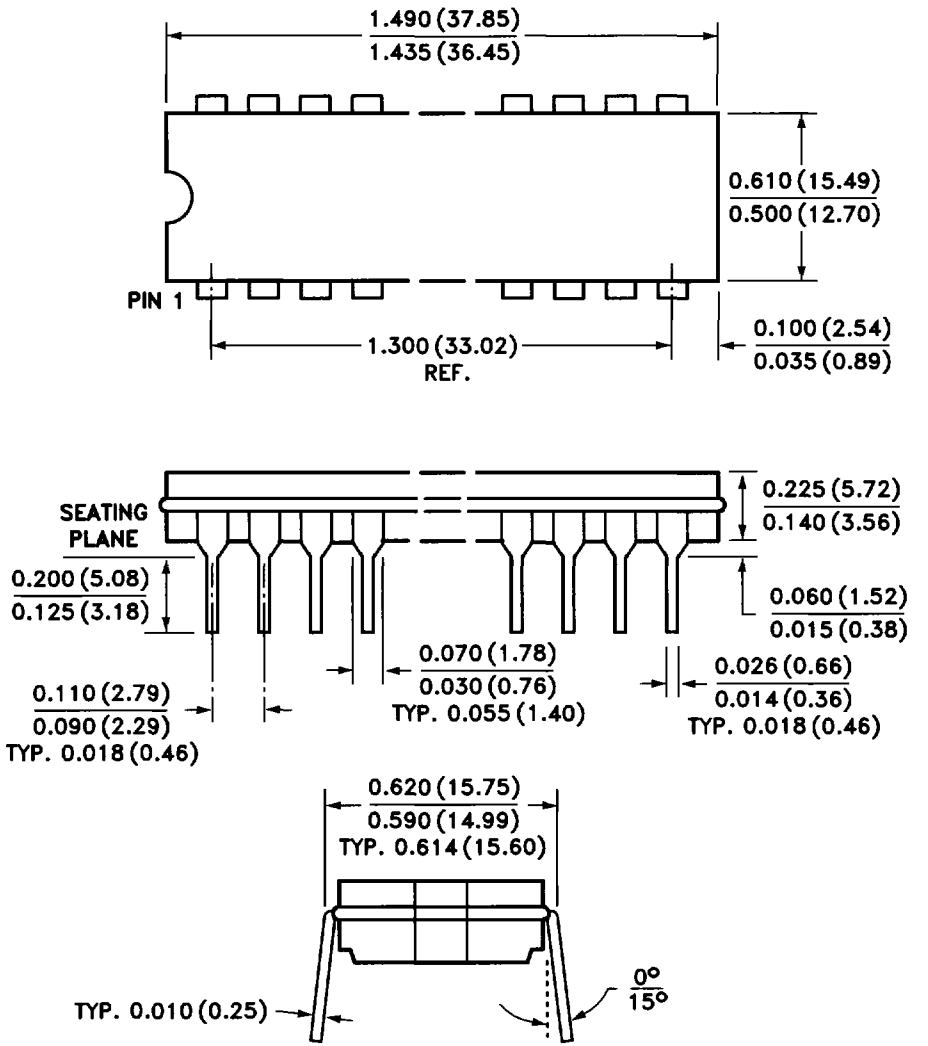


PPI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

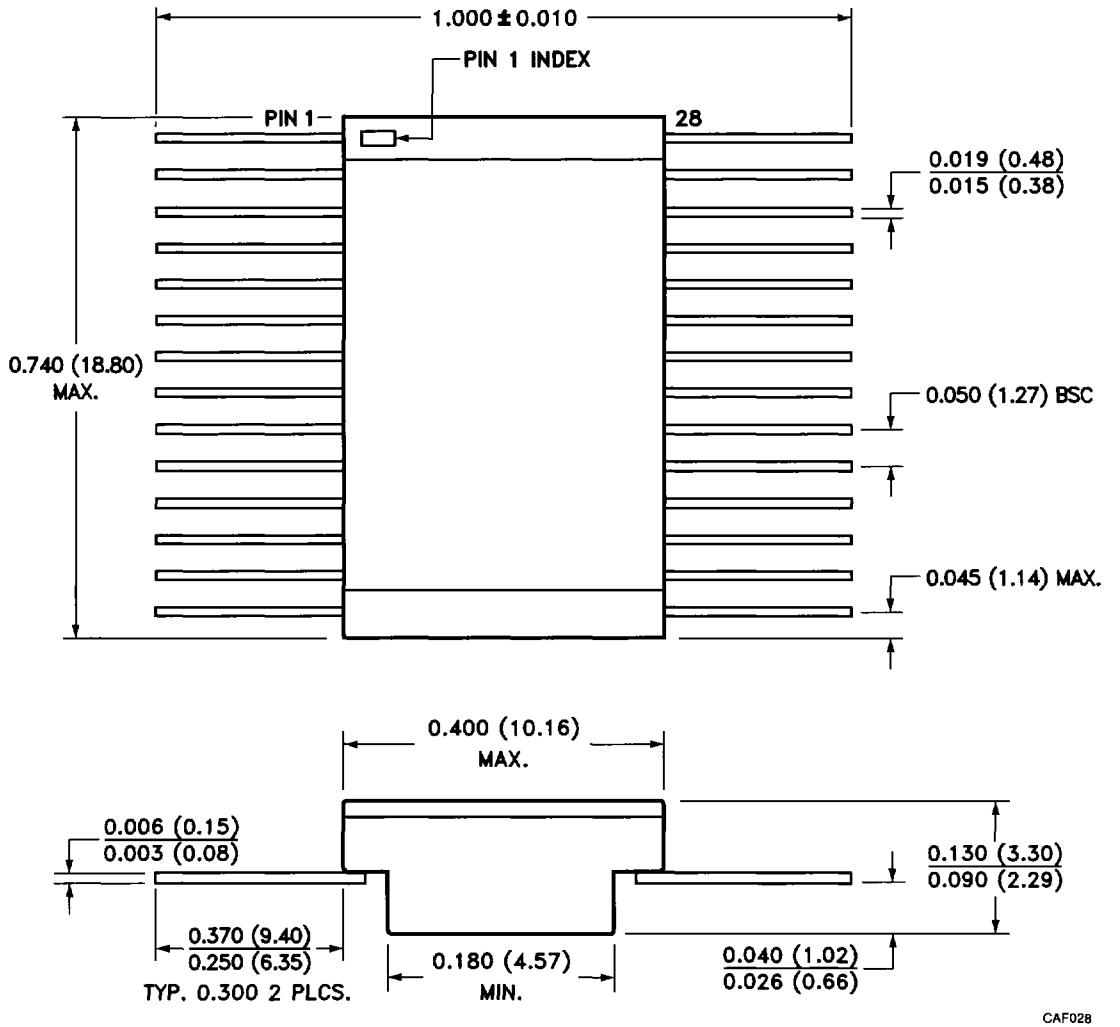


HDI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1



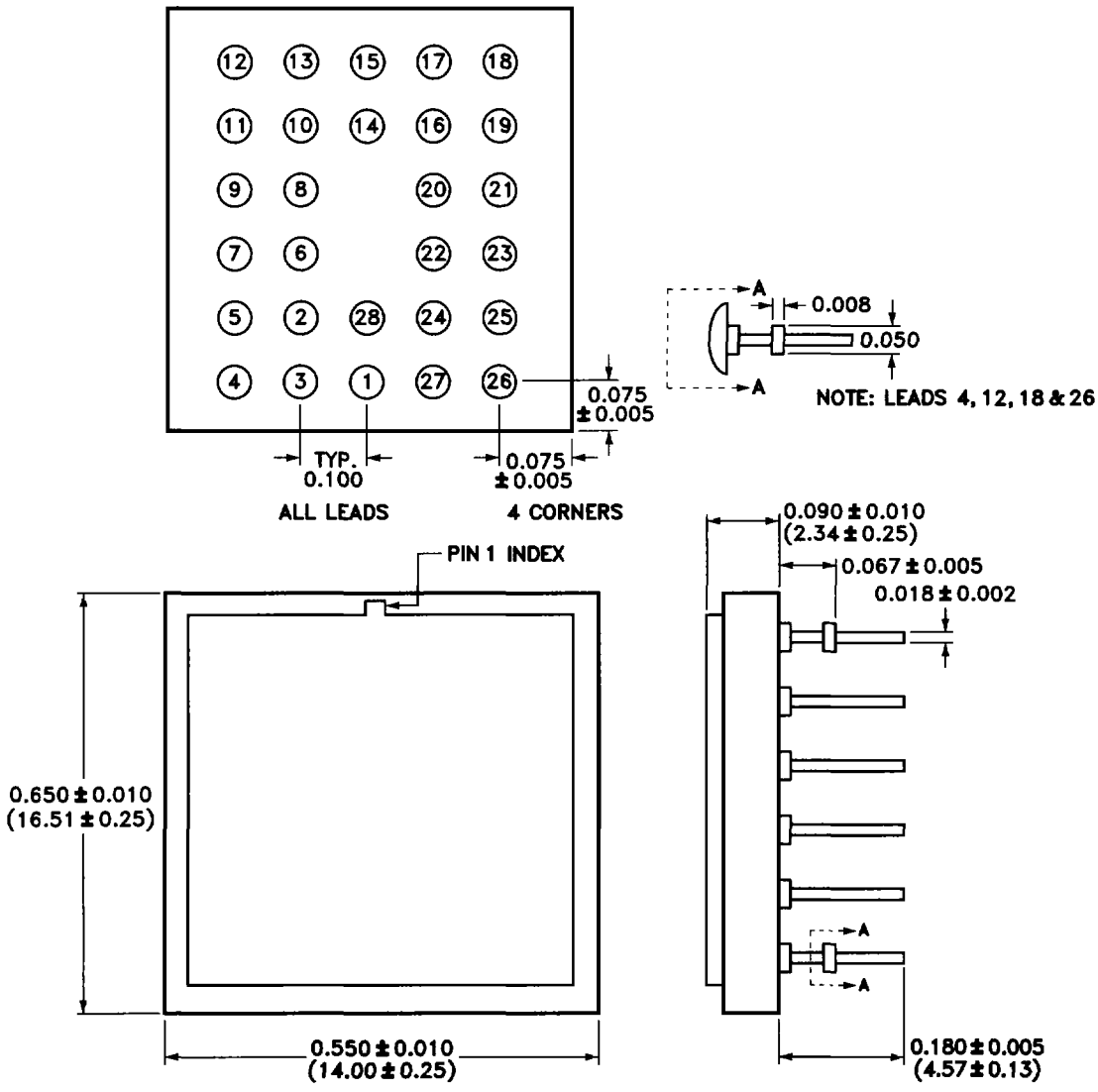
CAF028

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H

PACKAGING INFORMATION

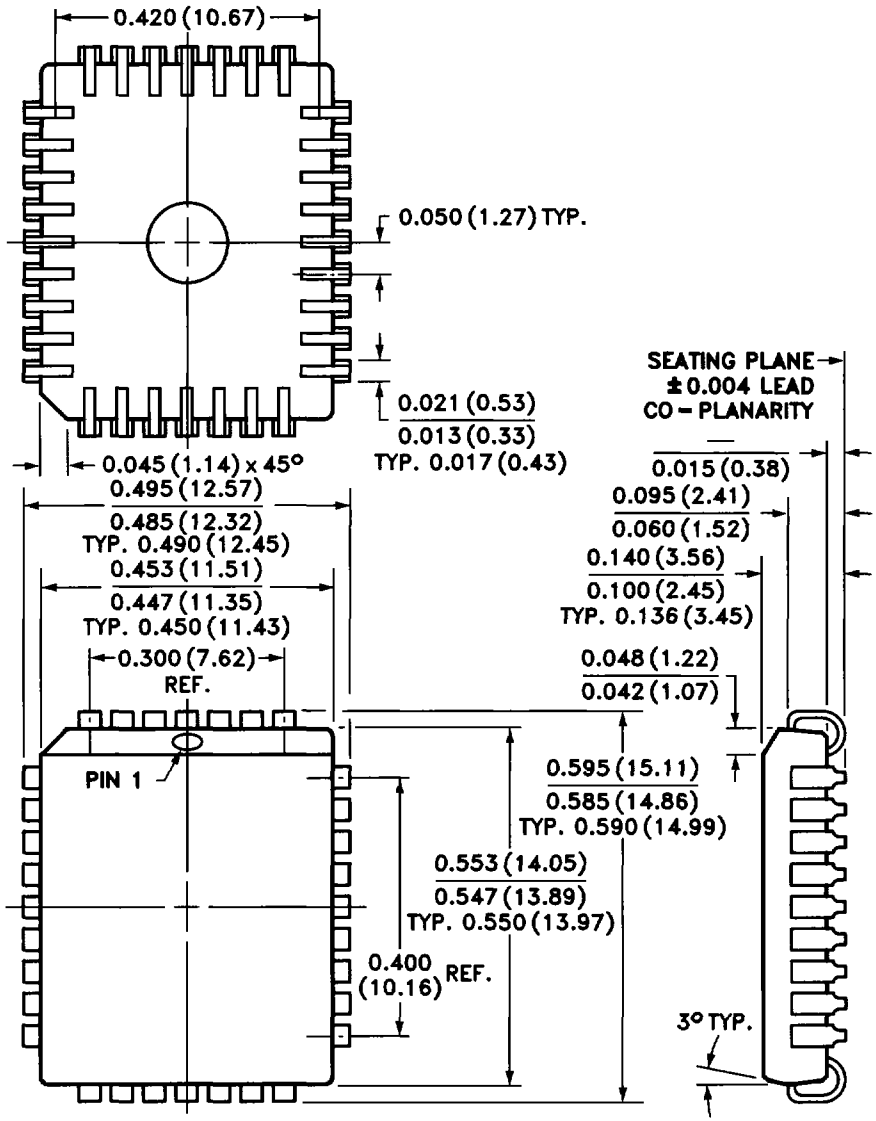
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



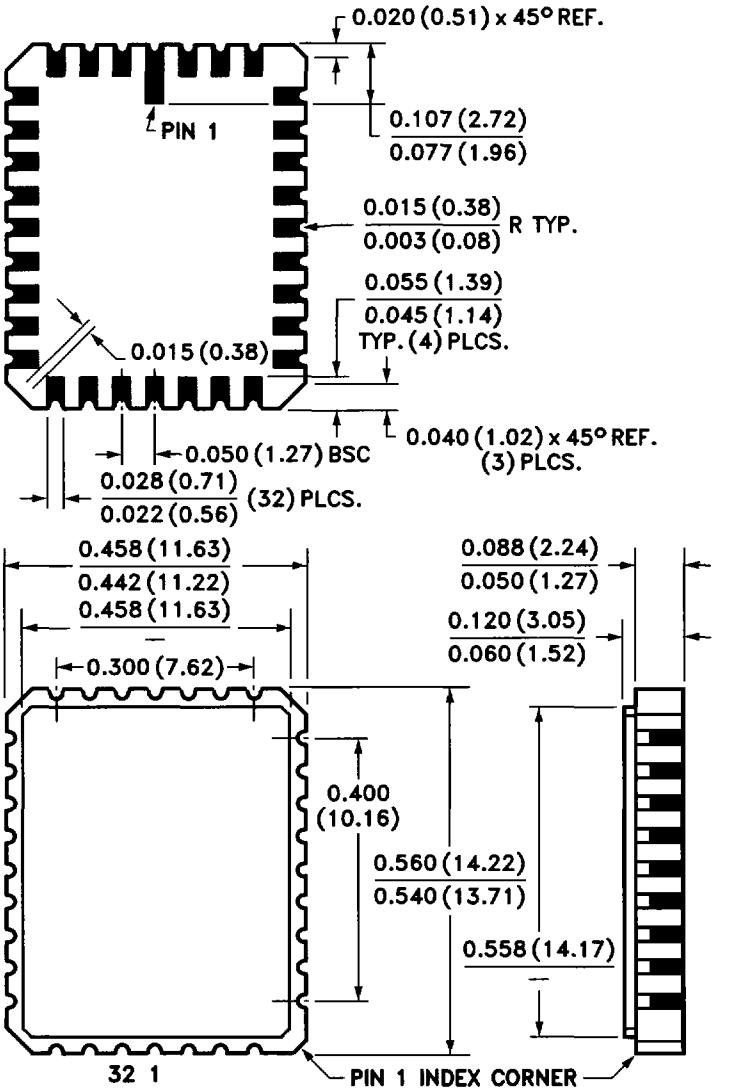
PJG032

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

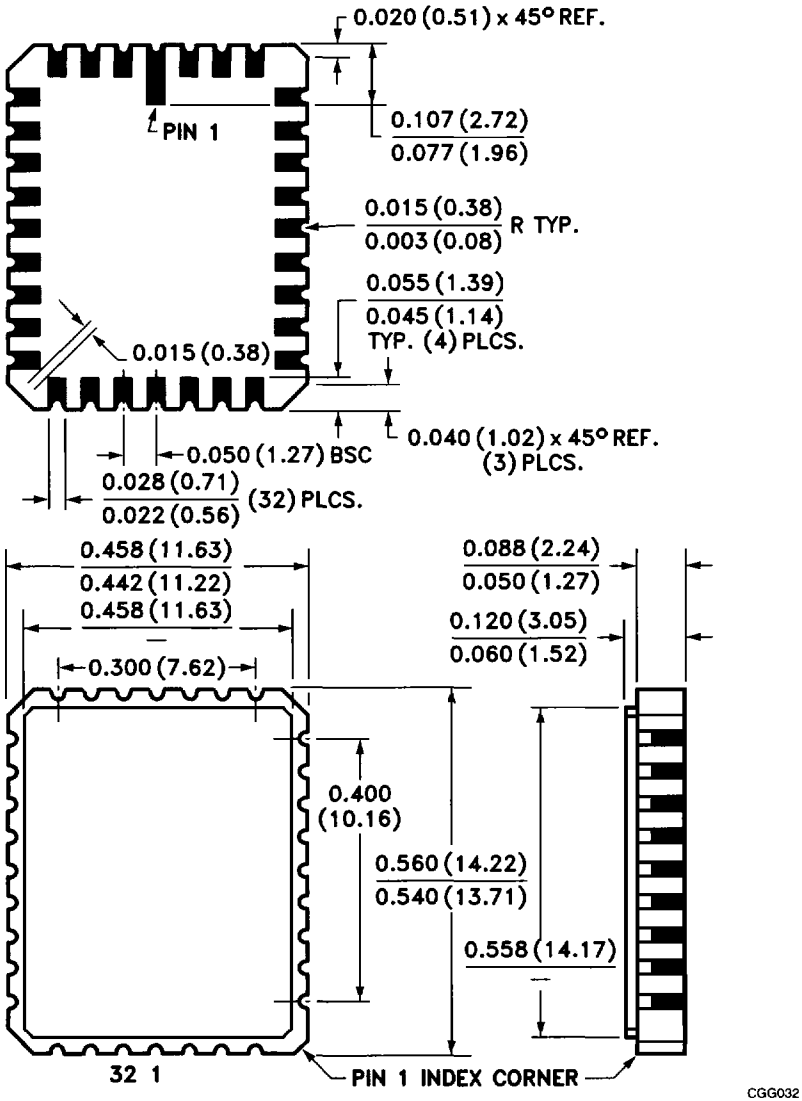


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS