XA2001

Low Speed USB Micro-controller

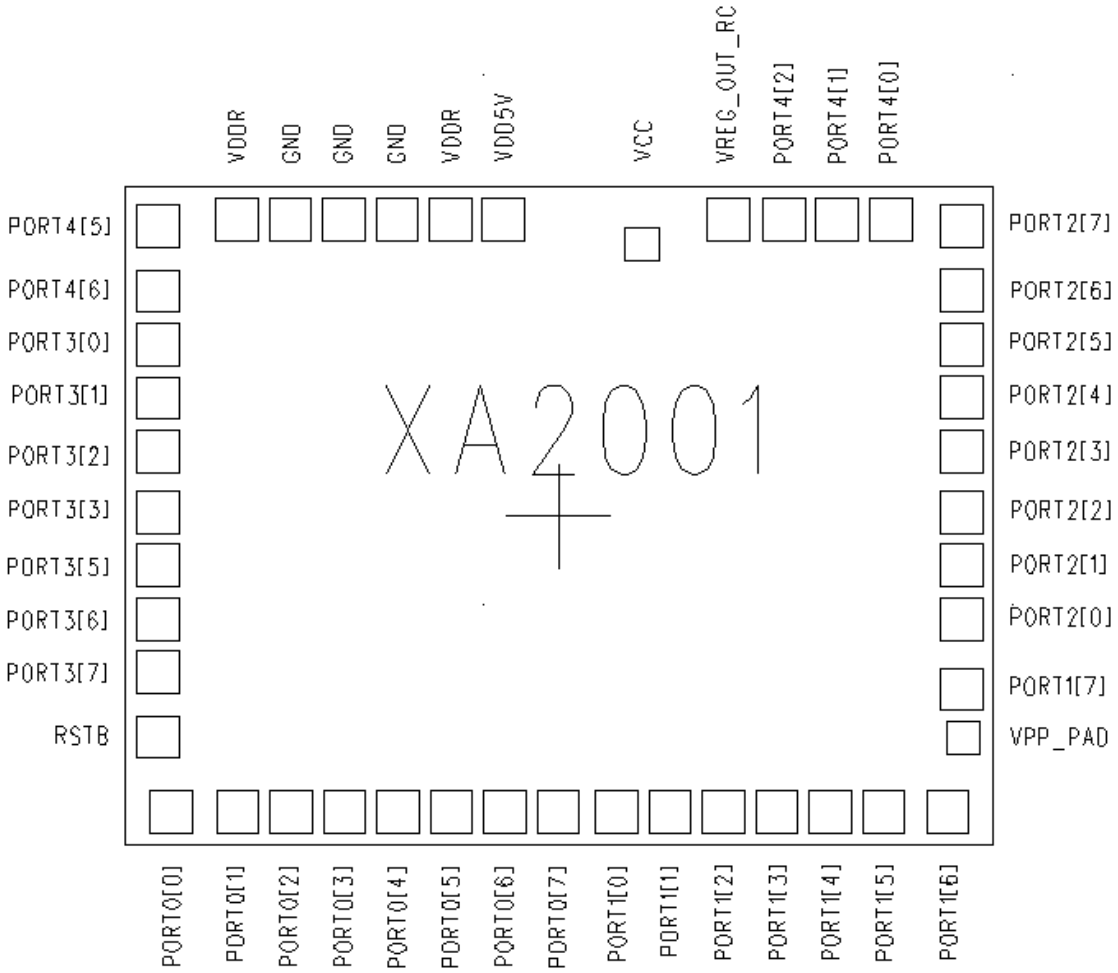
Features

- CMOS technology for low power consumption
- Operating voltage: 4.4V to 5.25V
- 3.3V regulator output
  - Maximum driving current 35mA
- 8-bit CMOS Micro-Processor (uP) core
  - Instruction set is compatible with standard 8051
- Program Memory
  - 16K Bytes Program Memory (MASK ROM)
- Data Memory
  - 256 Bytes Internal RAM
- Two 8-Bit auto-reloadable Base Timer
- Interrupt
  - 11 vectors interrupt structure
  - 2 programmable priority levels
- Built-in 1.5K ohm USB pull-up resistor
- USB Specification Compliance
  - Complies with USB specification 1.1
  - Support one Low-Speed USB Device Address with3 endpoints (endpoint 0, 1, and 2)
- One set of Time Capture circuit (rising and falling edge)
- Two Blue LED ports
- On-chip oscillator
  - Built-in 6MHz RC oscillator for MCU and USB
  - Built-in 32KHz RC oscillator for programmable Wake-up Timer
- General Purpose I/O
  - Up to 36 selectable GPIO
  - External interrupt input: P46
  - Source current selectable: Port0, Port1, Port2, Port3
- Reset
  - Hardware Reset (External Reset, Power-on reset and Low-Voltage Reset)
  - USB Reset
  - Watch-dog Reset
  - Resume Reset
- Two power-reducing mode
  - IDLE mode
  - Power-down mode

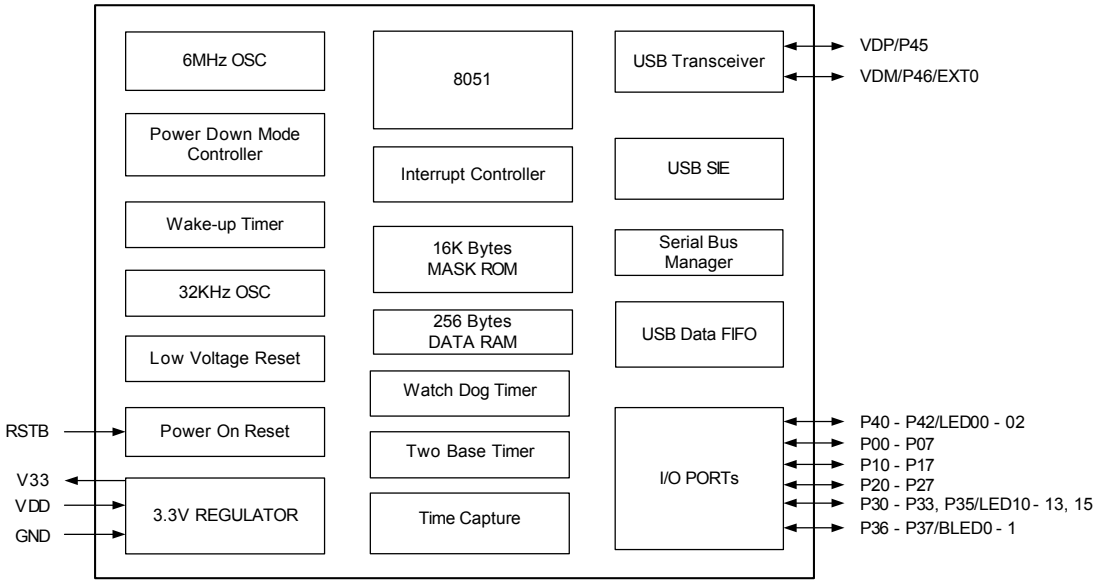
General Description

The XA2001 is designed for high performance Low-speed USB devices. It contains an 8051 micro-controller, Low-Speed USB SIE, Transceiver and data FIFO, build-in 3.3V regulator, on-chip 16K bytes Mask ROM and internal 256 bytes data RAM, Time Capture circuit, Base Timer, programmable Watch-dog Timer and Wake-up Timer, support multiple type LED driving capability for different application, built-in internal 32KHz oscillator, POR and LVR circuit saving your external components cost. Instead of external crystal, the XA2001 built in an on-chip high accuracy 6MHz RC Resonator for system and USB SIE. Up to 36 selectable GPIO are provided, while the source current of Port0, Port1, Port2, and Port3 can be configured smaller to support carbon membrane. Application can cover such items as Keyboards and others.

Pad Configuration



Block Diagram



Pad Description

PAD No.	Designation	I/O	Description
1	P46/VDM/EXT0	I/O	Bi-directional I/O pin shared with VDM
2	P30/LED10	I/O	Bi-directional I/O pin
3	P31/LED11	I/O	Bi-directional I/O pin
4	P32/LED12	I/O	Bi-directional I/O pin
5	P33/LED13	I/O	Bi-directional I/O pin
6	P35/LED15	I/O	Bi-directional I/O pin
7	P36/BLED0	I/O	Bi-directional I/O pin
8	P37/BLED1	I/O	Bi-directional I/O pin
9	RSTB	I	For external Reset Input with 55K (RRST) Ohm pull high resistance
10	P00	I/O	Bi-directional I/O pin
11	P01	I/O	Bi-directional I/O pin
12	P02	I/O	Bi-directional I/O pin
13	P03	I/O	Bi-directional I/O pin
14	P04	I/O	Bi-directional I/O pin
15	P05	I/O	Bi-directional I/O pin
16	P06	I/O	Bi-directional I/O pin
17	P07	I/O	Bi-directional I/O pin
18	P10	I/O	Bi-directional I/O pin
19	P11	I/O	Bi-directional I/O pin
20	P12	I/O	Bi-directional I/O pin
21	P13	I/O	Bi-directional I/O pin
22	P14	I/O	Bi-directional I/O pin
23	P15/TC0	I/O	Bi-directional I/O pin
24	P16	I/O	Bi-directional I/O pin
25	VPP	P	Voltage input (VPP)
26	P17	I/O	Bi-directional I/O pin
27	P20	I/O	Bi-directional I/O pin
28	P21	I/O	Bi-directional I/O pin
29	P22	I/O	Bi-directional I/O pin
30	P23	I/O	Bi-directional I/O pin
31	P24	I/O	Bi-directional I/O pin
32	P25	I/O	Bi-directional I/O pin
33	P26	I/O	Bi-directional I/O pin
34	P27	I/O	Bi-directional I/O pin
35	P40/LED00	I/O	Bi-directional I/O pin
36	P41/LED01	I/O	Bi-directional I/O pin
37	P42/LED02	I/O	Bi-directional I/O pin
38	VREG_OUT_RC	P	Regulator output(+1.8V)
39	VCC	P	Regulator output(+1.8V)
40	VDD	P	Power supply (5V)
41	VDDR	P	Regulator output (+3.3V)
42	GND	P	Ground
43	GND	P	Ground
44	GND	P	Ground
45	VDDR	P	Regulator output (+3.3V)
46	P45/VDP	I/O	Bi-directional I/O pin shared with VDP

Functional Description

1. Memory

1.1. Memory Allocation

There are 16K bytes Program Memory and 256 bytes Data Memory. These features are described as followed:

1.2. Program Memory

The XA2001 embeds 16K Bytes (0000H - 3FFFH) on-chip program memory for program code.

1.3. Data Memory

The XA2001 provides additional Bytes of RAM space for increased data parameter handling, high level language usage. The XA2001 has internal data memory that is mapped into three separate segments.

The three segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.

2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.

3. The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.

The Upper 128 bytes of RAM occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7Fh, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction. Note the unused address is unavailable in SFR.

The Internal RAM configuration is shown as below:

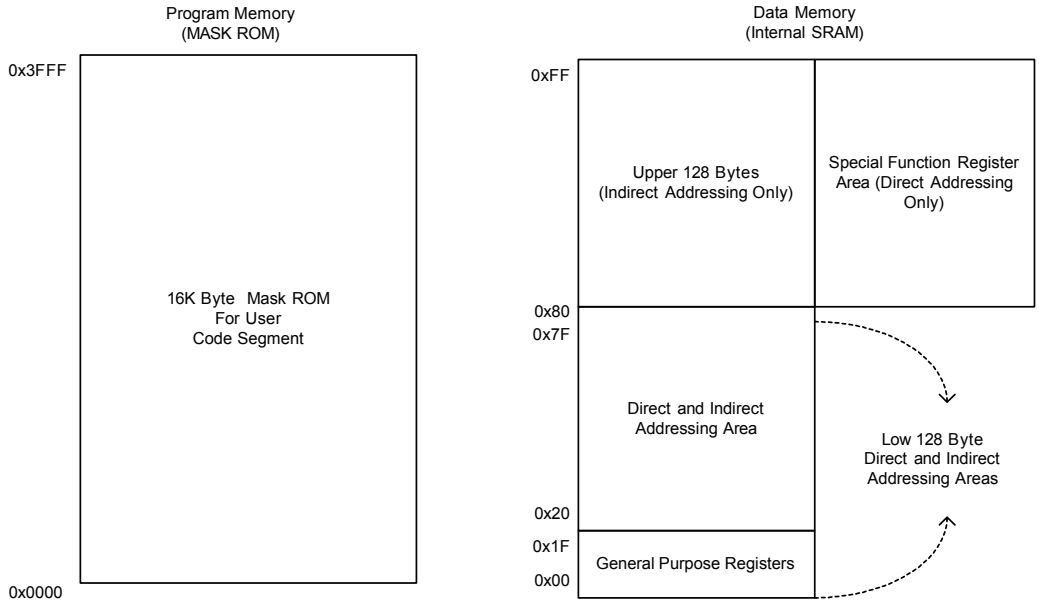


Figure 1-1. XA2001 Program/Data Memory Map

1.4. Registers

System Registers											
Address	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
00E0H	ACC	00H	R/W	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
00F0H	B	00H	R/W	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
00D0H	PSW	00H	R/W	CY	AC	F0	RS1	RS0	OV	0	P
0081H	SP	07H	R/W	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
0082H	DPL	00H	R/W	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
0083H	DPH	00H	R/W	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
0084H	DPL1	00H	R/W	DPL17	DPL16	DPL15	DPL14	DPL13	DPL12	DPL11	DPL10
0085H	DPH1	00H	R/W	DPH17	DPH16	DPH15	DPH14	DPH13	DPH12	DPH11	DPH10
0086H	INSCON	00H	R/W	0	0	0	0	INSCON3	INSCON2	0	INSCON0
00F1H	AUXC	00H	R/W	AUXC7	AUXC6	AUXC5	AUXC4	AUXC3	AUXC2	AUXC1	AUXC0
Idle and Power-down Control Registers											
Address	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0087H	PCON	00000000B	R/W	0	0	0	0	0	0	PD	IDL
008EH	SUSLO	00H	R/W	SUSL7	SUSL6	SUSL5	SUSL4	SUSL3	SUSL2	SUSL1	SUSL0
00AFH	PRCON	00000001B	R/W	0	0	0	0	0	ENWDT	0	ENLVR
General I/O Ports Registers											
Address	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0080H	P0	11111111B	R/W	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
0090H	P1	11111111B	R/W	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
00A0H	P2	11111111B	R/W	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
00B0H	P3	11111111B	R/W	P3.7	P3.6	P3.5	-	P3.3	P3.2	P3.1	P3.0
00C0H	P4	01100111B	R/W	0	P4.6	P4.5	0	0	P4.2	P4.1	P4.0
00A2H	P0WK	00000000B	R/W	P0WK7	P0WK6	P0WK5	P0WK4	P0WK3	P0WK2	P0WK1	P0WK0
00A3H	P1WK	00000000B	R/W	P1WK7	P1WK6	P1WK5	P1WK4	P1WK3	P1WK2	P1WK1	P1WK0
00A4H	P2WK	00000000B	R/W	P2WK7	P2WK6	P2WK5	P2WK4	P2WK3	P2WK2	P2WK1	P2WK0
00A5H	P3WK	00000000B	R/W	P3WK7	P3WK6	P3WK5	-	P3WK3	P3WK2	P3WK1	P3WK0
00A6H	P4WK	00000000B	R/W	0	P4WK6	P4WK5	0	0	P4WK2	P4WK1	P4WK0
009AH	P0CON	00000000B	R/W	P0CON7	P0CON6	P0CON5	P0CON4	P0CON3	P0CON2	P0CON1	P0CON0
009BH	P1CON	00000000B	R/W	P1CON7	P1CON6	P1CON5	P1CON4	P1CON3	P1CON2	P1CON1	P1CON0
009CH	P2CON	00000000B	R/W	P2CON7	P2CON6	P2CON5	P2CON4	P2CON3	P2CON2	P2CON1	P2CON0
009DH	P3CON	00000000B	R/W	P3CON7	P3CON6	P3CON5	-	P3CON3	P3CON2	P3CON1	P3CON0
009EH	P4CON	01100000B	R/W	0	P4CON6	P4CON5	0	0	P4CON2	P4CON1	P4CON0
00ADH	P3SEL	00000000B	R/W	P3SEL7	P3SEL6	P3SEL5	-	P3SEL3	P3SEL2	P3SEL1	P3SEL0
00AEH	P4SEL	00000000B	R/W	0	0	0	0	0	P4SEL2	P4SEL1	P4SEL0
00A7H	PHCON	00000000B	R/W	0	0	0	PHCON4	PHCON3	PHCON2	PHCON1	PHCON0
Base Timer/Time Capture Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
00D2H	BT0	00H	R/W	BT07	BT06	BT05	BT04	BT03	BT02	BT01	BT00
00D3H	BT1	00H	R/W	BT17	BT16	BT15	BT14	BT13	BT12	BT11	BT10
00D4H	BTCON	00H	R/W	ENBT1	BT1M2	BT1M1	BT1M0	ENBT0	BT0M2	BT0M1	BT0M0
00C8H	TCSTU	00H	R/W	0	0	0	TC0_OVL	0	0	TC0F_FULL	TC0R_FULL
00C9H	TCCON	00H	R/W	0	0	TC_CLREN	TC_OVLEN	0	0	TC0F_INT	TC0R_INT
00CAH	TCSCALE	00H	R/W	0	0	0	0	0	TC0TS2	TC0TS1	TC0TS0
00CBH	TCAP0R	00H	R	TCAP0R7	TCAP0R6	TCAP0R5	TCAP0R4	TCAP0R3	TCAP0R2	TCAP0R1	TCAP0R0
00CCH	TCAP0F	00H	R	TCAP0F7	TCAP0F6	TCAP0F5	TCAP0F4	TCAP0F3	TCAP0F2	TCAP0F1	TCAP0F0
Wake-up Timer & Resume Control Register											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0095H	WKT_CON	20H	R/W	0	0	PERIOD1	PERIOD0	WKT3	WKT2	WKT1	WKT0
Reset & Resume Flag											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0093H	CLRWDT	55H	W	CLRWDT7	CLRWDT6	CLRWDT5	CLRWDT4	CLRWDT3	CLRWDT2	CLRWDT1	CLRWDT0
0094H	PREWDT	00H	R/W	0	0	0	0	0	0	PREWDT1	PREWDT0

Registers (continued)

Interrupt Control Register											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
00A8H	IE	00H	R/W	EA	0	0	ETC0	ET1	0	ET0	EEXT0
00A9H	IE2	00H	R/W	0	EFUN	ESIE	EOUT0	EIN0	EOT0ERR	EOWSTUP	ESTUP
00B8H	IP	00H	R/W	0	0	0	PTC0	PT1	0	PT0	PEXT0
00B9H	IP2	00H	R/W	0	PFUN	PSIE	POUT0	PIN0	POT0ERR	POWSTUP	PSTUP
00DAH	IF	00H	R/W	0	0	0	TC0	T1	0	T0	EXT0
00DBH	IF2	00H	R/W	0	FUN	SIE	OUT0	IN0	OT0ERR	OWSTUP	STUP
00DCH	IRQEN	00H	R/W	EIN2	EIN1	ER0STL	ET0STL	ENAK2	ENAK1	ENAKR0	ENAKT0
00DDH	IRQEN2	00H	R/W	0	0	0	0	0	ESUSP	EOVL	0
00DEH	IRQFG	00H	R/W	IN2	IN1	R0STL	T0STL	NAK2	NAK1	NAKR0	NAKT0
00DFH	IRQFG2	00H	R/W	0	0	0	0	0	SUSP	OVL	0
USB Control Register											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
00F2H	DADDR	00H	R/W	0	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00F3H	DFC	01H	R/W	PULL_UP	USB_CON	FW_K	RSU_SEL	USBEN	0	ERWUP	VPCON
00EAH	TXDAT0	XXH	W	T07	T06	T05	T04	T03	T02	T01	T00
00EBH	TXCNT0	0XH	W	0	0	0	0	TC03	TC02	TC01	TC00
00ECH	TXFLG0	00H	R/W	0	0	0	0	0	0	STLT0	T0FULL
00EDH	RXDAT0	XXH	R	R07	R06	R05	R04	R03	R02	R01	R00
00EEH	RXCNT0	0XH	R	0	0	0	0	RC03	RC02	RC01	RC00
00EFH	RXFLG0	00H	R/W	0	0	RXERR	R0_OW	R0SEQ	OUT0ENB	STLR0	R0FULL
00E2H	TXDAT1	XXH	W	T17	T16	T15	T14	T13	T12	T11	T10
00E3H	TXCNT1	0XH	W	0	0	0	0	CNT13	CNT12	CNT11	CNT10
00E4H	TXFLG1	00H	R/W	0	0	0	0	T1EPE	T1SEQC	STL1	T1FULL
00E5H	TXDAT2	XXH	W	T27	T26	T25	T24	T23	T22	T21	T20
00E6H	TXCNT2	0XH	W	0	0	0	0	CNT23	CNT22	CNT21	CNT20
00E7H	TXFLG2	00H	R/W	0	0	0	0	T2EPE	T2SEQC	STL2	T2FULL
00E9H	CRWCON	00H	R/W	0	0	0	0	0	CRSEQ	STLCR	STLCW
0096H	MODE_FG	02H	R/W	0	Nonidle	WKUPT	RES_TRG	WDT	USBRST	POF	SUSF

2. Interrupt and Reset Vectors

- External Interrupt 0
- Base Timer 0
- Base Timer 1
- Time Capture Interrupt 0
- SETUP Interrupt
- OWSTUP Interrupt
- OT0ERR Interrupt
- IN0 Interrupt
- OUT0 Interrupt
- SIE Interrupt (NAKT0, NAKR0, T0STL, R0STL, NAK1, NAK2, IN1, IN2)
- Suspend/OVL Interrupt

Address	Interrupt Source	Enable	IRQ Flag	Description
0000H	Reset	-	-	System Reset
0003H	External Interrupt0	IE.0	EXT0	P4.6 Falling Edge
000BH	Base Timer0	IE.1	T0	Base Timer0 Interrupt
0013H	Reserved	-	-	-
001BH	Base Timer1	IE.3	T1	Base Timer1 Interrupt
0023H	Time Capture Interrupt0	IE.4	TC0	Time Capture0 Interrupt
002BH	Reserved	-	-	-
0033H	Reserved	-	-	-
0043H	Setup Interrupt	IE2.0	STUP	SETUP Token Interrupt
004BH	OWSTUP Interrupt	IE2.1	OWSTUP	-
0053H	OT0ERR Interrupt	IE2.2	OT0ERR	-
005BH	IN0 Interrupt	IE2.3	IN0	IN0 Token Interrupt
0063H	OUT0 Interrupt	IE2.4	OUT0	OUT0 Token Interrupt
006BH	SIE Interrupt	IE2.5	SIE	NAKT0, NAKR0, T0STL, R0STL, NAK1, NAK2, IN1, IN2
0073H	Suspend/OVL Interrupt	IE2.6	FUN	SUSP/OVL Interrupt
007BH	Reserved	-	-	-

3. Micro-Processor

3.1. General Description

The XA2001 is a high performance 8051 CPU core embedded micro-controller. The instruction set is compatible with standard 8051.

3.2. Special Function Registers (SFRs)

The XA2001 has a total of 69 SFRs, as shown in the figure below - SFR Map for XA2001. Note that not all the addresses are occupied by SFR's. The unoccupied addresses are not implemented and should not be used by the customer. Read access from these unoccupied locations will return unpredictable data, while write accesses will have no effect on the chip.

SFR Map for XA2001

F8H	-	-	-	-	-	-	-	-	FFH
F0H	B	AUXC	DADDR	DFC	-	-	-	XPAGE	F7H
E8H	-	CRWCON	TXDAT0	TXCNT0	TXFLG0	RXDAT0	RXCNT0	RXFLG0	EFH
E0H	ACC	-	TXDAT1	TXCNT1	TXFLG1	TXDAT2	TXCNT2	TXFLG2	E7H
D8H	-	-	IF1	IF2	IRQEN	IRQEN2	IRQFG	IRQFG2	DFH
D0H	PSW	-	BT0	BT1	BTCON	-	-	-	D7H
C8H	TCSTU	TCCON	TCSCALE	TCAP0R	TCAP0F	-	-		CFH
C0H	P4	-	-	-	-	-	-	-	C7H
B8H	IP	IP2	-	-	-	-	-	-	BFH
B0H	P3	-	-	-	-	-	-	-	B7H
A8H	IE	IE2	-	-	-	P3SEL	P4SEL	PRCON	AFH
A0H	P2	-	P0WK	P1WK	P2WK	P3WK	P4WK	PHCON	A7H
98H	-	-	P0CON	P1CON	P2CON	P3CON	P4CON	-	9FH
90H	P1	-	-	CLRWDT	PREWDT	WKT_CON	MODE_FG	-	97H
88H	-	-	-	-	-	-	SUSLO	-	8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H

Note 1: *SFR's in marked column are bit addressable.*
Note 2: *SFR's in gray color are standard 8051 SFR's, and others are SFR's for XA2001.*

3.2.1. Accumulator (ACC)

ACC is the accumulator register used for most of the arithmetic and logical instructions. Its initial value is 00h.

3.2.2. B Register (B)

The **B** register is an SFR which is used primarily in the multiply and divide instructions. It can also be used as a temporary scratch pad register for the other instructions and its initial value is 00h.

3.2.3. Program Status Word (PSW)

The **PSW** is the register that holds information about the status of the Accumulator, the selected register banks and other information. Its initial value is 00h.This register is described in details in the following figure.

PSW - Program Status Word Register		
Bit 7	CY	Carry flag
Bit 6	AC	Auxiliary Carry flag (for BCD operations)
Bit 5	F0	Flag 0 (Available to the user for general purposes)
Bit 4	RS1	Register Bank select control bit 1 & 0 Set/cleared by software to determine working bank. (RS1, RS0): (00) - Bank 0 ⇔ Address → (00H - 07H) (01) - Bank 1 ⇔ Address → (08H - 0FH) (10) - Bank 2 ⇔ Address → (10H - 17H) (11) - Bank 3 ⇔ Address → (18H - 1FH)
Bit 3	RS0	
Bit 2	OV	Overflow Flag
Bit 1	X	User definable flag
Bit 0	P	Parity Flag Set/Cleared by hardware each instruction cycle to indicate an odd/even number of “one” bit I the Accumulator, i.e., even parity.

3.2.4. Stack Pointer (SP)

The Stack Pointer is an 8-bit wide register that is used to point to the top of the stack where addresses are stored. After a reset, the stack pointer is initialized to 07H, and so the stack begins at 08H. However the stack can reside at any location in the Internal RAM and stack pointer can be programmed to suit the user’s needs.

3.2.5. Data Pointers (DPH, DPL)

One Data Pointers (DPTR) consist of **DPH**, **DPL** Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

3.2.6. Port 0, Port1, Port2, Port3 and Port4 (P0, P1, P2, P3 and P4)

The five ports have five SFR’s associated with them. Data to be brought out onto the port pins is written to the latches.

3.2.7. Enhanced function of CPU core

- Instruction extension of 'MUL' and 'DIV'
- Dual Data Pointer
- CPU core enhanced registers: **AUXC** (00F1H), **DPL1** (0084H), **DPH1** (0085H), **INSCON** (0086H)

(1) Instruction extension

The 8051 core of XA2001 extends 'MUL' and 'DIV' instructions to support a 16-bit operand. A new register **AUXC** is applied to hold the upper part of the operand/result. **AUXC** can act as a normal register in other operands except 'MUL' or 'DIV'.

After reset the core is in standard mode that means the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16-bit mode, the corresponding enable bit in the **INSCON** register has to be set.

	Operand		**Result**		
			A	B	AUXC
MUL	INSCON.2 = 0; 8-bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16-bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8-bit mode	(A) / (B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16-bit mode	(AUXC A) / (B)	Quotient Low Byte	Remainder	Quotient High Byte

(2) Dual Data Pointer

Data memory moves can be accelerated using two data pointer. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 consist of into two SFR registers, **DPL1** and **DPH1**, which can be individually accessed.

User can switch the data pointers by toggling the LSB of **INSCON** register. 'INC' instruction is fastest way to perform this. All DPTR-related instructions will use the currently selected data pointer.

0086H	**INSCON**	**Initial Value**	**CPU Enhanced Mode Control Register**	
Bit [7:4]	-	0000b	-	Reserved
Bit3	INSCON3	0b	R/W	**Instruction 'DIV' operand mode configuration bit** 1: 16-bit DIV 0: 8-bit DIV **Reset source: Hardware reset or USB reset**
Bit2	INSCON2	00b	R/W	**Instruction 'MUL' operand mode configuration bit** 1: 16-bit MUL 0: 8-bit MUL **Reset source: Hardware reset or USB reset**
Bit1	-	0b	-	Reserved
Bit0	INSCON0	0000b	R/W	**Data pointer selection bit** 1: DPTR1 0: DPTR **Reset source: Hardware reset or USB reset**

3.3. Instruction Set List

Arithmetic Instructions					
Opcode			**Bytes**	**Cycles**	**Meaning**
ADD	A, Rn		1	1	Add reg to acc
	A, @Ri		1	2	Add indir byte to acc
	A, direct		2	2	Add dir byte to acc
	A, #data		2	2	Add imm. Data to acc
ADDC	A, Rn		1	1	Add reg to acc with carry flag
	A, @Ri		1	2	Add indir byte to acc with carry flag
	A, direct		2	2	Add dir byte to acc with carry flag
	A, #data		2	2	Add imm. Data to acc with carry flag
SUBB	A, Rn		1	1	Subtract reg from acc with borrow
	A, @Ri		1	2	Subtract indir byte from acc with borrow
	A, direct		2	2	Subtract dir byte from acc with borrow
	A, #data		2	2	Subtract imm. Data from acc with borrow
INC	A		1	1	Increment acc
	Rn		1	2	Increment reg
	@Ri		1	3	Increment indir byte
	DPTR		1	4	Increment data pointer
	direct		2	3	Increment dir byte
DEC	A		1	1	Decrement acc
	Rn		1	2	Decrement reg
	@Ri		1	3	Decrement indir byte
	direct		2	3	Decrement dir byte
MUL	AB		1	11	Multiply A and B, 8-bit
			1	20	Multiply (AUXC A) and B, 16-bit
DIV	AB		1	11	Divide A by B, 8-bit
			1	20	Divide (AUXC A) by B, 16-bit
DA	A		1	1	Decimal adjust acc
Logical Instructions					
Opcode			**Bytes**	**Cycles**	**Meaning**
CLR	A		1	1	Clear acc
CPL	A		1	1	Complement acc
ANL	A, Rn		1	1	AND register to acc
	A, @Ri		1	2	AND indir byte to acc
	A, direct		2	2	AND dir byte to acc
	A, #data		2	2	AND imm. Data to acc
	direct, A		2	3	AND acc to dir byte
	direct, #data		3	3	AND imm. Data to dir byte
ORL	A, Rn		1	1	OR reg to acc
	A, @Ri		1	2	OR indir byte to acc
	A, direct		2	2	OR dir byte to acc
	A, #data		2	2	OR imm. Data to acc
	direct, A		2	3	OR acc to dir byte
	direct, #data		3	3	OR imm. Data to dir byte
XRL	A, Rn		1	1	Exclusive-OR reg to acc
	A, @Ri		1	2	Exclusive-OR indir byte to acc
	A, direct		2	2	Exclusive-OR dir byte to acc
	A, #data		2	2	Exclusive-OR imm. Data to acc
	direct, A		2	3	Exclusive-OR acc to dir byte
	direct, #data		3	3	Exclusive-OR imm. Data to dir byte

Instruction Set List (continued)

RL	A		1	1	Rotate acc left
RLC	A		1	1	Rotate acc left through the carry
RR	A		1	1	Rotate acc right
RRC	A		1	1	Rotate acc right throught the carry
SWAP	A		1	4	Swap nibbles within the acc
Data Transfer					
Opcode			**Bytes**	**Cycles**	**Meaning**
MOV	A, Rn		1	1	Move reg to acc
	A, @Ri		1	2	Move indir byte to acc
	Rn, A		1	2	Move acc to reg
	@Ri, A		1	2	Move acc to indir byte
	A, direct		2	2	Move dir byte to acc
	A, #data		2	2	Move imm. Data to acc
	Rn, #data		2	2	Move imm. Data to reg
	direct, A		2	2	Move acc to dir byte
	direct, Rn		2	2	Move reg to dir byte
	@Ri, #data		2	2	Move imm. Data to indir byte
	Rn, direct		2	3	Move dir byte to reg
	direct, @Ri		2	3	Move indir byte to dir byte
	@Ri, direct		2	3	Move dir byte to indir byte
	direct, direct		3	3	Move dir byte to dir byte
	direct, #data		3	3	Move imm. Data to dir byte
	DPTR,#data16		3	3	Load data pointer with 16-bit constant
MOVC	A, @A+DPTR		1	7	Move code byte relative to DPTR to acc
	A, @A+PC		1	8	Move code byte relative to PC to acc
MOVX	@Ri, A		1	4	Move acc to xdata byte (8 bit address)
	A, @Ri		1	5	Move xdata byte to acc (8 bit address)
	@DPTR, A		1	5	Move acc to xdata byte (16 bit address)
	A, @DPTR		1	6	Move xdata byte to acc (16 bit address)
PUSH	direct		2	5	Push dir byte to stack
POP	direct		2	4	Pop dir byte from stack
XCH	A, Rn		1	3	Exchange reg with acc
	A, @Ri		1	4	Exchange indir byte with acc
	A, direct		2	4	Exchange dir byte with acc
XCHD	A, @Ri		1	4	Exchange low-order digit in indir byte with acc
Bit Manipulation					
Opcode			**Bytes**	**Cycles**	**Meaning**
CLR	C		1	1	Clear carry
	bit		2	3	Clear dir bit
SETB	C		1	1	Set carry
	bit		2	3	Set dir bit
CPL	C		1	1	Complement carry
	bit		2	3	Complement dir bit
ANL	C, bit		2	2	AND dir bit to carry
	C, /bit		2	2	AND complement of dir bit to carry
ORL	C, bit		2	2	OR dir bit to carry
	C, /bit		2	2	OR complement of dir bit to carry
MOV	C, bit		2	2	Move dir bit to carry
	bit, C		2	3	Move carry to dir bit

Instruction Set List (continued)

Program Branching					
Opcode			**Bytes**	**Cycles**	**Meaning**
JC	rel	(not taken)	2	2	Jump if carry is set Jump if less than
		(taken)		4	
JNC	rel	(not taken)	2	2	Jump if carry is not set Jump if greater than or equal
		(taken)		4	
JB	bit, rel	(not taken)	3	4	Jump if dir bit is set
		(taken)		6	
JNB	bit, rel	(not taken)	3	4	Jump if dir bit is not set
		(taken)		6	
JBC	bit, rel	(not taken)	3	4	Jump if dir bit is set and clear bit
		(taken)		6	
JZ	rel	(not taken)	2	3	Jump if acc is zero
		(taken)		5	
JNZ	rel	(not taken)	2	3	Jump if acc is not zero
		(taken)		5	
SJMP	rel		2	4	Short jump (relative address)
ACALL	addr11		2	7	Absolute subroutine call
LCALL	addr16		3	7	Long subroutine call
RET			1	8	Return from subroutine
RETI			1	8	Return from interrupt
AJMP	addr11		2	4	Absolute jump
LJMP	addr16		3	5	Long jump
JMP	@A+DPTR		1	6	Jump indir relative to DPTR
CJNE	A, direct, rel	(not taken)	3	4	Compare dir byte to acc. And jump if not equal
		(taken)		6	
CJNE	A, #data, rel	(not taken)	3	4	Compare imm. Data to acc. And jump if not equal
		(taken)		6	
CJNE	Rn, #data, rel	(not taken)	3	4	Compare imm. Data to reg and jump if not equal
		(taken)		6	
CJNE	@Ri, #data, rel	(not taken)	3	4	Compare imm. Data to indir and jump if not equal
		(taken)		6	
DJNZ	Rn, rel	(not taken)	2	3	Decrement reg and jump if not zero
		(taken)		5	
DJNZ	direct, rel	(not taken)	3	4	Decrement dir byte and jump if not zero
		(taken)		6	
NOP			1	1	No operation

4. Oscillators

The XA2001 has a built-in 6MHz RC resonator for system clock. The oscillator generates the system timing and control signal to be supplied to the CPU core and the on-chip peripherals, such as USB, Timer and so on.

Besides, the XA2001 also has a built-in 32 KHz RC resonator to generate the clock for wake up timer.

5. Reset and Power-reducing Mode

There are totally four Reset Sources in the XA2001 application.

- Hardware reset: Low-Voltage Reset, Power-On Reset or External Reset
- WDT (Watch-dog Timer) Reset
- Resume Reset
- USB Reset

5.1. Hardware Reset

5.1.1. Power-On Reset (POR)

When power is first applied to the XA2001, the internal Power-On Reset will be generated and reset the whole chip.

This process is fulfilled by a power-on reset circuit and an auxiliary Lower-voltage reset circuit (LVRA) monitoring V_{DD}. Once V_{DD} climb up from 0V and cross the V_{POR}, the internal POR signal will active and end after $T_{RST(POR)}$.

The LVRA will perform as a function Low-voltage Reset when system is normal running (under normal/idle/power-down mode). LVRA reset signal (this signal is shared with POR singal) will active when V_{DD} was less than V_{LVRA} and lasts for $T_{PW(LVRA)}$, LVRA signal will end after $T_{RST(LVR)}$ when V_{DD} was larger than V_{LVRA}.

See Figure.5-1 for the POR and LVRA behavior.

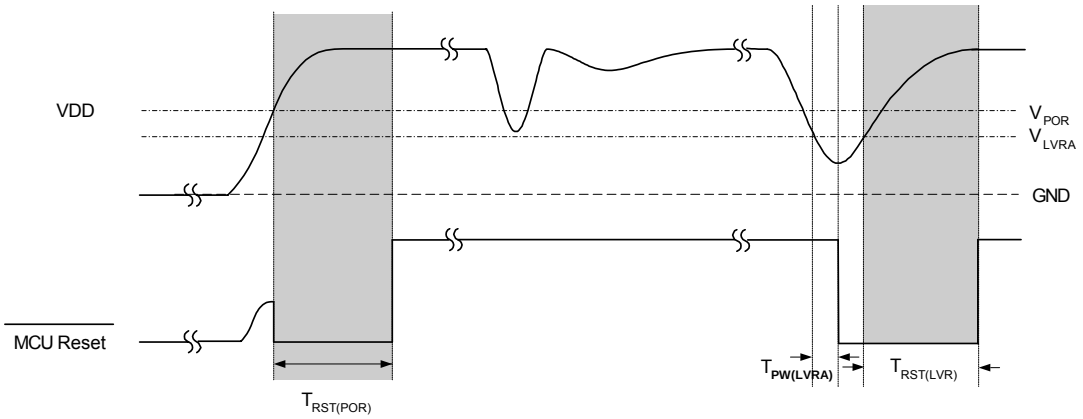


Figure 5-1. Power-on Reset and LVRA

Note:

$V_{POR(max.)}$ = 3.8V

$V_{LVRA(min.)}$ = 3.2V, $V_{LVRA(typ.)}$ = 3.5V, and $V_{LVRA(max.)}$ = 3.8V

$T_{PW(LVRA)}$ (Drop-Down Pulse Width for LVR1) = 2^9 X T_{SYS}

$T_{RST(POR)}$ (Internal Power-on Reset Hold Time) = 2^{16} X T_{SYS} + 165 X T_{RING}

$T_{RST(LVR)}$ ((Internal Low-voltage Reset Hold Time) = 2^{16} X T_{SYS} + 165 X T_{RING}

5.1.2. Low Voltage Reset (LVR)

(1) Low Voltage Reset 1 (LVR1)

00AFH	PRCON	Initial Value	Power-reducing Control Register	
Bit [7:3]	-	00000b	-	Reserved
Bit 2	ENWDT	0b	R/W	1: Enable Watch-Dog timer under idle mode 0: Disable Watch-Dog timer under idle mode **Reset source: Hardware reset, USB reset, or Resume Reset**
Bit 1	-	0b	-	Reserved
Bit 0	ENLVR1	1b	R/W	1: Enable Low-Voltage Reset 1 under power-down mode 0: Disable Low-Voltage Reset 1 under power-down mode **Reset source: Hardware reset, USB reset, or Resume Reset**

The LVR1 circuit will monitor the 1.8V regulator output voltage to the MCU core.

LVR1 reset signal will active when the input power of MCU core was less than V_{LVR1} and lasts for $T_{PW(LVR1)}$, LVR1 signal will end after $T_{RST(LVR)}$ when the power was larger than V_{LVR1}. See Figure 5-2 for the LVR1 behavior.

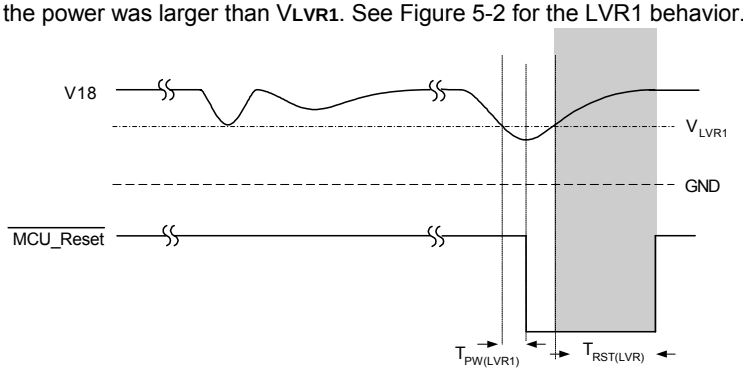


Figure 5-2. Low Voltage Reset 1

Note:
$V_{LVR1(min.)}$ = 1.4V, $V_{LVR1\ (typ.)}$ = 1.5V, and $V_{LVR1\ (max.)}$ = 1.6V
$T_{PW(LVR1)}$ (Drop-Down Pulse Width for LVR1) = 2^9 X T_{SYS}
$T_{RST(LVR)}$ (Internal Low-voltage Reset Hold Time) = 2^{16} X T_{SYS}

Under Power-down mode:
- **ENLVR1** = 0: Disable LVR1 under Power-down mode
- **ENLVR1** = 1: Enable LVR1 under Power-down mode

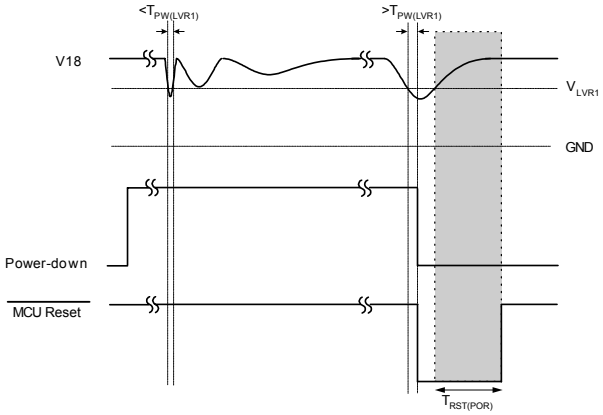


Figure 5-3. Low Voltage Reset 1 under Power-down Mode

(2) Low Voltage Reset (LVR2)

The embedded Low-Voltage Reset (LVR2) circuit monitors the 3.3V regulator output Voltage. It will generate a internal reset to the whole chip while heavy loads at 3.3V regulator output switched on cause the regulator output voltage temporarily fall below the minimum specified operating voltage. This feature is can protect system from working under bad power supply environment.

LVR2 reset signal will active when the 3.3V regulator output was less than V_{LVR2} and lasts for $T_{PW(LVR2)}$, LVR2 signal will end after $T_{RST(LVR)}$ when the power was larger than V_{LVR2}. See Figure 5-4 for the LVR2 behavior.

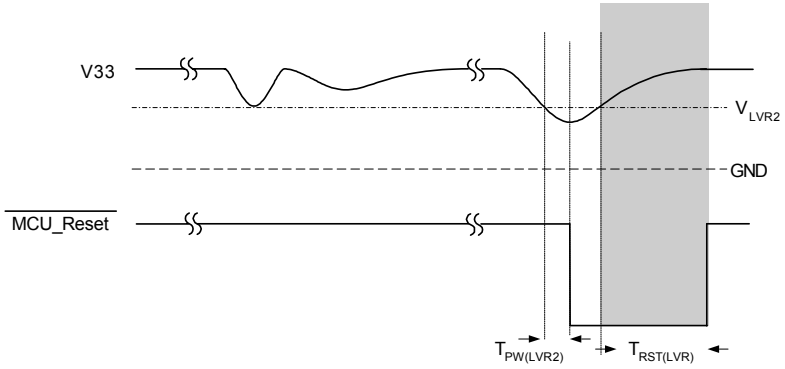


Figure 5-4. Low Voltage Reset 2

Note:
$T_{PW(LVR2)}$ (Drop-Down Pulse Width for LVR2) = 2^9 X T_{SYS}
$T_{RST(LVR)}$ (Internal Low-voltage Reset Hold Time) = 2^{16} X T_{SYS}

5.1.3. External Reset

(1) Normal mode and IDLE mode

The MCU will generate internal system reset when the voltage level of the External Reset is less than the lower-threshold voltage $V_{LT(RSTB)}$ and its pulse width larger than $T_{PW(RSTB)}$. The reset cycle will end after $T_{RST(RSTB)}$ when the RSTB pin level is larger than the upper-threshold voltage $V_{UT(RSTB)}$.

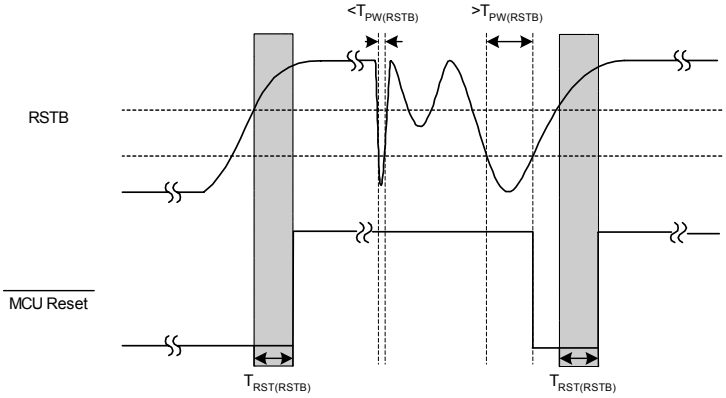


Figure 5-5. External Reset

Note:
$T_{PW(RSTB)}$ (RESETB Input Low Pulse Width) = 2^{13} X T_{SYS}
$T_{RST(RSTB)}$ (External Reset Hold Time) = 2^7 X T_{SYS}
$V_{UT(RSTB)}$ (Upper-threshold voltage of External reset) = 2 V (Min.)
$V_{LT(RSTB)}$ (Lower-threshold voltage of External reset) = 0.8 V (Max.)

(2) Power-down mode

When the device was in Power-down mode, an External Reset can't force the device to exit its Power-down mode.

5.2. Watch-dog Timer Reset

The XA2001 implements a Watchdog timer to avoid system stop or malfunction. The clock source of the WDT is Fsys. The time-out interval of Watchdog timer is selected by **PREWDT[1:0]**. The Watchdog timer must be cleared within time-out period; otherwise the Watchdog timer will overflow and cause a system reset. The Watchdog timer is cleared and enabled after the system is reset, and can be disabled by the software only on idle mode. Users can clear the Watchdog timer by writing a #55H to the **CLRWDT** (0093H) register.

0093H	CLRWDT	Initial Value	Clear Watch-dog Timer Control Register	
Bit [7:0]	CLRWDT [7:0]	55H	W	Write “55H” to clear watch-dog timer **Reset source: Hardware reset, USB reset, WDT reset, Resume reset**

0094H	PREWDT	Initial Value	Watch-dog Timer Pre-scalar Control Register	
Bit [7:2]	-	000000b	-	Reserved
Bit [1:0]	PREWDT [1:0]	00b	R/W	**Watch-dog timer Pre-scalar control register** 00: 2^{16} Tsys (10.922ms) 01: 2^{17} Tsys (21.845ms) 10: 2^{18} Tsys (43.688ms) 11: 2^{19} Tsys (87.376ms) **Reset source: Hardware reset, USB reset, WDT reset, Resume reset**

Note1: *The new Pre-scalar value will be loaded after the Watchdog Timer was cleared (write #55H to **CLRWDT** register)*

Note2: *When system enters Power-Down Mode, WDT will stop due to the lack of Tsys. When system resumes from Power-Down Mode, the WDT control register will be cleared to the initial state.*

5.3. IDLE and Power-Down Mode

The XA2001 has two power-reducing modes:

- IDLE mode (**IDL** = 1 & **SUSLO** = 55H): The CPU is frozen, but otherwise the circuit continues to run.
- Power-down mode (**PD** = 1 & **SUSLO** = 55H): The oscillator is frozen.

008EH	SUSLO	Initial Value	Power saving Control Register 1	
Bit [7:0]	SUSLO [7:0]	00H	R/W	IDL = 1 & SUSLO = 55H: Enter idle mode PD = 1 & SUSLO = 55H: Enter Power-down mode **Reset source: Hardware reset, USB reset, WDT reset, Resume reset**

0087H	PCON	Initial Value	Power saving Control Register 2	
Bit [7:2]	-	000000b	-	Reserved
Bit 1	PD	0b	R/W	PD = 1 & SUSLO = 55H: Enter Power-down mode **Reset source: Hardware reset, USB reset, WDT reset, Resume reset**
Bit 0	IDL	0b	R/W	IDL = 1 & SUSLO = 55H: Enter idle mode **Reset source: Hardware reset, USB reset, WDT reset, Resume reset**

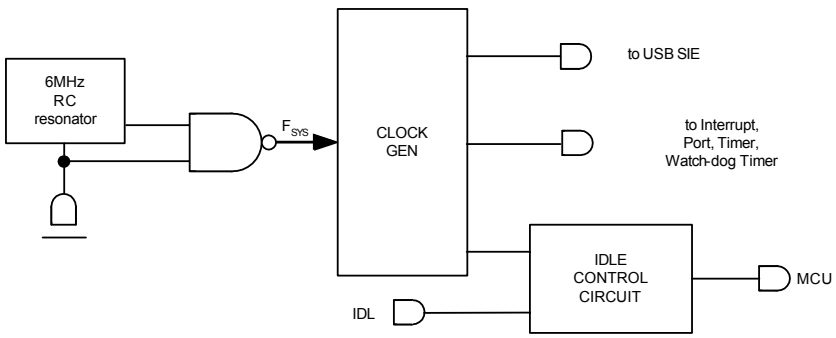


Figure 5-6. Sketch map for IDLE and Power-Down Mode implement

5.3.1. IDLE mode

Two continuous instructions that set PCON.0 to '1' and set SUSLO to '55H' let the XA2001 enter IDLE mode. In IDLE mode, the internal clock signal is gated off to the CPU only. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their value during IDLE mode. The port pins hold the latest logical states before system enter IDLE mode.

There are four ways to terminate IDLE mode and back to Normal mode. In order to make the program execute properly, user should add three NOPs after the instruction that put the device into IDLE mode. (If Watch-Dog Timer was disabled at IDLE mode, then it will restart to count from the value where it was stopped when entering IDLE Mode. When the system leaves IDLE Mode, PCON.0 and SUSLO will be cleared by hardware)

(1) Activation of any enabled interrupt will terminate the IDLE mode. (As same as standard 8051 micro controller) The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into IDLE mode.

(2) Port0, Port1, Port2, Port3 and Port4 can be set as a resume ports by setting **P0WK**, **P1WK**, **P2WK**, **P3WK**, and **P4WK**. Any low level of enabled resume source will terminate the IDLE mode

(3) When the wake-up timer is time-out in IDLE mode, the next instruction to be executed will be the one following the instruction that put the device into IDLE mode.

(4) Hardware reset USB reset or Watch Dog Reset. At this time, the CPU resumes program execution from the beginning of the whole program, which is 0000H.

Example:

```
IDLE2:
        MOV     PORT2, #FFH     ; Initialize PORT2 resume source to be high.
        MOV     P2WK,  #FFH     ; Enable PORT2 resume ability.
        MOV     PORT0, #00H     ; Pull low PORT0.
        MOV     P0WK,  #00H     ; Disable PORT0 resume ability.
        ANL     PRCON, #FBH     ; Disable Watch-Dog timer under idle mode.
        MOV     CLRWDT, #55H    ; Clear Watch-Dog Timer
        ORL     PCON,  #01H     ; Set IDLE mode.
        MOV     SUSLO, #55H     ; Enter IDLE mode.
        NOP                     ; 3 NOP instruction (make sure program will executes properly)
        NOP
        NOP
        MOV     CLRWDT, #55H    ; Clear Watch-dog Timer
```

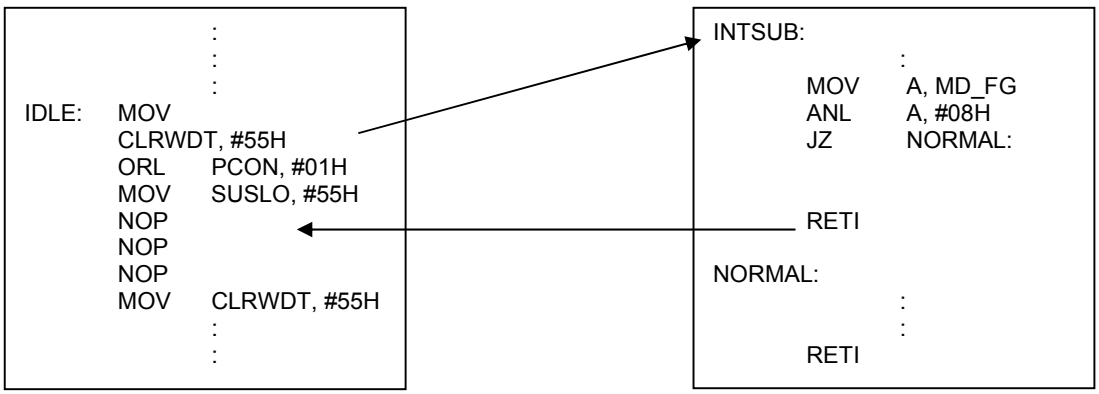
00A2H	P0WK	Initial Value	Port0 Resume Enable Register	
Bit [7:0]	P0WK [7:0]	00h	**R/W**	1: Enable wake-up function of PORT0's pins (Low level trigger) 0: Disable wake-up function of PORT0's pins (Low level trigger) **Reset source: Hardware reset**

00A3H	P1WK	Initial Value	Port1 Resume Enable Register	
Bit [7:0]	P1WK [7:0]	00h	**R/W**	1: Enable wake-up function of PORT1's pins (Low level trigger) 0: Disable wake-up function of PORT1's pins (Low level trigger) **Reset source: Hardware reset**

00A4H	P2WK	Initial Value	Port2 Resume Enable Register	
Bit [7:0]	P2WK [7:0]	00h	**R/W**	1: Enable wake-up function of PORT2's pins (Low level trigger) 0: Disable wake-up function of PORT2's pins (Low level trigger) **Reset source: Hardware reset**

00A5H	P3WK	Initial Value	Port3 Resume Enable Register	
Bit [7:5,3:0]	P3WK [7:5,3:0]	00h	**R/W**	1: Enable wake-up function of PORT3's pins (Low level trigger) 0: Disable wake-up function of PORT3's pins (Low level trigger) **Reset source: Hardware reset**

00A6H	P4WK	Initial Value	Port4 Resume Enable Register	
Bit 7	-	0b	-	Reserved
Bit [6:5]	P4WK [6:5]	00b	R/W	1: Enable wake-up function of PORT4's pins (Low level trigger) 0: Disable wake-up function of PORT4's pins (Low level trigger) **Reset source: Hardware reset**
Bit [4:3]	-	00b	-	Reserved
Bit [2:0]	P4WK [2:0]	000b	-	1: Enable wake-up function of PORT4's pins (Low level trigger) 0: Disable wake-up function of PORT4's pins (Low level trigger) **Reset source: Hardware reset**



In this example, Watch-dog Timer can be cleared either before entering IDLE mode or after terminating IDLE mode. The number of NOPs applied after the instruction that put the device into IDLE mode depends on the type of the instruction in order to make the program work properly. In INTSUB, it detects if interrupts occur in Idle mode or not.

5.3.2. Power-down mode

Method of entering Power-down mode: set PCON.1 = 1 and set SUSLO = 55h

- In the Power- down mode, the on-chip oscillator stops.
- With the clock frozen, all functions are stopped, but the on-chip RAM and Special function Registers are held.
- In order to make sure the program will resume properly, user should add three NOPs immediately after setting SUSLO to 55H.

There are two ways to exit from Power-down mode.

- Low Voltage Reset or Power-On Reset.
- Resume reset: A resume reset holds SFR values, CPU status and Pin state, but program is re-run at 0000h. **There are three ways to generate resume reset.**
  (1) Port0, Port1, Port2, Port3 and Port4 can be set as a resume ports by setting **P0WK**, **P1WK**, **P2WK**, **P3WK**, and **P4WK**. Any low level of enabled resume source is triggered in Power-down mode will cause a resume reset.
  (2) Wake-up Timer time out
  (3) USB Bus Non-idle State (VDM is low, or VDM & VDP both high)

Port resume reset example 1: Assume that PORT2 is resume source and H/W issues K-State when Resume Reset occurs.

```
PWRDN_HW：
        MOV     PORT2  #FFH    ; initialize PORT2 resume source to be high.
        MOV     P2WK   #FFH    ; Enable PORT2 resume ability.
        MOV     PORT0  #00H    ; Pull low PORT0.
        MOV     P0WK   #00H    ; Disable PORT0 resume ability.
        ANL     DFC    #EFH    ; RSU_SEL = 0, H/W issue K-State to respond RESUME signal.
        ORL     DFC,   #02H    ; ERWUP = 1, Enable Remote Wake Up function.
        MOV     CLRWDT #55H    ; Clear Watch-Dog Timer.
        ORL     PCON   #02H    ; Set POWER DOWN mode.
        MOV     SUSLO  #55H    ; Enter POWER DOWN mode.
        NOP                    ; 3 NOP instruction (make sure program will executes properly)
        NOP
        NOP
```

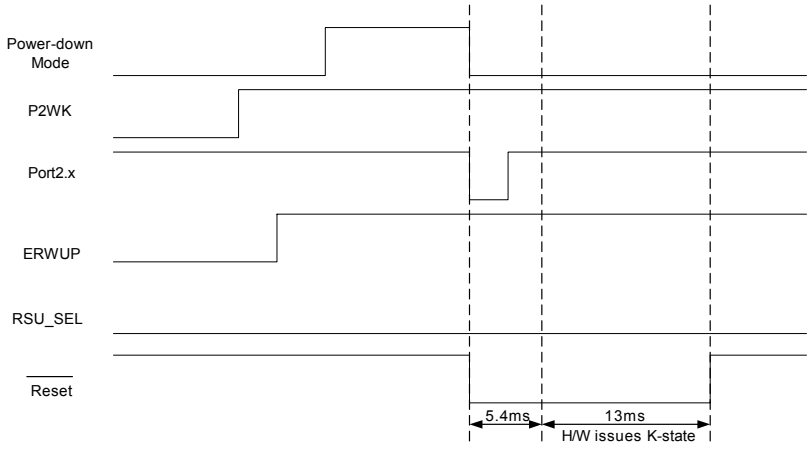


Figure 5-7. Select H/W Issues K-State by Resume Ports Reset

Port resume reset example 2: Assume that PORT2 is resume source and F/W issue K-State when Resume Reset occurs.

```
PWRDN_FW：
        MOV     PORT2  #FFH    ; initialize PORT2 resume source to be high.
        MOV     P2WK   #FFH    ; Enable PORT2 resume ability.
        MOV     PORT0  #00H    ; Pull low PORT0.
        MOV     P0WK   #00H    ; Disable PORT0 resume ability.
        ORL     DFC    #10H    ; RSU_SEL = 1, FW issue K-State
        ORL     DFC,   #02H    ; ERWUP = 1, Enable Remote Wake Up function.
        MOV     CLRWDT #55H    ; Clear Watch-Dog Timer.
        ORL     PCON   #02H    ; Set POWER DOWN mode.
        MOV     SUSLO  #55H    ; Enter POWER DOWN mode.
        NOP                    ; 3 NOP instruction (make sure program will executes properly)
        NOP
        NOP
```

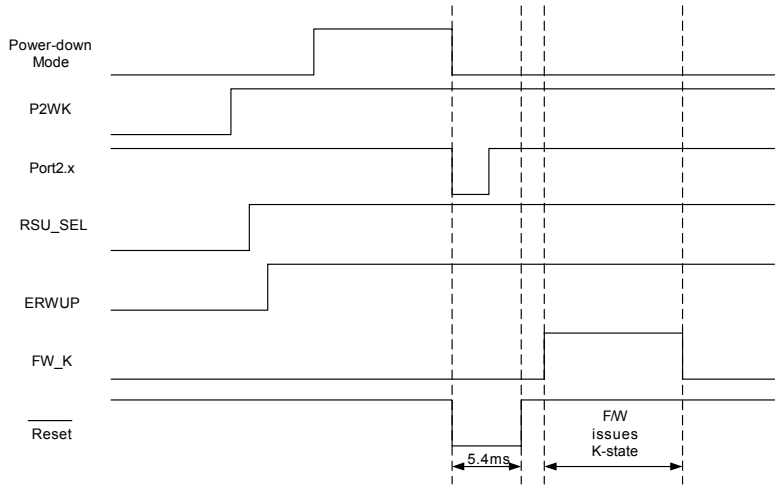


Figure 5-8. Select F/W Issues K-State by Resume Ports Reset

Wake-up Timer time out resume reset

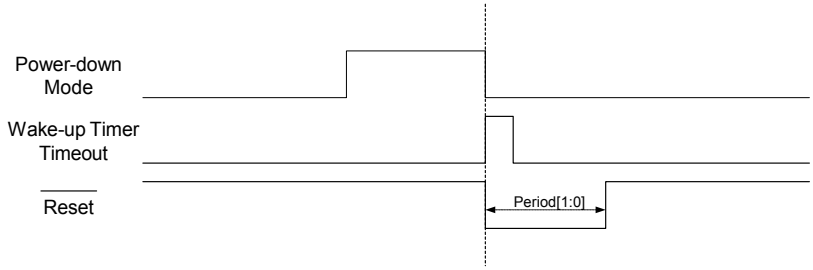


Figure 5-9. Wake-up Timer time out waveform

USB Bus Non-idle state resume reset

■ Resume reset after Non-idle event

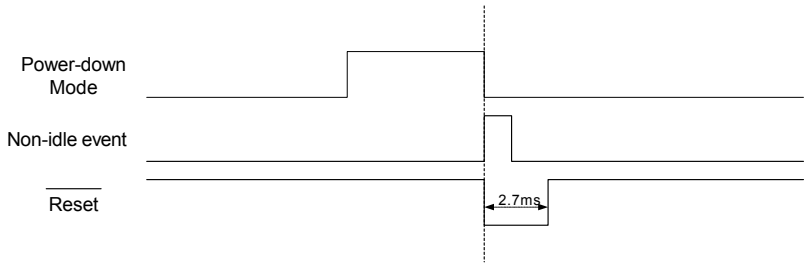


Figure 5-10. USB Non-idle resume reset waveform

■ USB reset signal at Power-down mode

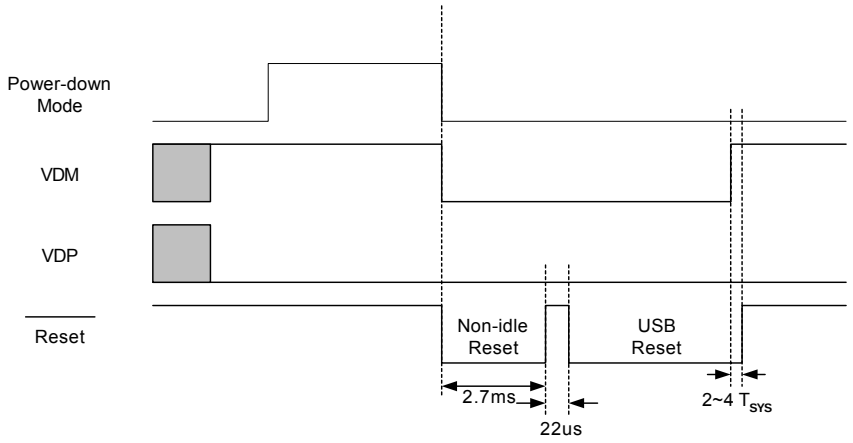


Figure 5-11. USB Reset wake-up waveform

5.4. Wake-up Timer

- The XA2001 has a Built-in 32KHz Ring-Oscillator. It is the clock source of wake-up timer. The 32KHz Ring-Oscillator will start when the control register **WKT[3:2]** was not equal to #00b.
- The wake-up timer can only be enabled/disabled by **WKT[3:0]** (**WKT[3:0]** not equal to 00xxb).
- If the Wake-up timer is enabled and system enter idle/power-down mode, the wake-up timer will load the time-out period register **WKT[3:0]** and start to count.

0095H	WKT_CON	Initial Value	Wake-up Timer & Resume Reset Control Register	
Bit [7:6]	-	00b	-	Reserved
Bit [5:4]	Period [1:0]	10b	R/W	**Internal Resume Reset period for Power-Down mode** (these times do not include resonator start-up time) 00: 2^{10} TSYS (170us) 01: 2^{11} TSYS (340us) 10: 2^{16} TSYS (10.922ms) 11: 2^{17} TSYS (21.845ms) **Reset source: Hardware reset**
Bit [3:0]	WKT [3:0]	0000b	R/W	**Wake-up timer** 00xx: disable Wake-up timer under **Power-down mode** or **IDLE mode** Others: enable Wake-up timer under **Power-down mode** or **IDLE mode** 0101: Reserved 0110: 2^{7} TRING (4ms@ 32KHz) 0111: 2^{8} TRING (8ms@ 32KHz) 0100: 2^{9} TRING (16ms@ 32KHz) 1001: 2^{10} TRING (32ms@ 32KHz) 1010: 2^{11} TRING (64ms@ 32KHz) 1011: 2^{12} TRING (128ms@ 32KHz) 1000: 2^{13} TRING (256ms@ 32KHz) 1101: 2^{14} TRING (512ms@ 32KHz) 1110: 2^{15} TRING (1.024s@ 32KHz) 1111: 2^{16} TRING (2.048s@ 32KHz) 1100: 2^{17} TRING (4.096s@ 32KHz) **Reset source: Hardware reset**

5.5 MODE_FG Flag

0096H	MODE_FG	Initial Value	Mode Register	
Bit 7	-	0b	-	Reserved
Bit 6	Nonidle	0b	R/W	USB bus flag. Write “0” to clear, write “1” no effect. 1: set by non-idle event **Reset source: Hardware reset or USB reset**
Bit 5	WKUPT	0b	R/W	Set “1” after wake-up timer time-out. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset or USB reset**
Bit 4	RES_TRG	0b	R/W	“1”: Remote wake up; “0”: Global wake up. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset or USB reset**
Bit 3	WDT	0b	R/W	Set “1” after Watchdog reset. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset or USB reset**
Bit 2	USBRST	0b	R/W	Set “1” after USB reset. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset**
Bit 1	POF	1b	R/W	Set “1” after power-on reset, Low voltage reset and External reset. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset**
Bit 0	SUSF	0b	R/W	Set “1” when entering Power-down mode. Write “0” to clear, write “1” no effect. **Reset source: Hardware reset or USB reset**

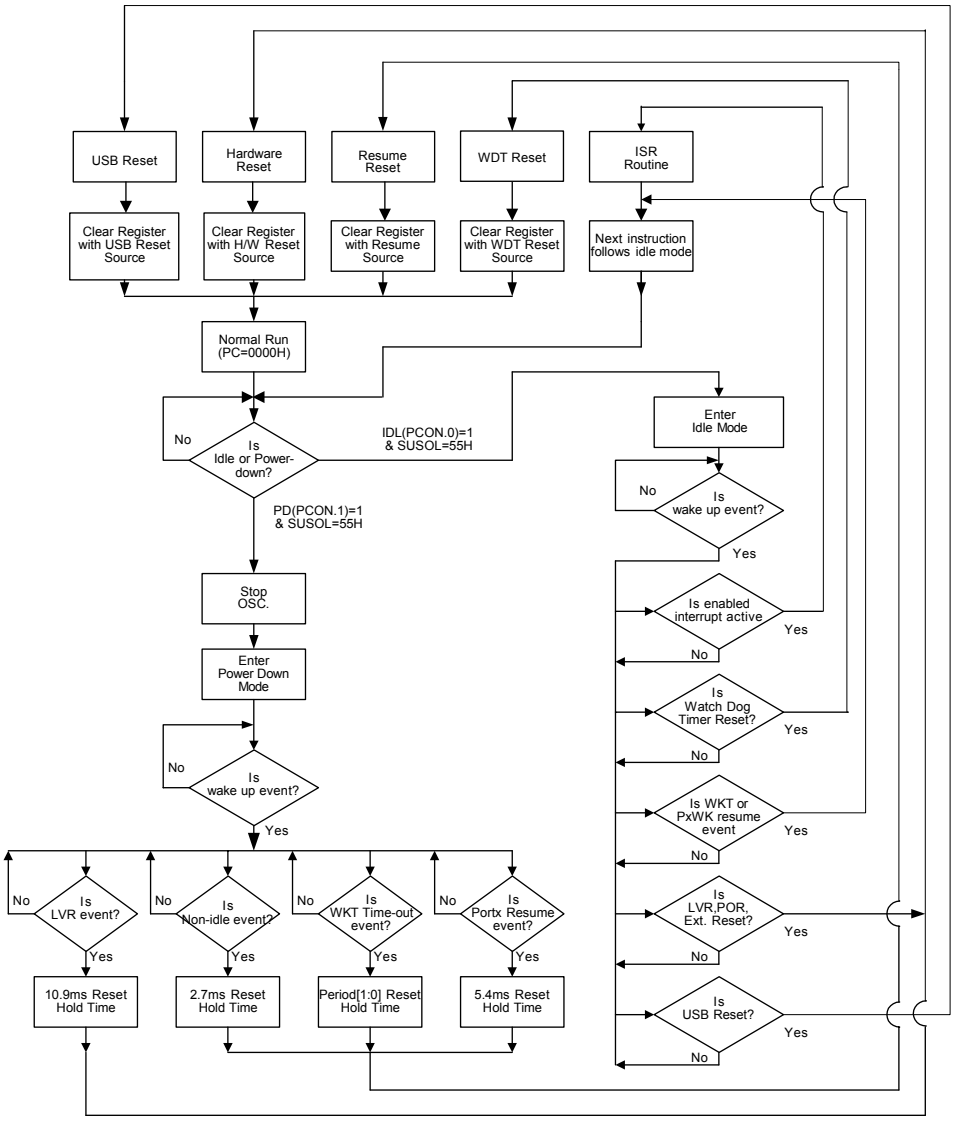


Figure 5-12. Event for exit from idle and power down mode

6. Input/Output Ports

6.1. Port-0 Configuration: (Reset source: Hardware reset)

I/O Port	Function	I/O	Circuit Structure	Control Bits		Description
				P0.x	P0CON.x	
Port0 [7:0]	Port0	I/O	Shown in Figure 6-1	0	0	Output Low (0.4V, min: 5mA)
				1	0	Output High (determined by **PHCON0**)
		I		X	1	HI-Z

Note: *P02 and P03 have the Schmitt trigger functions.*

6.2. Port-1 Configuration: (Reset source: Hardware reset)

I/O Port	Function	I/O	Circuit Structure	Control Bits		Description
				P1.x	P1CON.x	
Port1 [7:0]	Port1	I/O	Shown in Figure 6-1	0	0	Output Low (0.4V, min: 5mA)
				1	0	Output High (determined by **PHCON1**)
		I		X	1	HI-Z

Note: *P15 and P16 have the Schmitt trigger functions.*

6.3. Port-2 Configuration: (Reset source: Hardware reset)

I/O Port	Function	I/O	Circuit Structure	Control Bits		Description
				P2.x	P2CON.x	
Port2 [7:0]	Port2	I/O	Shown in Figure 6-1	0	0	Output Low (0.4V, min: 5mA)
				1	0	Output High (determined by **PHCON2**)
		I		X	1	HI-Z

6.4. Port-3 Configuration: (Reset source: Hardware reset)

I/O Port	Function	I/O	Circuit Structure	Control Bits			Description
				P3.x	P3CON.x	P3SEL.x	
Port3 [5], Port3 [3:0]	Port3	I/O	Shown in Figure 6-2	0	0	0	Output Low (0.4V, min: 5mA)
				1	0	0	Output High (determined by **PHCON3**)
				0	0	1	Output Low (2.6V - 3.2V, typ: 12mA)
				1	0	1	Output High (determined by **PHCON3**)
		I		X	1	X	HI-Z

I/O Port	Function	I/O	Circuit Structure	Control Bits			Description
				P3.x	P3CON.x	P3SEL.x	
Port3 [7:6]	Port3	I/O	Shown in Figure 6-2	0	0	0	Output Low (0.4V, min: 5mA)
				1	0	0	Output High (determined by **PHCON3**)
				0	0	1	Output Low (1.0V - 1.2V, typ: 20mA)
				1	0	1	Output High (determined by **PHCON3**)
		I		X	1	X	HI-Z

6.5. Port-4 Configuration: (Reset source: Hardware reset)

I/O Port	Function	I/O	Circuit Structure	Control Bits			Description
				P4.x	P4CON.x	P4SEL.x	
Port4 [2:0]	Port4	I/O	Shown in Figure 6-2	0	0	0	Output Low (2.6V - 3.2V, typ: 12mA)
				1	0	0	Output High (determined by **PHCON4**)
				0	0	1	Output Low (0.4V, min: 5mA)
				1	0	1	Output High (determined by **PHCON4**)
		I		X	1	X	HI-Z

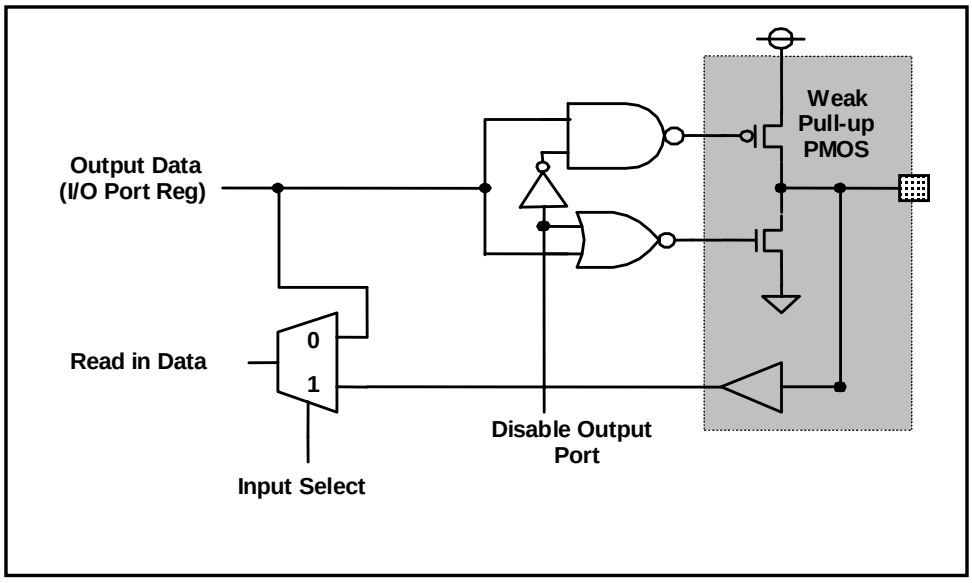


Figure 6-1. PORT Configuration-1

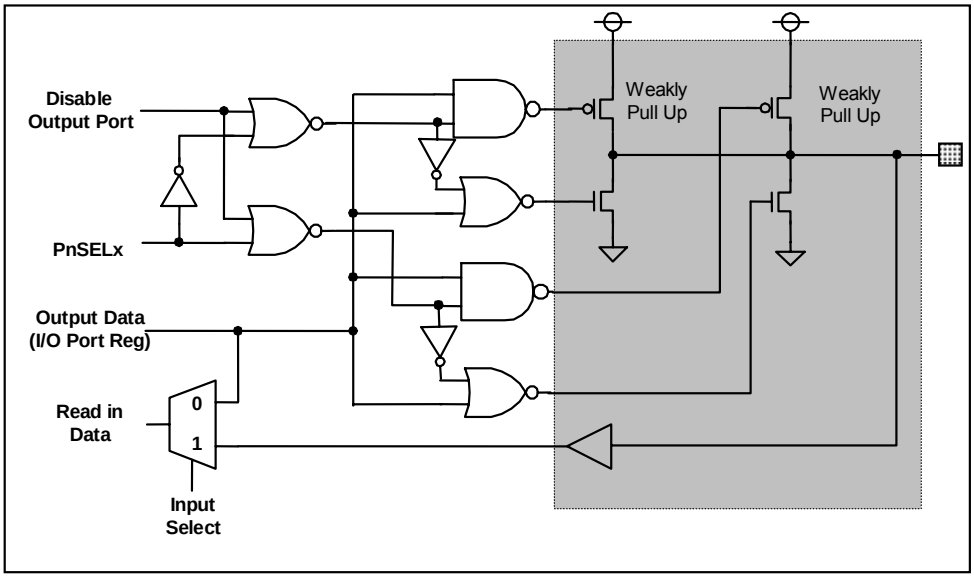


Figure 6-2. PORT Configuration-2

6.6. USB VDM/P46 Configuration: (Reset source: Hardware reset)

USB_CON	PULL_UP	VPCON	P46	P4CON6	Description
0	0	X	X	1	P46 output in Hi-Z mode, Read P46 will get the value on pad P46
0	1	X	X	1	1.5K ohm pull-up resistor active when bit “PULL_UP” = “1”, P46 in Hi-Z mode, Read P46 will get the value on pad P46
0	X	X	0	0	Output Low (0.4V, min: 8mA)
0	X	X	1	0	Output High (2.4V, min: -0.8mA)
1	X	0	X	X	USB Mode (VDM Pull-up by 1.5Kohm) Read P46 will get the value of “DM_I” signal on USB transceiver
1	X	1	X	X	USB Mode. Force Low (For pseudo Plug off)

Note 1: *Read Figure 6-3 for the general circuit diagram*
Note 2: *When entering USB Mode (USB_CON = 1) or P46 Output Mode (**P4CON6** = 0), **PULL_UP** function will be controlled by H/W automatically regardless of the value in the control bit (**PULL_UP**).*
Note 3: *P46 has the Schmitt trigger function.*

6.7. USB VDP/P45 Configuration: (Reset source: Hardware reset)

USB_CON	VPCON	P45	P4CON5	Description
0	X	X	1	P45 output in Hi-Z mode, Read P45 will get the value on pad P45
0	X	0	0	Output Low (0.4V, min: 8mA)
0	X	1	0	Output High (2.4V, min: -0.8mA)
1	0	X	X	USB Mode Read P45 will get the value of “DP_I” signal on USB transceiver
1	1	X	X	USB Mode. Force Low (Plug off)

Note 1: *Read Figure 6-3 for the general circuit diagram*
Note 2: *P45 has the Schmitt trigger function.*

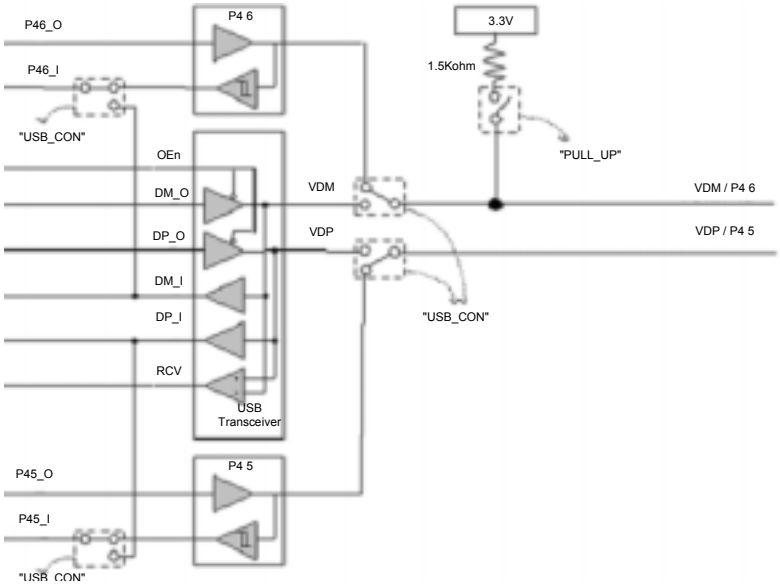


Figure 6-3. USB configuration

6.8. I/O Pull-high Driving ability Control Register

The pull-high current of Port0 - Port3, Port4[2:0] is determined by the SFR **PHCON**.

00A7H	PHCON	Initial Value	Port Pull High Control Register	
Bit [7:5]	-	000b	-	Reserved
Bit 4	PHCON4	0b	R/W	**Port4[2:0] Pull High Control bit** 0: determined by DRV_OUT[1:0] 1: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.) **Reset source: Hardware reset**
Bit 3	PHCON3	0b	R/W	**Port3 Pull High Control bit** 0: determined by DRV_OUT[1:0] 1: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.) **Reset source: Hardware reset**
Bit 2	PHCON2	0b	R/W	**Port2 Pull High Control bit** 0: determined by DRV_OUT[1:0] 1: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.) **Reset source: Hardware reset**
Bit1	PHCON1	0b	R/W	**Port1 Pull High Control bit** 0: determined by DRV_OUT[1:0] 1: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.) **Reset source: Hardware reset**
Bit 0	PHCON0	0b	R/W	**Port 0 Pull High Control bit** 0: determined by DRV_OUT[1:0] 1: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.) **Reset source: Hardware reset**

6.9. Code option

To support Carbon-Line membrane, user can configure the driving high ability of Port0~Port3 and Port4.0~Port4.2 via Code option DRV_OUT [1:0]

DRV_OUT [1:0]:

00: 50uA (Min.) ~70uA (Typ.) ~100uA (Max.)

01: 8uA (Typ.)

10: 4uA (Typ.)

11: 2uA (Typ.)

For detail, please refer to the DC specification.

7. Interrupts

7.1. Interrupt Enables

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the SFR named **IE**, **IE2**, **IRQEN**, **IRQEN2**. The register **IE** also contains a global disable bit, which can be cleared to disable all interrupts at once. Figure 7-1 shows the interrupt register for the XA2001.

Interrupt Enable Register

00A8H	IE	Initial Value	Interrupt Enable Register	
Bit 7	EA	0b	R/W	**Disable all interrupts.** If EA = 0, no any interrupts will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit. **Reset Source: Hardware reset, USB reset or WDT reset**
Bit 6	-	0b	-	Reserved
Bit 5	-	0b	-	Reserved
Bit 4	ETC0	0b	R/W	Time Capture0 interrupt
Bit 3	ET1	0b	R/W	Base Timer1 interrupt
Bit 2	-	0b	-	Reserved
Bit 1	ET0	0b	R/W	Base Timer0 interrupt
Bit 0	EEXT0	0b	R/W	External interrupt0
Enable bit = 1, enables the interrupt **Enable bit = 0, disables the interrupt** **Reset source: Hardware reset or USB reset** ***Note:*** *EA bit will also be clear by WDT reset*				

00A9H	IE2	Initial Value	Interrupt Enable Register	
Bit 7	-	0b	-	Reserved
Bit 6	EFUN	0b	R/W	SUSP/OVL interrupt
Bit 5	ESIE	0b	R/W	SIE interrupt (NAKT0, NAKR0, NAK1, NAK2, T0STL, R0STL)
Bit 4	EOUT0	0b	R/W	Out0 interrupt
Bit 3	EIN0	0b	R/W	IN0 interrupt
Bit 2	EOT0ERR	0b	R/W	OT0ERR interrupt
Bit 1	EOWSTUP	0b	R/W	OWSTUP interrupt
Bit 0	ESTUP	0b	R/W	Setup interrupt
Enable bit = 1, enables the interrupt **Enable bit = 0, disables the interrupt** **Reset source: Hardware reset or USB reset**				

00DCH	IRQEN	Initial Value	SIE Interrupt Enable Register	
Bit 7	EIN2	0b	R/W	IN2 interrupt
Bit 6	EIN1	0b	R/W	IN1 interrupt
Bit 5	ER0STL	0b	R/W	R0 stall interrupt
Bit 4	ET0STL	0b	R/W	T0 stall interrupt
Bit 3	ENAK2	0b	R/W	T2 NAK interrupt
Bit 2	ENAK1	0b	R/W	T1 NAK interrupt
Bit 1	ENAKR0	0b	R/W	R0 NAK interrupt
Bit 0	ENAKT0	0b	R/W	T0 NAK interrupt
Enable bit = 1, enables the interrupt **Enable bit = 0, disables the interrupt** **Reset Source: Hardware reset or USB reset**				

00DDH	IRQEN2	Initial Value	FUN Interrupt Enable Register	
Bit 7	**-**	0b	**-**	Reserved
Bit 6	-	0b	**-**	Reserved
Bit 5	-	0b	-	Reserved
Bit 4	-	0b	-	Reserved
Bit 3	-	0b	-	Reserved
Bit 2	ESUSP	0b	R/W	Suspend interrupt (bus idle > 5ms)
Bit 1	EOVL	0b	R/W	OVL interrupt
Bit 0	-	0b	-	Reserved
Enable bit = 1, enables the interrupt **Enable bit = 0, disables the interrupt** **Reset Source: Hardware reset or USB reset**				

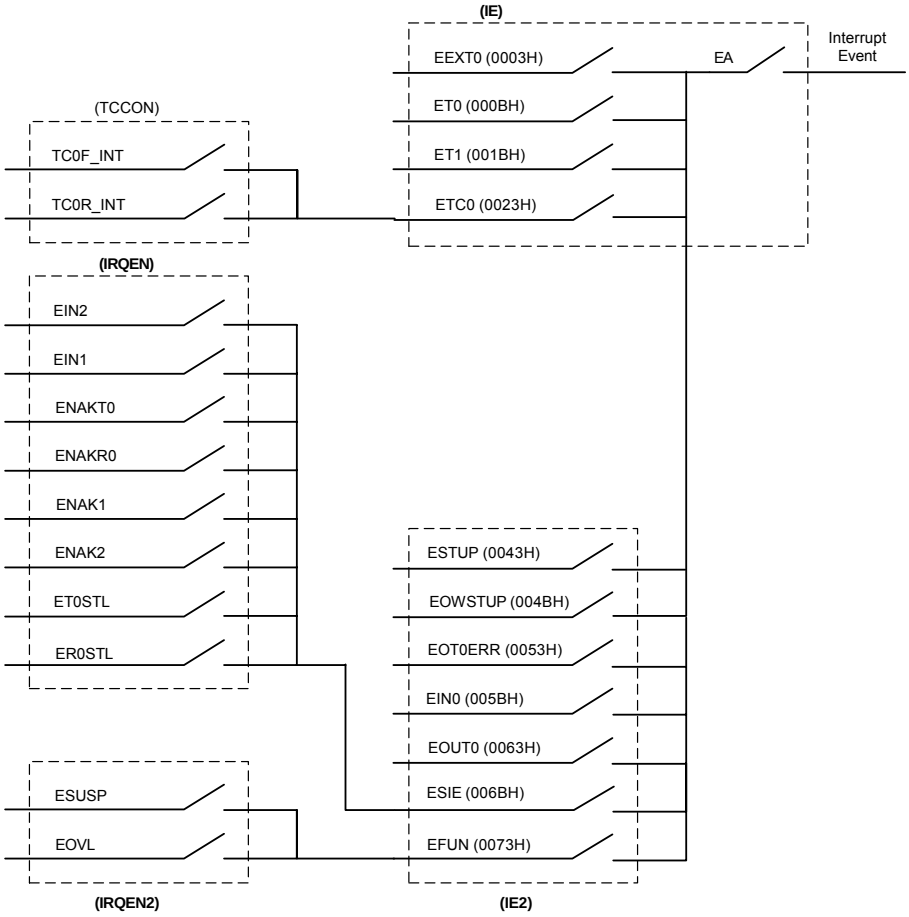


Figure 7-1. Interrupt Structure

7.2. Interrupt Priorities

- Each interrupt source can also be individually programmed to one of the two priority levels by setting or clearing a bit in the SFR named **IP** (Interrupt Priority) and **IP2**. The Following figure shows the **IP** & **IP2** register in the XA2001.
- Low-priority interrupt can be interrupted by a high-priority interrupt, but cannot be interrupted by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.
- If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests the same priority levels are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the software polling sequence.
- In operation, all the interrupt flags are latched into the interrupt control system every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is set to 1, the interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other condition blocks an interrupt, such as an interrupt of equal or higher priority level already in progress.
- The hardware-generated LCALL accesses the contents of the Program Counter pushed onto the stack, and reloads the PC with the beginning address of the service routine. As previously noted, the service routine for each interrupt begins at a fixed location.
- **Only the Program Counter is automatically pushed onto the stack, not the PSW or any other register.** Having only the PC automatically saved allows the programmer to decide how much time to spend saving other registers.

00B8H	IP	Initial Value	Interrupt Priority Register	
Bit 7	-	0b	-	Reserved
Bit 6	-	0b	-	Reserved
Bit 5	-	0b	-	Reserved
Bit 4	PTC0	0b	R/W	Time Capture0 interrupt priority bit
Bit 3	PT1	0b	R/W	Base Timer1 interrupt priority bit
Bit 2	-	0b	-	Reserved
Bit 1	PT0	0b	R/W	Base Timer0 interrupt priority bit
Bit 0	PEXT0	0b	R/W	External interrupt0 priority bit
1: high priority, 0: low priority **Reset Source: Hardware reset or USB reset**				

00B9H	IP2	Initial Value	Interrupt Priority Register	
Bit 7	-	0b	-	Not implemented (always 0)
Bit 6	PFUN	0b	R/W	SUSP/OVL interrupt priority bit
Bit 5	PSIE	0b	R/W	SIE interrupt priority bit (NAKT0, NAKR0, NAK1, NAK2, T0_STL, R0_STL, IN1, IN2)
Bit 4	POUT0	0b	R/W	Out0 interrupt priority bit
Bit 3	PIN0	0b	R/W	IN0 interrupt priority bit
Bit 2	POT0ERR	0b	R/W	OT0ERR interrupt priority bit
Bit 1	POWSTUP	0b	R/W	OWSTUP interrupt priority bit
Bit 0	PSTUP	0b	R/W	Setup interrupt priority bit
1: high priority, 0: low priority **Reset Source: Hardware reset or USB reset**				

7.3. Interrupt Flag

00DAH	IF1	Initial Value	Interrupt Control Flag	
Bit [7:5]	-	0b	-	Reserved
Bit 4	TC0	0b	R/W	**Time Capture 0 Interrupt flag**. Set by hardware when the eight bits are received or end condition is detected. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 3	T1	0b	R/W	**Base Timer 1 Interrupt flag**. Set by hardware when the Base timer1 overflow is detected. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 2	-	0b	-	Reserved
Bit 1	T0	0b	R/W	**Base Timer 0 Interrupt flag**. Set by hardware when the Base Timer0 over flow is detected. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 0	EXT0	0b	R/W	**External Interrupt 0 flag**. Set by hardware when the P46 falling edge signal is detected. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**

00DBH	IF2	Initial Value	Interrupt Control Flag	
Bit 7	-	0b	-	Reserved
Bit 6	FUN	0b	R/W	**FUN Interrupt flag**. Set by hardware when an invalid program ROM address is detected or the idle time of USB bus large then 5ms. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 5	SIE	0b	R/W	When OUT0, IN0, IN1 or IN2 is responded by a NAK, responds ACK to IN1, IN2 or responds STALL to IN0 or OUT0 tokens, SIE will be set. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 4	OUT0	0b	R/W	When OUT token for endpoint 0 is done, it will set the OUT0 flag. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 3	IN0	0b	R/W	When IN token for endpoint 0 is done, it will set the IN0 flag. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 2	OT0ERR	0b	R/W	When an Out token with wrong data sequence is received, OT0ERR will be set 1. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 1	OWSTUP	0b	R/W	When a receiving setup token overwrites the existing data in FIFO, R0_OW will set 1. After the overwriting setup packet is received and a following IN or OUT token happens, OWSTUP is set. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 0	STUP	0b	R/W	When a SETUP TOKEN for endpoint 0 is done, it will set the STUP flag. Cleared by hardware when interrupt is processed. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**

00DEH	IRQFG	Initial Value	Interrupt Control Flag	
Bit 7	IN2	0b	R/W	When IN token for endpoint 2 is done, it will set the IN2 flag. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 6	IN1	0b	R/W	When IN token for endpoint 1 is done, it will set the IN1 flag. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 5	R0STL	0b	R/W	When XA2001 responds STALL to OUT0 tokens, R0_STL will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 4	T0STL	0b	R/W	When XA2001 responds STALL to IN0 tokens, T0_STL will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 3	NAK2	0b	R/W	When IN2 is responded by a NAK, NAK2 will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 2	NAK1	0b	R/W	When IN1 is responded by a NAK, NAK1 will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 1	NAKR0	0b	R/W	When OUT0 is responded by a NAK, NAKR0 will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 0	NAKT0	0b	R/W	When IN0 is responded by a NAK, NAKT0 will be set. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**

00DFH	IRQFG2	Initial Value	Interrupt Control Flag	
Bit 7	-	0b	-	Reserved
Bit 6	-	0b	-	Reserved
Bit 5	-	0b	-	Reserved
Bit 4	-	0b	-	Reserved
Bit 3	-	0b	-	Reserved
Bit 2	SUSP	0b	R/W	When USB SIE detects a bus idle state (J state > 5ms), its sets the SUSP Flag. Write “0” to clear, write “1” no effect **Reset Source: Hardware reset or USB reset**
Bit 1	OVL	0b	R/W	OVL Interrupt 1 flag. Set by hardware when an invalid program ROM address is detected. Write “0” to clear, write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 0	-	0b	-	Reserved

8. Base Timer

- The Timer-x is an 8-bit counter with a programmable clock source selection and the value of Base Timer-x counter can be read out any time.(x=0,1)
- The Base Timer-x can be enabled/disabled by the CPU. After reset, the Base Timer-x is disabled and cleared.
- The Base Timer-x can be preset by writing a preset value to BTx register at any time. When the Base Timer-x is enabled, the Base Timer-x starts counting from the preset value to FFH and when the values reaches 00H, it generates a Base Timer-x interrupt if the Base Timer-x interrupt is enabled. When it reaches 00H, the Base Timer-x will auto-load the value in BTx register and begin counting.
- The Base Timer-x can be enabled by writing a "1" to "ENBTx" in the **BTCON** (Base Timer Control) register. The ENBTx is level trigger. If any value is written to **BTx** register when it is counting, Base Timer-x will reload that value immediately and continue counting from that written value. Every time ENBTx goes rising, the counter begins to count from the preset value in **BTx** register.
- The input clock source of Base Timer-x is controlled by the BTxM[2:0] register. The following table shows 8 ranges of the Base Timer-x. For counting accuracy, please set the Base Timer-x register first, then preset the BTxM[2:0] register, last, enable the Base Timer-x.

00D2H	BT0	Initial Value	Base Timer-0 Control Register	
Bit [7:0]	BT0 [7:0]	00h	R/W	Base Timer-0 register **Reset Source: Hardware reset or USB reset**

00D3H	BT1	Initial Value	Base Timer-1 Control Register	
Bit [7:0]	BT1 [7:0]	00h	R/W	Base Timer-1 register **Reset Source: Hardware reset or USB reset**

00D4H	BTCON	Initial Value	Base Timer Control Register	
Bit 7	ENBT1	0b	R/W	0: Disable Base Timer-1 1: Enable Base Timer-1 **Reset Source: Hardware reset or USB reset**
Bit [6:4]	BT1M [2:0]	000b	R/W	**Base Timer-1 clock source** 000: $F_{BT}/2^0$ 001: $F_{BT}/2^1$ 010: $F_{BT}/2^2$ 011: $F_{BT}/2^3$ 100: $F_{BT}/2^4$ 101: $F_{BT}/2^5$ 110: $F_{BT}/2^6$ 111: $F_{BT}/2^7$ $F_{BT} = F_{SYS}/6$ **Reset Source: Hardware reset or USB reset**
Bit 3	ENBT0	0b	R/W	0: Disable Base Timer-0 1: Enable Base Timer-0 **Reset Source: Hardware reset or USB reset**
Bit [2:0]	BT0M [2:0]	000b	R/W	**Base Timer-0 clock source** 000: $F_{BT}/2^0$ 001: $F_{BT}/2^1$ 010: $F_{BT}/2^2$ 011: $F_{BT}/2^3$ 100: $F_{BT}/2^4$ 101: $F_{BT}/2^5$ 110: $F_{BT}/2^6$ 111: $F_{BT}/2^7$ $F_{BT} = F_{SYS}/6$ **Reset Source: Hardware reset or USB reset**

9. Time Capture 0

The XA2001 provide one set of Time Capture I/O pins, TC0, the Time Capture input provides both rising and falling edge 8 bits time register. A PreScaler allows TCAP0 to select 8 types of time capture tick size (From 2us to 16us).

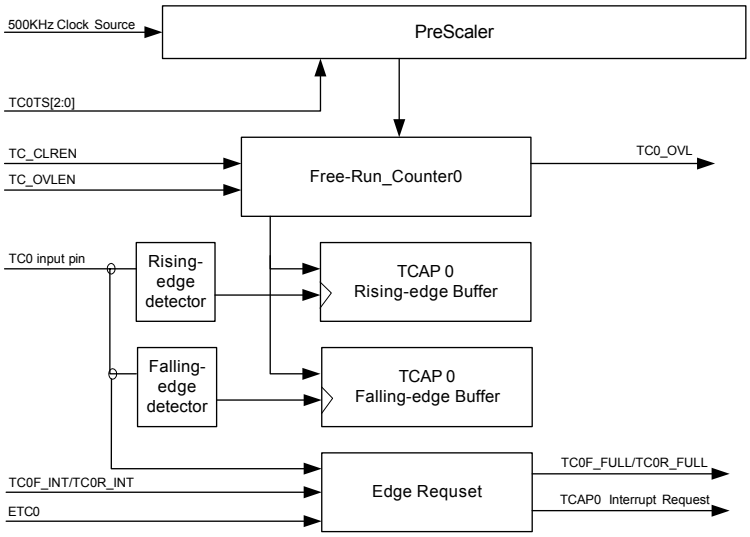


Figure 9-1. Function Block Diagram of Time Capture Function TCAP0

00CBH	TCAP0R	Initial Value	Time Capture 0 Rising-edge Register	
Bit [7:0]	TCAP0R [7:0]	00h	R	Time Capture 0 Rising-edge data register. **Reset Source: Hardware reset or USB reset**

00CCH	TCAP0F	Initial Value	Time Capture 0 Falling-edge Register	
Bit [7:0]	TCAP0F [7:0]	00h	R	Time Capture 0 Falling-edge data register. **Reset Source: Hardware reset or USB reset**

00C8H	TCSTU	Initial Value	Time Capture Status register	
Bit [7:5]	-	000b	-	Reserved
Bit4	TC0_OVL	0b	R/W	**Time Capture 0 (TCAP0) Over Flow flag.** TC0_OVL event will active If TC_CLREN = 1 & TC_OVLEN = 1 and the data width on TC0 pad is longer than TCAP0 free-run counter. TCAP0 free-run counter will count continuously. Write '0' to clear TC0_OVL flag, write '1' no effect. **Reset Source: Hardware reset or USB reset**
Bit [3:2]	-	00b	-	Reserved
Bit 1	TC0F_FULL	0b	R	**Time Capture 0 Falling Edge Register (TCAP0F) Full flag.** When TC0 pin get a falling-edge, TCAP0 free-run counter value will be load into TCAP0F and TC0F_FULL bit will be set to "1" also. This bit will be clear by hardware when firmware read a byte from TCAP0F. **Reset Source: Hardware reset or USB reset**
Bit 0	TC0R_FULL	0b	R	**Time Capture 0 Rising Edge Register (TCAP0R) Full flag.** When TC0 pin get a rising-edge, TCAP0 free-run counter value will be load into TCAP0R and TC0R_FULL bit will be set to "1" also. This bit will be clear by hardware when firmware read a byte from TCAP0R. **Reset Source: Hardware reset or USB reset**

00C9H	TCCON	Initial Value	Time Capture Control Register	
Bit [7:6]	-	00b	-	Reserved
Bit 5	TC_CLREN	0b	R/W	**Enable force clear TCAP0 free-run counter control bit** 0: TCAP0 free-run counter is continued. 1: Enable force clear TCAP0 free-run counter function. When force clear function enable, TCAP0 free-run counter is clear when a rising or falling edge is detected on TC0 pad. **Reset Source: Hardware reset or USB reset**
Bit 4	TC_OVLEN	0b	R/W	**Enable TC0_OVL event function** 0: Disable TC0_OVL event. 1: Enable TC0_OVL event. User can set both TC_CLREN and TC_OVLEN to detect the over-run event of TCAP0 free-run counter. **Reset Source: Hardware reset or USB reset**
Bit [3:2]	-	00b	-	Reserved
Bit 1	TC0F_INT	0b	R/W	**Enable Time Capture 0 falling-edge interrupt request.** When ETC0 = 1 & TC0F_INT = 1, the falling-edge on TC0 pad will cause an ETC0 IRQ. **Reset Source: Hardware reset or USB reset**
Bit 0	TC0R_INT	0b	R/W	**Enable Time Capture 0 rising-edge interrupt request.** When ETC0 = 1 & TC0R_INT = 1, the rising-edge on TC0 pad will cause an ETC0 IRQ. **Reset Source: Hardware reset or USB reset**

00CAH	TCSCALE	Initial Value	Time Capture Input Clock Scale Register	
Bit [7:4]	-	0000b	-	**Reserved**
Bit 3	-	0b	-	**Reserved**
Bit [2:0]	TC0TS[2:0]	000b	R/W	**Time Capture 0 free-run timer scale control**: 000: Select 2us time scale for TCAP0 free-run counter base timer 001: Select 4us time scale for TCAP0 free-run counter base timer 010: Select 6us time scale for TCAP0 free-run counter base timer 011: Select 8us time scale for TCAP0 free-run counter base timer 100: Select 10us time scale for TCAP0 free-run counter base timer 101: Select 12us time scale for TCAP0 free-run counter base timer 110: Select 14us time scale for TCAP0 free-run counter base timer 111: Select 16us time scale for TCAP0 free-run counter base timer **Reset Source: Hardware reset or USB reset**

Following figures show how Time Capture function works on TC0 input signal with different H/W setting condition

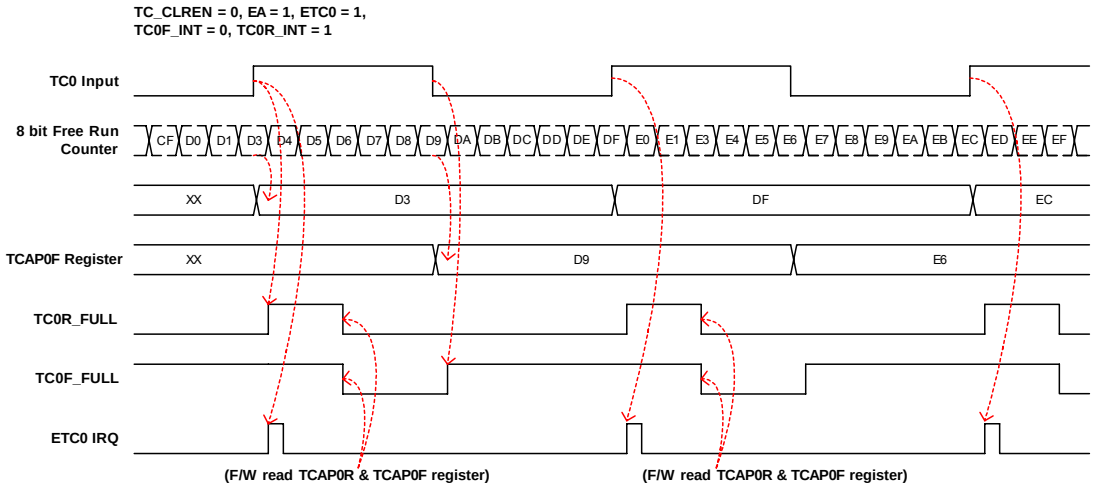


Figure 9-2. Timing Diagram of TC0 #1

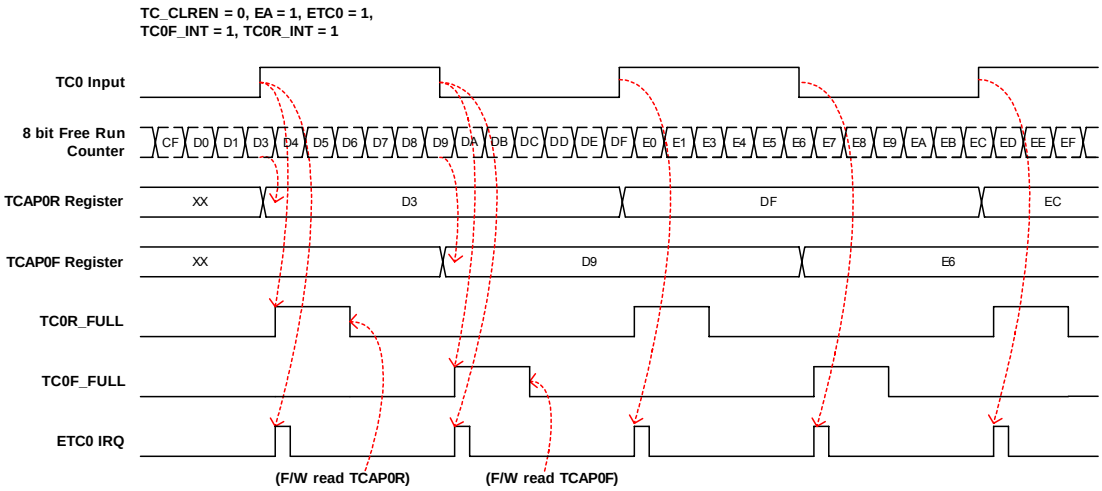


Figure 9-3. Timing Diagram of TC0 #2

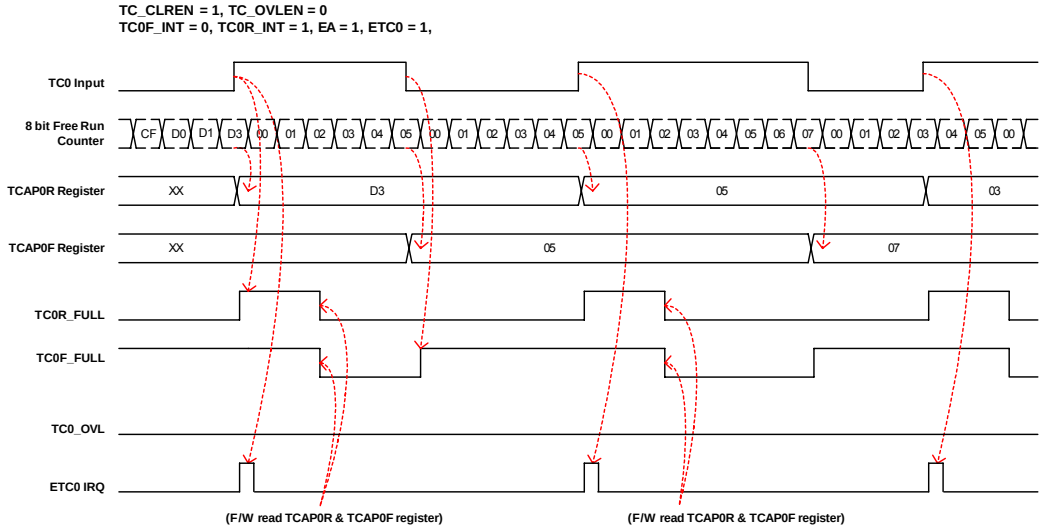


Figure 9-4. Timing Diagram of TC0 #3

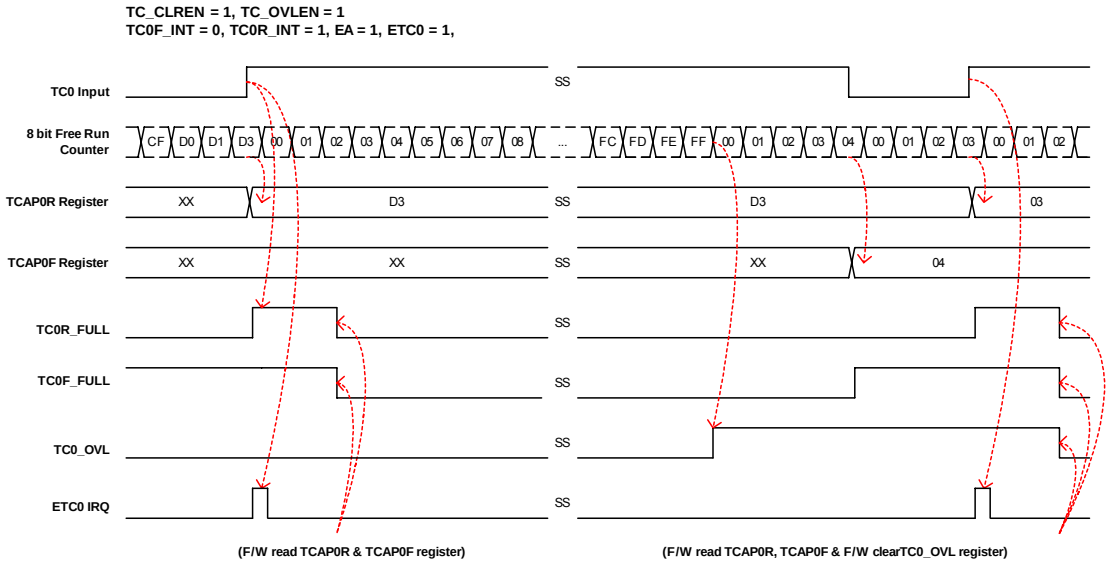


Figure 9-5. Timing Diagram of TC0 #4

10. USB Control Register

10.1. DADDR

USB Device Address Register

00F2H	DADDR	Initial Value	Device Address Register	
Bit 7	-	0B	-	Reserved
Bit [6:0]	DADDR [6:0]	0000000B	R/W	USB Device address **Reset Source: Hardware reset or USB reset**

10.2. DFC

USB Feature Control Register

00F3H	DFC	Initial Value	Device Feature Control Register	
Bit 7	PULL_UP	0B	R/W	**Internal 1.5K ohm pull up resistor On/Off control** 0: Disable internal USB D- pad 1.5K ohm pull-up resistor 1: Enable internal USB D- pad 1.5K ohm pull-up resistor This F/W controlled function will be mask and is controlled by H/W if USB Mode was enabled (USB_CON = 1) **Reset Source: Hardware reset**
Bit 6	USB_CON	0B	R/W	0: Enable GPIO Mode 1: Enable USB Mode **Reset Source: Hardware reset**
Bit 5	FW_K	0B	R/W	0: FW stops issuing K-state on USB bus 1: FW starts to issue K-state on USB bus **Reset Source: Hardware reset or USB reset**
Bit 4	RSU_SEL	0B	R/W	0: Enable HW to response RESUME by issuing K-state 1: Disable HW to response RESUME by issuing K-state **Reset Source: Hardware reset or USB reset**
Bit 3	USBEN	0B	R/W	After power on, USBEN is reset to 0. USBEN will be set to 1 after HOST issues USB reset and then the device starts to respond USB commands. This bit can be also read and written by F/W. 0: Disable USB functions 1: Enable USB functions **Reset Source: Hardware reset**
Bit 2	-	0B	-	Reserved
Bit 1	ERWUP	0B	R/W	**Remote Wake Up Enable Bit** 0: Disable remote wake-up 1: Enable remote wake-up ERWUP can be returned by SETUP command - GetStatus ( ) to a device ERWUP can be set by SETUP command - ClearFeature (DEVICE_REMOTE_WAKEUP) and SetFeature (DEVICE_REMOTE_WAKEUP). For remote wake-up function, H/W designer and F/W programmer must follow the below notes. Remote wake bit in DFC register can only be set/reset by HOST. **Reset Source: Hardware reset or USB reset**
Bit 0	VPCON	1B	R/W	**USB Virtual Plug-off Control** 0: Perform USB plug-in only if the device is disconnected 1: Perform USB pseudo plug-off **Reset Source: Hardware reset**

10.3. TXDATx

USB Transmit FIFO Data Register, x = 0/1/2 for Endpoint 0/1/2. The byte count of the transmitted data must be equal to or less than 8.

00EAH	TXDAT0	Initial Value	USB TX FIFO 0 Data Register	
Bit [7:0]	TXDAT0 [7:0]	XXH	W	Transmit FIFO 0 **Reset Source: no reset source**

00E2H	TXDAT1	Initial Value	USB TX FIFO 1 Data Register	
Bit [7:0]	TXDAT1 [7:0]	XXH	W	Transmit FIFO 1 **Reset Source: no reset source**

00E5H	TXDAT2	Initial Value	USB TX FIFO 2 Data Register	
Bit [7:0]	TXDAT2 [7:0]	XXH	W	Transmit FIFO 2 **Reset Source: no reset source**

10.4. TXCNTx

USB FIFO Transmit Bytes Count Register, x = 0/1/2 for Endpoint 0/1/2. The firmware writes the corresponding bytes count to this register after writing data to the **TXDATx**.

00EBH	TXCNT0	Initial Value	USB TX FIFO 0 Bytes Count Register	
Bit [7:4]	-	0000B	-	Reserved
Bit [3:0]	TXCNT0 [3:0]	XXXXB	W	TX FIFO 0 Transmit Bytes Count **Reset Source: no reset source**

00E3H	TXCNT1	Initial Value	USB TX FIFO 1 Bytes Count Register	
Bit [7:4]	-	0000B	-	Reserved
Bit [3:0]	TXCNT1 [3:0]	XXXXB	W	TX FIFO 1 Transmit Bytes Count **Reset Source: no reset source**

00E6H	TXCNT2	Initial Value	USB TX FIFO 2 Bytes Count Register	
Bit [7:4]	-	0000B	-	Reserved
Bit [3:0]	TXCNT2 [3:0]	XXXXB	W	TX FIFO 2 Transmit Bytes Count **Reset Source: no reset source**

10.5. TXFLGx

USB Transmit FIFO Flag/Control Register, x = 0/1/2 for Endpoint 0/1/2.

00ECH	TXFLG0	Initial Value	USB TX FIFO 0 Flag/Control Register	
Bit [7:2]	-	000000B	-	Reserved
Bit 1	STLT0	0	R/W	**Pipe 0 stall bit** 0: SIE responds ACK, NAK or not respond to pipe 0 IN token 1: STLT0 bit is used to stall the pipe 0 IN token. SIE will respond STALL to pipe 0 IN token as long as STLT0 bit is set **Reset source: Hardware reset or USB reset**
Bit 0	T0FULL	0	R/W	**TXDAT0 FIFO full status bit**. F/W writes “1” to set H/W FIFO pointer. Clear to “0” by H/W after receiving ACK from host. 0: empty 1: full **Reset Source: Hardware reset or USB reset**

00E4H	TXFLG1	Initial Value	USB TX FIFO 1 Flag/Control Register	
Bit [7:4]	-	0000B	-	Reserved
Bit 3	T1EPE	0b	R/W	**This bit is used to enable/disable the endpoint 1** 1: Enable endpoint 1 0: Disable, the corresponding endpoint does not respond to a valid IN Token **Reset source: Hardware reset or USB reset**
Bit 2	T1SEQC	0b	W	The data sequence of each transmitted data packet is controlled by hardware and is toggled after receiving ACK from host. The F/W can reset the data sequence by writing "1" to T1SEQC for resetting the next transmitting data sequence on endpoint 1. Write "0" to no effect. Read this bit will always get value with "0" **Reset source: Hardware reset or USB reset**
Bit 1	STLT1	0b	R/W	**Pipe 1 stall bit**, this bit is used to stall the pipe 1. STL1 is set by SETUP command - SetFeature (ENDPOINT_HALT) and STL1 is reset by SETUP command - ClearFeature (ENDPOINT_HALT). 0: responds ACK, NAK or not respond to IN1 1: STLT1 bit is used to stall the pipe 1 IN token. SIE will respond STALL to Host IN token as long as STLT1 bit is set **Reset source: Hardware reset or USB reset**
Bit 0	T1FULL	0b	R/W	**TXDAT1 FIFO full status bit**. F/W writes "1" to set H/W FIFO pointer. Clear to "0" by H/W after receiving ACK form host. 0: Empty 1: Full **Reset Source: Hardware reset, USB reset**

00E7H	TXFLG2	Initial Value	USB TX FIFO 2 Flag/Control Register	
Bit [7:4]	-	0000B	-	Reserved
Bit 3	T2EPE	0b	R/W	**This bit is used to enable the endpoint 2**. 1: Enable endpoint 2 0: Disable, the corresponding endpoint does not respond to a valid IN Token **Reset source: Hardware reset or USB reset**
Bit 2	T2SEQC	0b	W	The data sequence of each transmitted data packet is controlled by hardware and is toggled after receiving ACK from host. The F/W can reset the data sequence by writing "1" to T2SEQC for resetting the next transmitting data sequence on endpoint 2. Write "0" to no effect. Read this bit will always get value with "0" **Reset source: Hardware reset or USB reset**
Bit 1	STLT2	0b	R/W	**Pipe 2 stall bit**, this bit is used to stall the pipe 2. STL2 is set by SETUP command - SetFeature(ENDPOINT_HALT) and STL2 is reset by SETUP command - ClearFeature (ENDPOINT_HALT). 0: responds ACK, NAK or not respond to IN2 1: STLT2 bit is used to stall the pipe 2 IN token. SIE will respond STALL to Host IN token as long as STLT2 bit is set **Reset source: Hardware reset or USB reset**
Bit 0	T2FULL	0b	R/W	**TXDAT 2 FIFO full status bit**. F/W writes "1" to set H/W FIFO pointer. Clear to "0" by H/W after receiving ACK form host. 0: Empty 1: Full **Reset Source: Hardware reset or USB reset**

The TX FIFO operational model refers to Figure10-1.

In the following, the related F/W procedures and H/W actions are described.

(1) After Hardware Reset or USB Reset, the **TxFULL** bit in **TXFLGx** will reset to 0 to announce no data in FIFOs (x = 0/1/2).

(2) F/W save EA value (PUSH IE), and disables Interrupt (clear EA = 0).

(3) F/W writes up to n bytes of data to the **TXDATx** FIFO. (n = 0-8)

(4) F/W writes data byte count to the corresponding **TXCNTx** register.

(5) F/W sets the **TxFULL** bit.

(6) F/W restores the EA value (POP IE).

(7) SIE issues data from the corresponding FIFO byte-by-byte after SIE receives a valid corresponding IN transaction.

(8) SIE waits the ACK.

(9) After SIE receives ACK package successively, the **TxFULL** bit is then reset to 0 by H/W. If SIE don't receive ACK, **TxFULL** is on its original status.

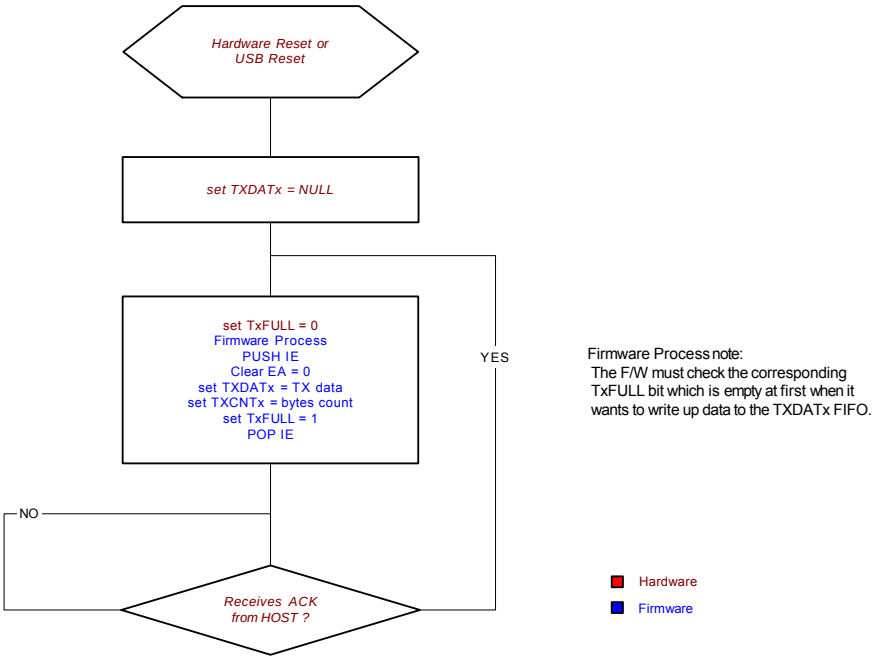


Figure 10-1. TX FIFO Operating Model (for a valid IN Transaction)

10.6. RXDAT0

USB Receive FIFO Data Register for Endpoint 0.SIE writes data to the RXDAT0 FIFO for Endpoint 0. CPU read data from the RXDAT0 for Endpoint 0. The operational model refers to Figure 10-2.

00EDH	RXDAT0	Initial Value	USB RX FIFO 0 Data Register	
Bit [7:0]	RXDAT0 [7:0]	XXH	R	RX FIFO Data Register for Endpoint 0 **Reset Source: no reset source**

10.7. RXCNT0

USB Received FIFO bytes count register for Endpoint 0. SIE writes the corresponding bytes count to this register after writing data to the RXDAT0.

00EEH	RXCNT0	Initial Value	USB RX FIFO 0 Bytes Count Register	
Bit [7:4]	-	0000B	-	Reserved
Bit [3:0]	RXCNT0 [3:0]	XXXXB	W	RX FIFO bytes count register for Endpoint 0 **Reset Source: no reset source**

10.8. RXFLG0

USB Receive FIFO Flag/Control Register for Endpoint 0

00EFH	RXFLG0	Initial Value	USB RX FIFO Flag/Control Register	
Bit [7:6]	-	00B	-	Reserved
Bit 5	RXERR	0B	R/W	**Receiving error on pipe 0**. When device receives a DATA packet with CRC or bit stuffing errors, this bit is set. Write “0” to clear, Write “1” no effect. **Reset Source: Hardware reset or USB reset**
Bit 4	R0_OW	0B	R	This bit is set as long as receiving FIFO is corrupted by setup token **Reset Source: Hardware reset or USB reset**
Bit 3	R0SEQ	0B	R	**The data toggle bit of receiving transaction on pipe 0**. This bit is updated by hardware as long as pipe 0 receives a setup or out transaction. **Reset Source: Hardware reset or USB reset**
Bit 2	OUT0ENB	0B	R/W	0: The device will receive the data of OUT0 packet when RX FIFO 0 is empty and respond ACK if no bit stuffing error or CRC error. 1: The XA2001 will respond OUT0 token with NAK. **Reset Source: Hardware reset or USB reset**
Bit 1	STLR0	0B	R/W	**Pipe 0 stall bits**. STLR0 bit is used to stall the pipe 0 OUT token. 0: responds ACK, NAK or not respond to OUT token. 1: SIE will respond STALL to HOST OUT token. **Reset Source: Hardware reset or USB reset**
Bit 0	R0FULL	0B	R/W	**RXDAT0 FIFO full bit**. Set to “1” by H/W when the RX FIFO 0 fills with valid data. 0: Empty. 1: Full. Write “0” to clear, Write “1” no effect. **Reset Source: Hardware reset or USB reset**

10.9. CRWCON

EP0 Control Read/Write Function Control Register

00E9H	CRWCON	Initial Value	EP0 Control Read/Write Setup Register	
Bit [7:3]	-	00000B	-	**Reserved**
Bit 2	CRSEQ	0B	R/W	Select “Valid OUT0 Token” for “STLCR” as Data 1 or Data 0/1. 0: “Valid OUT0 Token” include both OUT Token with “Data 1” & “Data 0” 1: “Valid OUT0 Token” means only OUT Token with “Data 1” **Reset Source: Hardware reset, USB reset, SETUP**
Bit 1	STLCR	0B	R/W	1: Enable H/W set “STLR0” and “STLT0” bits when a “valid OUT0 token” was processed 0: Disabled **Reset Source: Hardware reset, USB reset, SETUP**
Bit 0	STLCW	0B	R/W	1: Enable H/W set “STLT0” and “STLR0” bits when a “valid IN0 token” was processed 0: Disabled **Reset Source: Hardware reset, USB reset, SETUP**

CRSEQ	STLCR	STLCW	Valid OUT0 Data 0	Valid OUT0 Data 1	Valid IN0 Token	Note
0	0	0	STLT0 = 0 & STLR0 = xx	STLT0 = 0 & STLR0 = xx	STLT0 = xx & STLR0 = 0	
1	0	0	STLT0 = 0 & STLR0 = xx	STLT0 = 0 & STLR0 = xx	STLT0 = xx & STLR0 = 0	
0	1	0	STLT0 = 1 & STLR0 = 1	STLT0 = 1 & STLR0 = 1	STLT0 = xx & STLR0 = 0	
1	1	0	STLT0 = 0 & STLR0 = xx	STLT0 = 1 & STLR0 = 1	STLT0 = xx & STLR0 = 0	
0	0	1	STLT0 = 0 & STLR0 = xx	STLT0 = 0 & STLR0 = xx	STLT0 = 1 & STLR0 = 1	
1	0	1	STLT0 = 0 & TLR0 = xx	STLT0 = 0 & STLR0 = xx	STLT0 = 1 & STLR0 = 1	
0	1	1	STLT0 = 0 & STLR0 = 1	STLT0 = 0 & STLR0 = 1	STLT0 = 1 & STLR0 = 0	Illegal
1	1	1	STLT0 = 0 & STLR0 = xx	STLT0 = 0 & STLR0 = 1	STLT0 = 1 & STLR0 = 0	Illegal

***Note1**: xx means unchanged*

***Note2:** Set the control register in the illegal condition will result in abnormal state under EP0 Control Read/Write Transfer.*

The RX FIFO operational model refers to Figure 10-2.

In the following, the related F/W procedures and H/W actions are described.

*(1) After Hardware Reset or USB Reset, the **R0FULL** bit in **RXFLG0** will reset to 0 to announce no data in **RXDAT0** FIFO.*

(2) SIE receives data (a valid SETUP Transaction or a valid OUT Transaction) byte-by-byte from USB transceiver.

(3) SIE issues ACK.

*(4) A SETUP or OUT IRQ occurs and H/W writes data and bytes count to the **RXDAT0** and **RXCNT0** registers.*

*(5) H/W sets the **R0FULL** bit to "1".*

(6) F/W PUSH IE, clear EA = 0

*(7) After F/W read data from **RXDAT0** FIFO, F/W has to set the **R0FULL** bit to "0".*

(8) F/W POP IE.

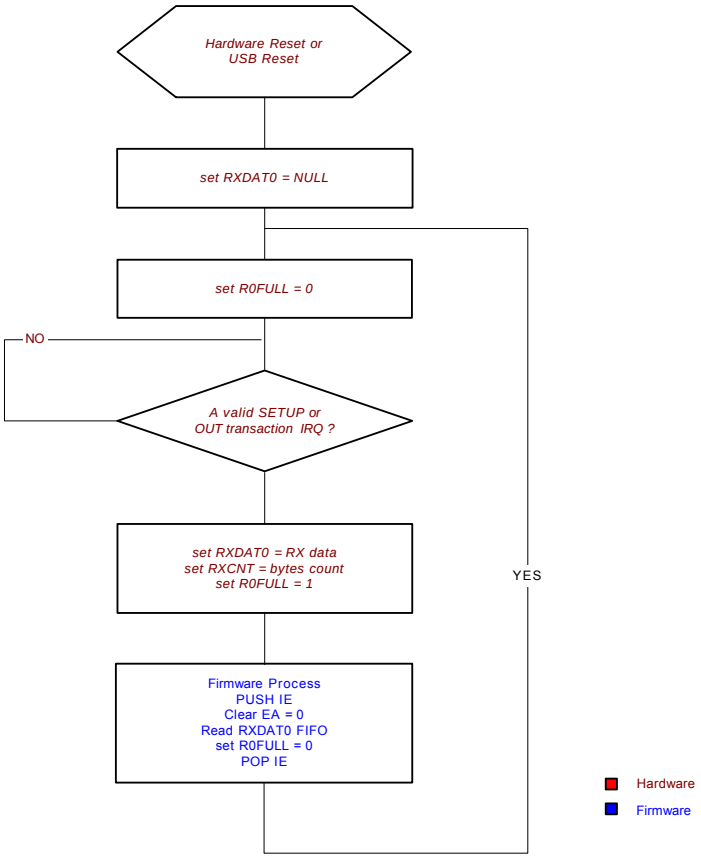


Figure 10-2. RXFIFO Operation Model

11. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input/Output Voltage . . . . . GND - 0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . 0℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

Operating Voltage (V_{DD}) . . . . . +4.4V to 5.5V

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5V, GND = 0V, T_A = 25°C, F_{OSC} = 6MHz, unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Main Power						
Operating Voltage	V_{DD}	4.4	5	5.25	V	
Operating Current 1 (F_{SYS} = 6Mhz)	I_{OP}	-	-	10	mA	No load (F_{OSC} = 6Mhz)
Idle mode Current	I_{IDLE}	-	-	6	mA	No Load (Enable Wake-up timer)
Power down Current	I_{PD}	-	-	200	µA	No Load, In Power-down mode (Disable wake-up timer, LVR Disable)
Regulator (For Customer)						
3.3V Regulator Voltage	V_{33} (V33)	3.0	3.3	3.6	V	V_{DD} = 4.4V - 5.25V, I_O = 35mA (max)
1.8V Regulator Voltage	V_{18}	1.7	1.8	1.9	V	V_{DD} = 4.4V - 5.25V, I_O = 10mA (max)
Regulator (For Designer)						
V33 dropout voltage	V_{DROP33}	-	-	0.1	V	V_{IN} = 5V, I_{OUT33} = 35mA
V18 dropout voltage	V_{DROP18}	-	-	0.05	V	V_{IN} = 5V, I_{OUT33} = 10mA
GPIO and LED Port						
Output High Voltage Port0	V_{OH1}	2.4	-	-	V	Determined by **PHCON0**
Output High Voltage Port1	V_{OH2}	2.4	-	-	V	Determined by **PHCON1**
Output High Voltage Port2	V_{OH3}	2.4	-	-	V	Determined by **PHCON2**
Output High Voltage Port3	V_{OH4}	2.4	-	-	V	Determined by **PHCON3**
Output High Voltage Port4[2:0]	V_{OH5}	2.4	-	-	V	Determined by **PHCON4**
Output High Voltage Port4[6:5] (When **USB_CON** = 0)	V_{OH6}	2.4	-	-	V	I_{OH6} = -0.8mA (min.)
Output Low Voltage Port0	V_{OL1}	-	-	0.4	V	I_{OLI} = 5mA (min.)
Output Low Voltage Port1	V_{OL2}	-	-	0.4	V	I_{OL2} = 5mA (min.)
Output Low Voltage Port2	V_{OL3}	-	-	0.4	V	I_{OL3} = 5mA (min.)
Output Low Voltage Port3[7:6] (When **P3SEL**x = 0)	V_{OL5}	-	-	0.4	V	I_{OL5} = 5mA (min.)
Output Low Voltage Port3[7:6] (When **P3SEL**x = 1)	V_{OL6}	1.0	-	1.2	V	I_{OL6} = 20mA (Typ.) (Blue)
Output Low Voltage Port3[5:0] (When **P3SEL**x = 0)	V_{OL7}	-	-	0.4	V	I_{OL7} = 5mA (min.)
Output Low Voltage Port3[5:0] (When **P3SEL**x = 1)	V_{OL8}	2.6	-	3.2	V	I_{OL8} = 11mA (Typ.) (LED)

Output Low Voltage Port4[2:0] (When **P4SEL**x = 0)	V_{OL9}	2.6	-	3.2	V	I_{OL9} = 11mA (Typ.) (LED)
Output Low Voltage Port4[2:0] (When **P4SEL**x = 1)	V_{OL10}	-	-	0.4	V	I_{OL10} = 5mA (min.)
Output Low Voltage Port4[6:5] (When **USB_CON** = 0)	V_{OL11}	-	-	0.4	V	I_{OL11} = 8mA (min.)
RSTB internal pull-up resistor	R_{RST}	30	55	80	kΩ	@ 0v
Schmitt Trigger Input High Voltage (P02, P03, P15, P16, P45 and P46)	V_{STIH}	2.2	-	-	V	
Schmitt Trigger Input Low Voltage (P02, P03, P15, P16, P45 and P46)	V_{STIL}	-	-	1	V	
Input High Voltage	V_{IH}	2	-	-	V	
Input Low Voltage	V_{IL}	-	-	1	V	
Reset (DC)						
Power-on Reset Level	V_{POR}			3.8	V	
Auxiliary Lower-voltage Reset Level	V_{LVRA}	3.2	3.5	3.8	V	
Low Voltage Reset 1 Level	V_{LVR1}	1.4	1.5	1.6	V	
Upper Threshold Voltage for external Reset	$V_{UT(RESET)}$	2	-	-	V	
Lower Threshold Voltage for external Reset	$V_{LT(RESET)}$	-	-	0.8	V	
V_{OH} against DRV_OUT[1:0] (Note)						
Output High Voltage of Port0 - Port3, Port4:[2:0]	V_{OH_00}	2.4			V	**PHCONx** = 1, **PHCONx** = 0 & **DRV_OUT**[1:0] = 0x00 I_{OH_00} = 50uA (Min.) - 70uA (Typ.) - 100uA (Max.)
Output High Voltage of Port0 - Port3, Port4:[2:0]	V_{OH_01}	1.0			V	**PHCONx** = 0 & **DRV_OUT**[1:0] = 0x01 I_{OH_01} = 8uA (Typ.)
Output High Voltage of Port0 - Port3, Port4:[2:0]	V_{OH_10}	1.0			V	**PHCONx** = 0 & **DRV_OUT**[1:0] = 0x10 I_{OH_10} = 4uA (Typ.)
Output High Voltage of Port0 - Port3, Port4:[2:0]	V_{OH_11}	1.0			V	**PHCONx** = 0 & **DRV_OUT**[1:0] = 0x11 I_{OH_11} = 2uA (Typ.)

Note:
*There are four types of Port0 - Port3, Port4 [2:0] pull high ability. Under this condition, user can select code option **DVR_OUT.** For more information, please refer to **Ordering Information** on Page xx.*

AC Electrical Characteristics (V_{DD} = 5V, GND = 0V, T_A =25°C, F_{OSC}= 6MHz, unless otherwise noted)

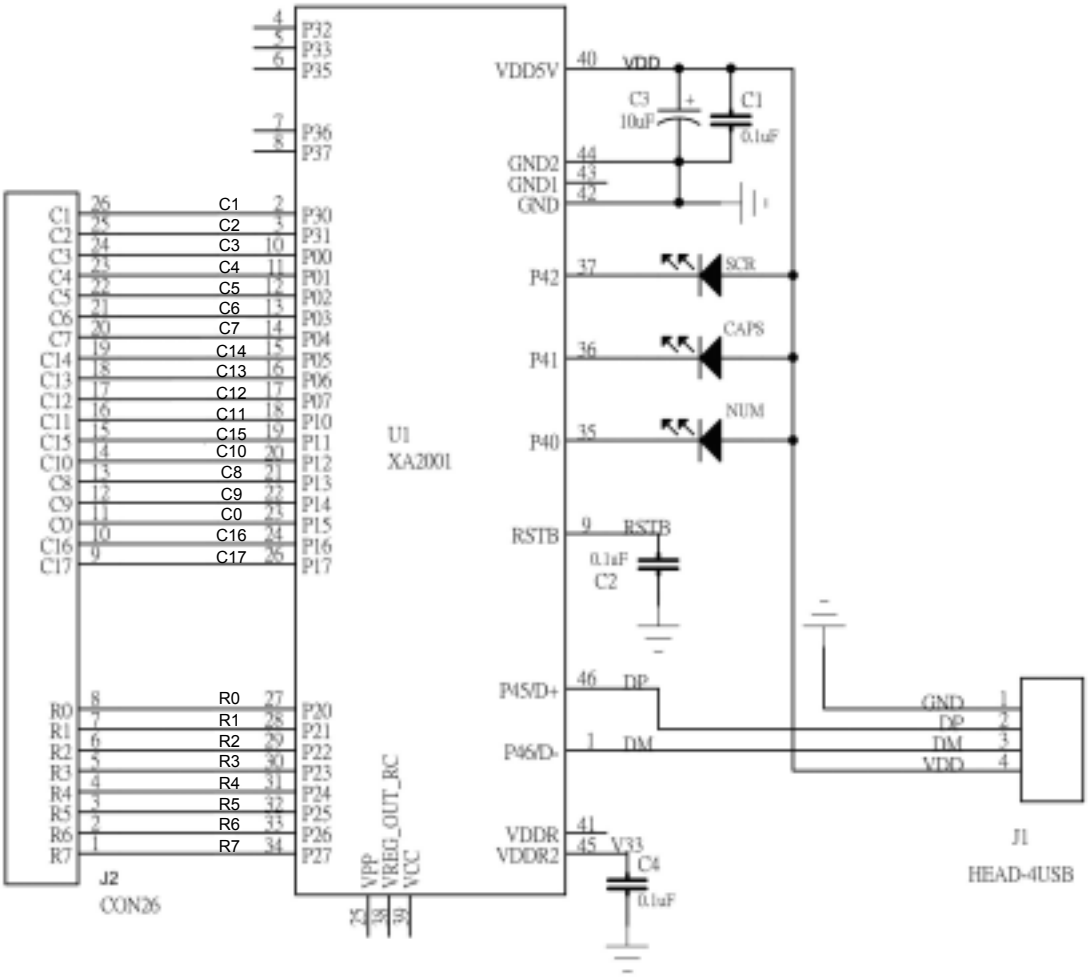
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Oscillator						
Internal RC Frequency 1	F_{SYS}	5.91	6	6.09	MHz	±1.5%
Internal RC Frequency 2	F_{RING}	27.2	32	36.8	KHz	±15%
Reset (AC)						
External Reset Pulse Width	$T_{PW(RSTB)}$	-	2^{13}	-	T_{SYS}	F_{SYS} = 6MHz
External Reset hold time	$T_{RST(RSTB)}$	-	2^{7}	-	T_{SYS}	F_{SYS} = 6MHz
Power On Reset time	$T_{RST(POR)}$	-	12.2	-	ms	F_{SYS} = 6MHz
Low Voltage Reset time	$T_{RST(LVR)}$	-	12.2		ms	F_{SYS} = 6MHz
Drop-Down Width for LVR1	$T_{PW(LVR1)}$	-	2^{9}	-	T_{SYS}	F_{SYS} = 6MHz
Drop-Down Width for LVR2	$T_{PW(LVR2)}$	-	2^{9}	-	T_{SYS}	F_{SYS} = 6MHz
Watch-Dog Reset Hold Time	$T_{RST(WDT)}$	-	500	-	µs	
Internal USB Reset Hold Time	$T_{RST(USB)}$	2	-	4	T_{SYS}	F_{SYS} = 6MHz
SE0 Width for USB Reset	T_{URST}	22	-	-	µs	
SE0 Width for USB Reset (power-down mode)	T_{URST1}	3	-	-	ms	
Internal Resume Reset Width (Global wake-up)	T_{WKRST1}	-	2.7	-	ms	
Internal Resume Reset Width (Remote Wakeup, **RSU_SEL** = 0)(HW Issue K)	T_{WKRST2}	-	18.4	-	ms	
Internal Resume Reset Width (Remote Wakeup, **RSU_SEL** = 1)	T_{WKRST3}	-	5.4	-	ms	
Internal Resume Reset Width (Wake-Up timer)	T_{WKRST4}	2^{10}	-	2^{17}	T_{SYS}	F_{SYS} = 6MHz ,(Depend on Period[1:0])
Noise cancellation for ExT0	$T_{PW(EXT0)}$	-	-	2^{2}	T_{SYS}	F_{SYS} = 6MHz
Noise cancellation for P15/TC0	$T_{PW(SDA)}$	-	-	6	T_{SYS}	F_{SYS} = 6MHz
P46 and P45 slew rate	T_{DAT}	-	2.6	-	µs	500pF load

USB DC/AC Specifications

- Please refer to the UNIVERSAL SERIAL BUS specification Version 1.1 Chapter 7.
- Some items are listed in the following table.
- In addition, the crossover point voltage should meet the following specifications.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Voltage (Driven)	V_{IH} (USB)	2.0	-	-	V	DM, DP
Input High Voltage (Floating)	V_{IHZ} (USB)	2.7	-	3.6	V	DM, DP
Input Low Voltage	V_{IO} (USB)	-	-	0.8	V	DM, DP
Differential Input Sensitivity	V_{DI} (USB)	0.2	-	-	V	DM, DP (|VDP - VDM|)
Differential Common Mode Range	V_{DM} (USB)	0.8	-	2.5	V	DM, DP (Includes V_{DI} Range)
Output Low Voltage	V_{OL} (USB)	0.0	-	0.3	V	DM, DP
Output High Voltage (Drive)	V_{OH} (USB)	2.8	-	3.6	V	DM, DP
Output Crossover Voltage	V_{CRS} (USB)	1.3	-	2.0	V	DP, DM, V_{DD} = 4.4V - 5.25V

Application Circuit (For Reference Only)



Ordering Information

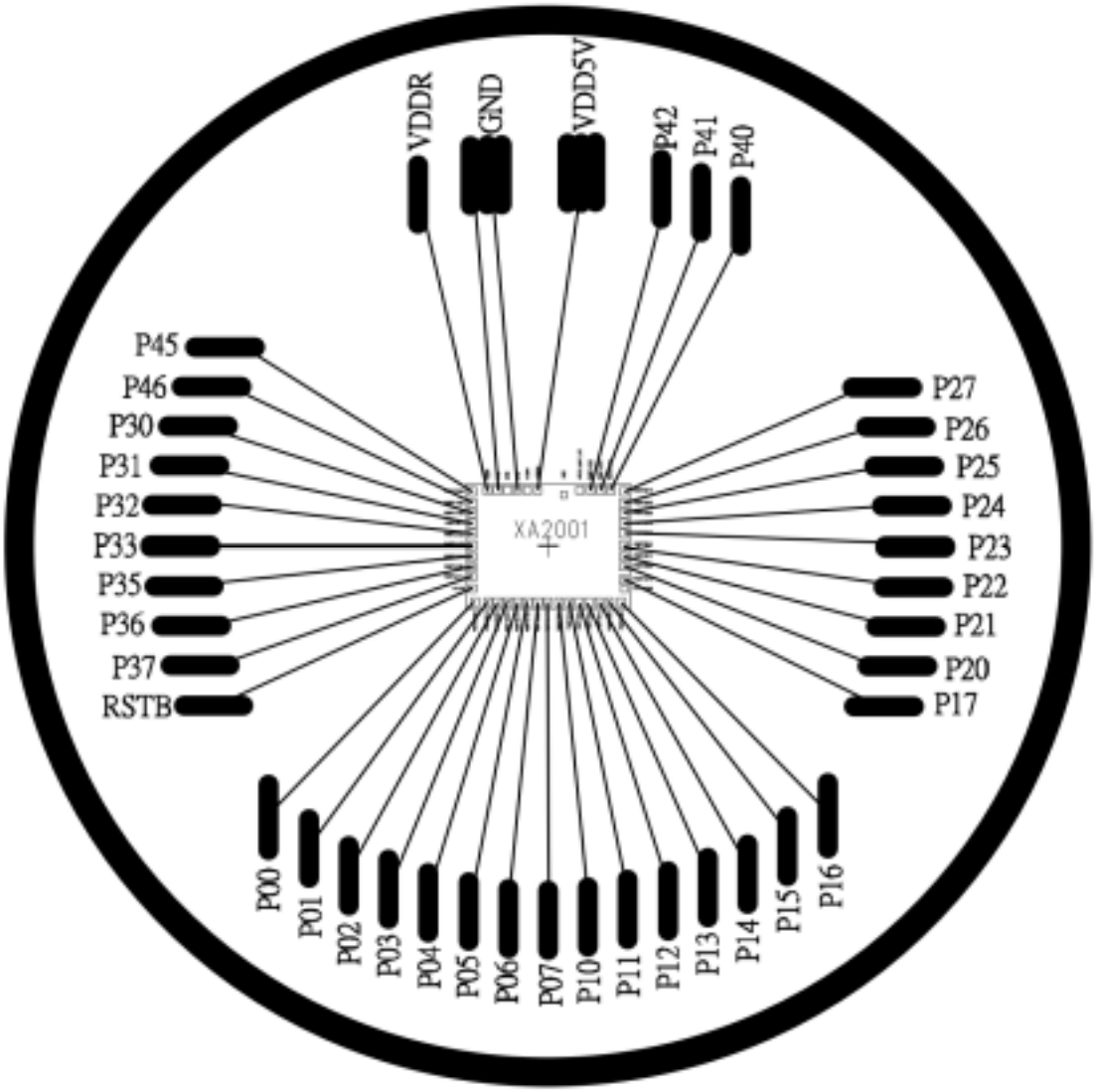
Part No.	Package
XA2001H-YYXXX	Chip Form

Note: Choose YY from HA, HB, HC, HD as follows, XXX is code number.

Code Type No.	Output High Voltage of Port0 - Port3, Port4:[2:0]
HAXXX	V_{OH_00}
HBXXX	V_{OH_01}
HCXXX	V_{OH_10}
HDXXX	V_{OH_11}

Bonding Diagram

Compatible to XA2000 COB bonding



Pad Location unit: μm

Pad NO.	Pad Name	X	Y	COB	Pad NO.	Pad Name	X	Y	COB
1	PORT4[6]	758.83	-423.89	P46	24	PORT1[6]	-733.5	558.13	P16
2	PORT3[0]	758.83	-323.09	P30	25	vpp_pad	-762.88	419.4	NC
3	PORT3[1]	758.83	-222.29	P31	26	PORT1[7]	-758.83	327.15	P17
4	PORT3[2]	758.83	-121.49	P32	27	PORT2[0]	-758.83	194.86	P20
5	PORT3[3]	758.83	-6.58	P33	28	PORT2[1]	-758.83	94.06	P21
6	PORT3[5]	758.83	94.22	P35	29	PORT2[2]	-758.83	-6.74	P22
7	PORT3[6]	758.83	195.02	P36	30	PORT2[3]	-758.83	-121.95	P23
8	PORT3[7]	758.83	295.82	P37	31	PORT2[4]	-758.83	-222.75	P24
9	RSTB	758.83	417.15	RSTB	32	PORT2[5]	-758.83	-323.55	P25
10	PORT0[0]	733.5	558.13	P00	33	PORT2[6]	-758.83	-424.35	P26
11	PORT0[1]	607.5	558.13	P01	34	PORT2[7]	-758.83	-545.85	P27
12	PORT0[2]	506.7	558.13	P02	35	PORT4[0]	-624.89	-558.13	P40
13	PORT0[3]	405.9	558.13	P03	36	PORT4[1]	-524.09	-558.13	P41
14	PORT0[4]	305.1	558.13	P04	37	PORT4[2]	-423.29	-558.13	P42
15	PORT0[5]	204.3	558.13	P05	38	VREG_OUT_RC	-318.89	-558.13	NC
16	PORT0[6]	103.5	558.13	P06	39	VCC	-155.89	-511.65	NC
17	PORT0[7]	2.7	558.13	P07	40	VDD5V	105.3	-558.13	VDD5V
18	PORT1[0]	-108	558.13	P10	41	VDDR	206.1	-558.13	NC
19	PORT1[1]	-208.8	558.13	P11	42	GND:	306.9	-558.13	GND
20	PORT1[2]	-309.6	558.13	P12	43	GND:	407.7	-558.13	NC
21	PORT1[3]	-410.4	558.13	P13	44	GND:	508.5	-558.13	GND
22	PORT1[4]	-511.2	558.13	P14	45	VDDR	609.3	-558.13	VDDR
23	PORT1[5]	-612	558.13	P15	46	PORT4[5]	758.83	-545.39	P45

Data Sheet Revision History

Revision No.	History	Date
1.0	Original	Aug. 2013