

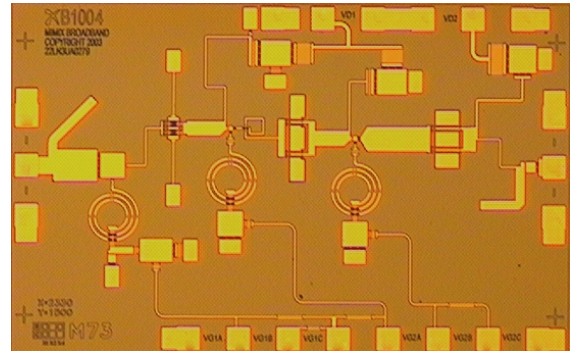
16.0-30.0 GHz GaAs MMIC Buffer Amplifier

April 2005 - Rev 01-Apr-05

Features

- X High Dynamic Range
- X Excellent LO Driver/Buffer Amplifier
- X Low Noise or Power Bias Configurations
- X 21.0 dB Small Signal Gain
- X 2.2 dB Noise Figure at Low Noise Bias
- X +19.0 dBm P1dB Compression Point at Power Bias
- X 100% On-Wafer RF, DC and Noise Figure Testing
- X 100% Visual Inspection to MIL-STD-883 Method 2010

Chip Device Layout



General Description

Mimix Broadband's three stage 16.0-30.0 GHz GaAs MMIC buffer amplifier has a small signal gain of 21.0 dB with a noise figure of 2.2 dB across the band. This MMIC uses Mimix Broadband's 0.15 μm GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Absolute Maximum Ratings

Supply Voltage (Vd)	+6.5 VDC
Supply Current (Id)	200 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (Pin)	+5 dBm
Storage Temperature (Tstg)	-65 to +165 °C
Operating Temperature (Ta)	-55 to MTTF Table ⁵
Channel Temperature (Tch)	MTTF Table ⁵

(5) Channel temperature affects a device's MTBF. It is recommended to keep channel temperature as low as possible for maximum life.

Electrical Characteristics (Ambient Temperature T = 25 °C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	16.0	-	30.0
Input Return Loss (S11) ³	dB	6.0	14.0	-
Output Return Loss (S22) ³	dB	10.0	14.0	-
Small Signal Gain (S21) ³	dB	18.0	21.0	24.0
Gain Flatness ($\Delta S21$)	dB	-	+/-1.0	-
Reverse Isolation (S12) ³	dB	40.0	50.0	-
Noise Figure (NF) ⁴	dB	-	2.2	3.0
Output Power for 1 dB Compression (P1dB) ^{1,2,3}	dBm	-	+19.0	-
Output Third Order Intercept Point (OIP3) ^{1,2,3}	dBm	-	+29.0	-
Saturated Output Power (Psat) ^{1,2,3}	dBm	-	+22.0	-
Drain Bias Voltage (Vd1,2)	VDC	-	+4.0	+6.0
Gate Bias Voltage (Vg1c,2c)	VDC	-1.2	-0.3	+0.1
Supply Current (Id) (Vd=4.0V, Vg=-0.3V Typical)	mA	-	90	180

(1) Optional low noise bias Vd1,2=4.0V, Id=90mA will typically yield 3-4dB decreased P1dB and OIP3.

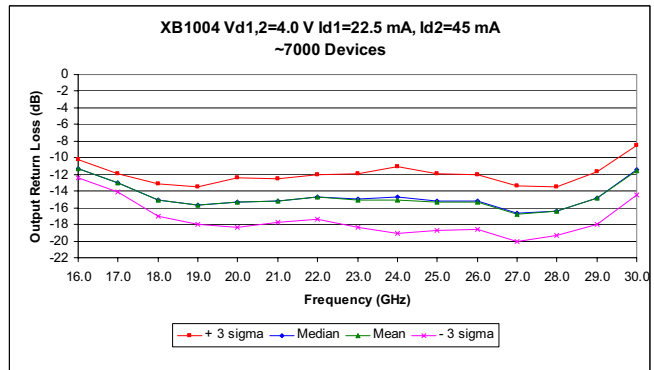
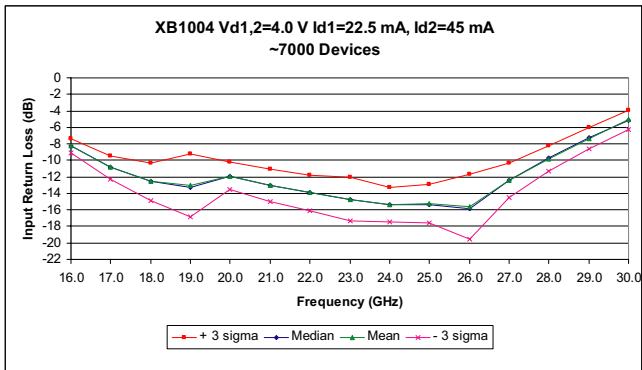
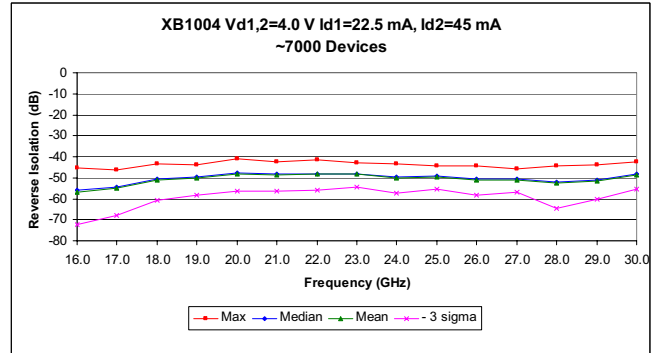
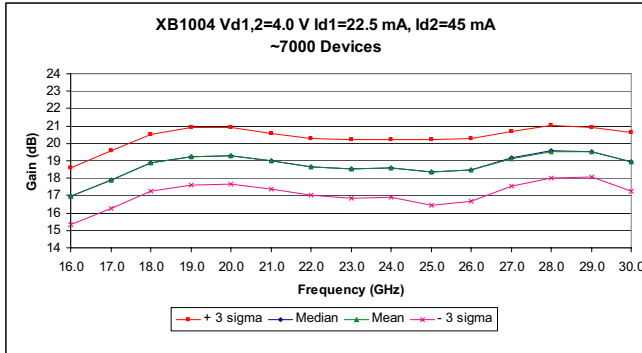
(2) Measured using constant current.

(3) Unless otherwise indicated Min/Max over 17.0-28.0 GHz and biased at Vd=6.0V, Id1=90mA, Id2=90mA.

(4) Unless otherwise indicated Min/Max over 17.0-28.0 GHz and biased at Vd=4.0V, Id1=45mA, Id2=45mA.

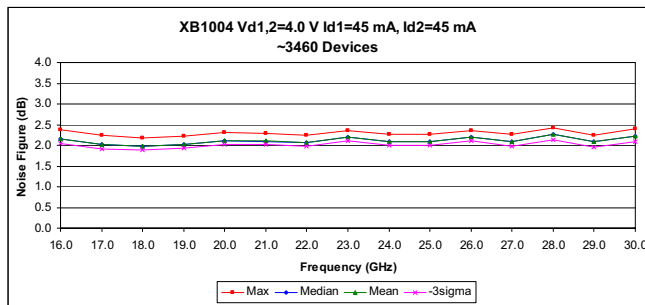
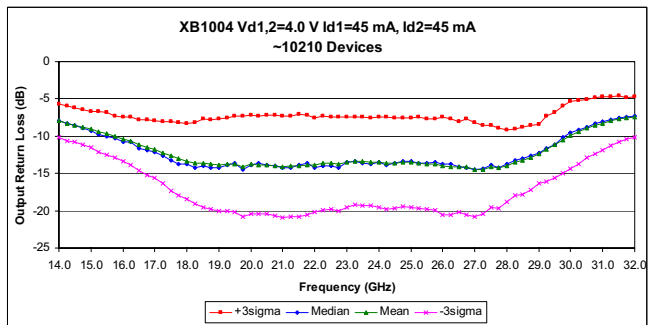
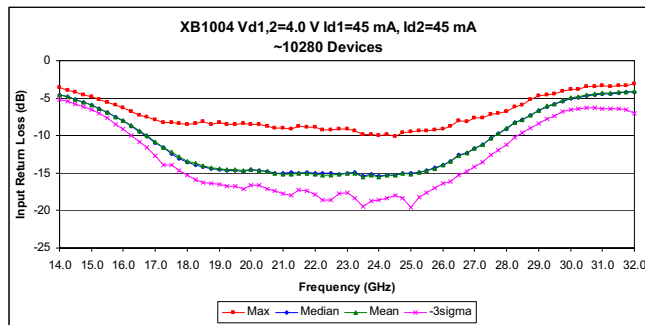
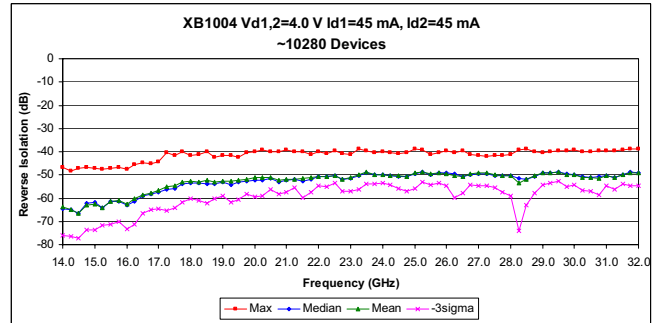
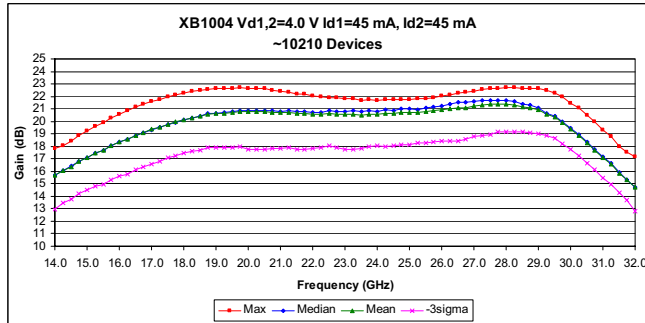
16.0-30.0 GHz GaAs MMIC Buffer Amplifier

Buffer Amplifier Measurements



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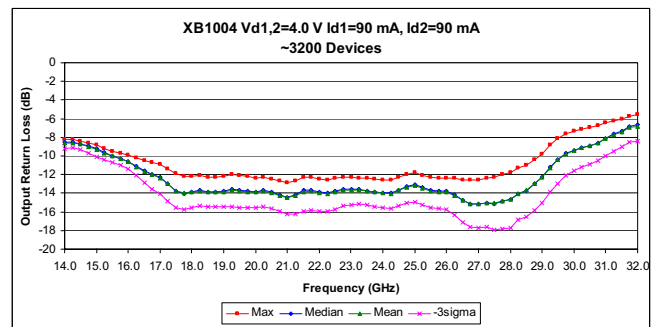
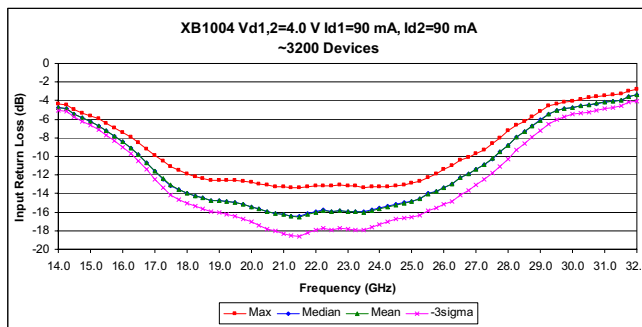
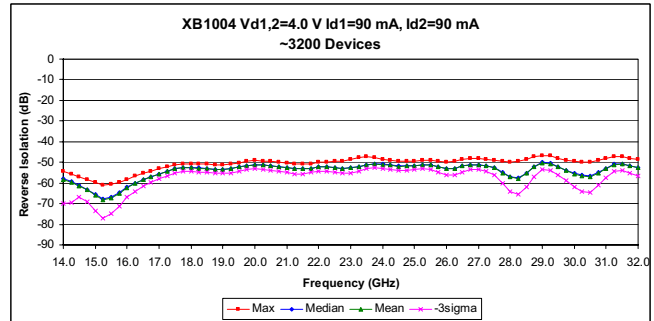
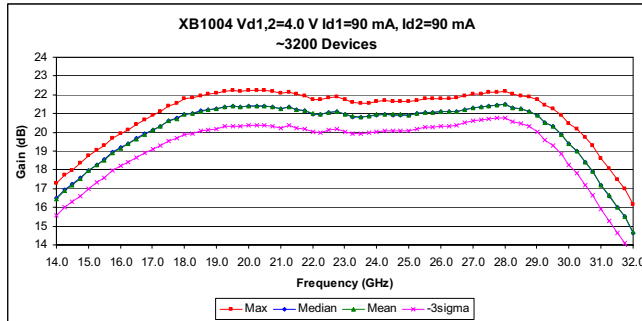
Buffer Amplifier Measurements (cont.)



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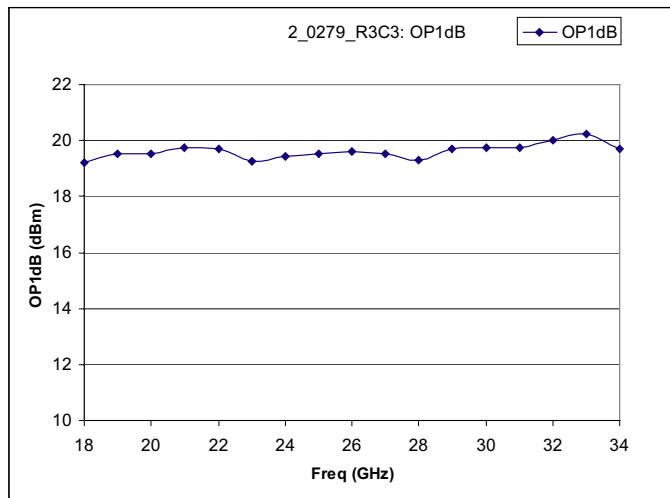
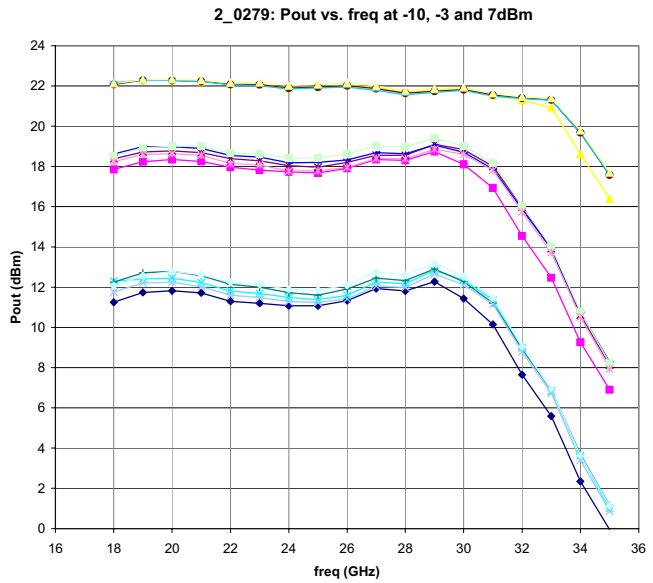
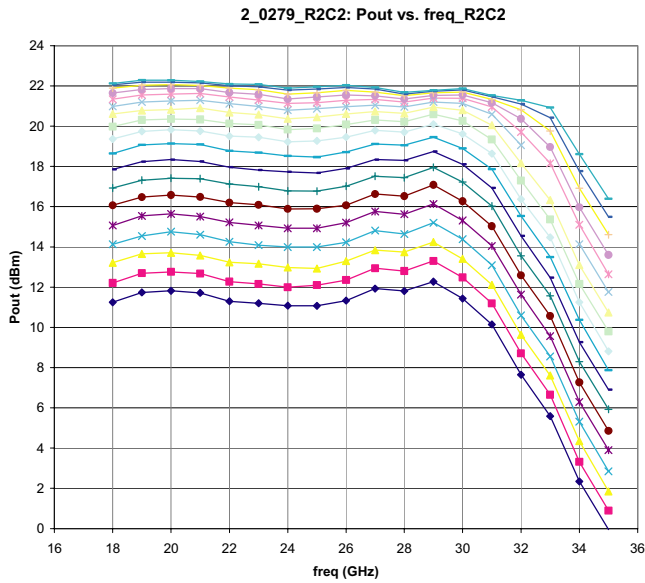
April 2005 - Rev 01-Apr-05

Buffer Amplifier Measurements (cont.)



16.0-30.0 GHz GaAs MMIC Buffer Amplifier

Buffer Amplifier Measurements at Power Bias

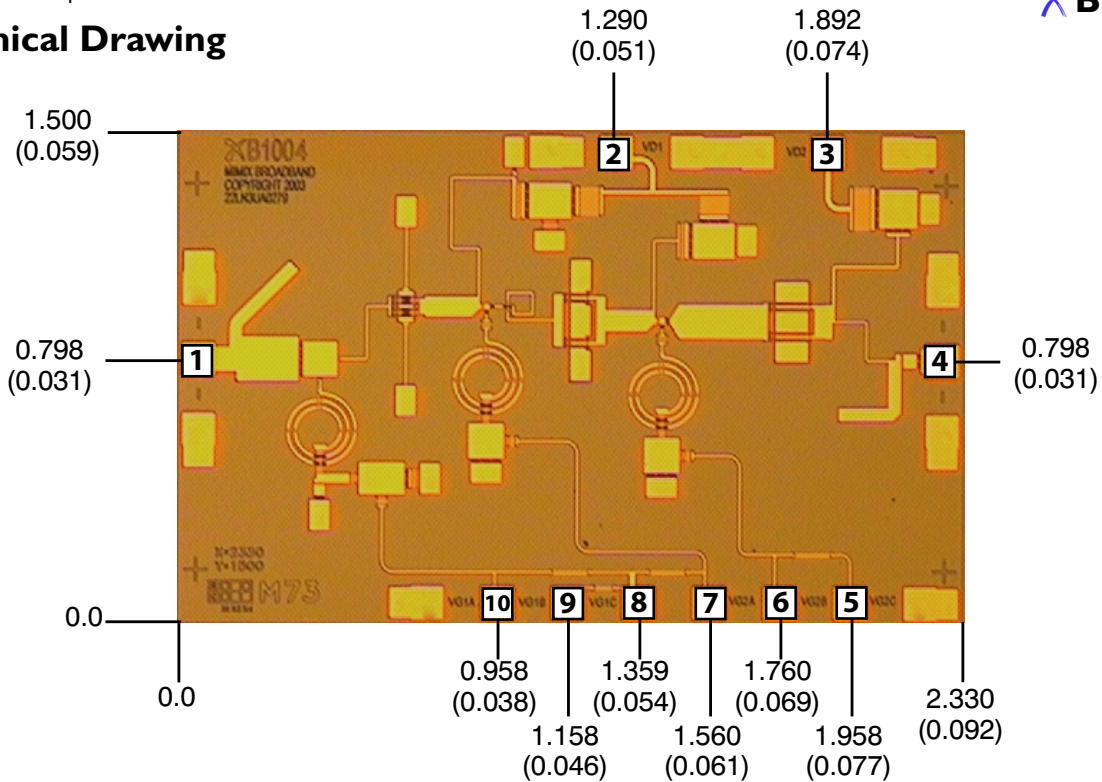


16.0-30.0 GHz GaAs MMIC Buffer Amplifier

April 2005 - Rev 01-Apr-05

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Mechanical Drawing

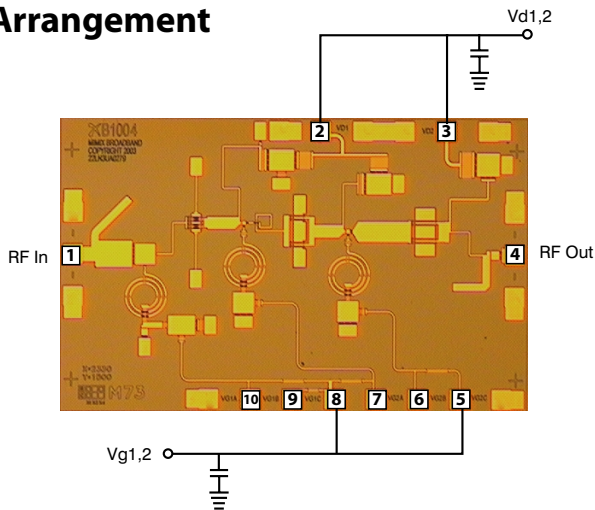


(Note: Engineering designator is 22LN3UA0279)

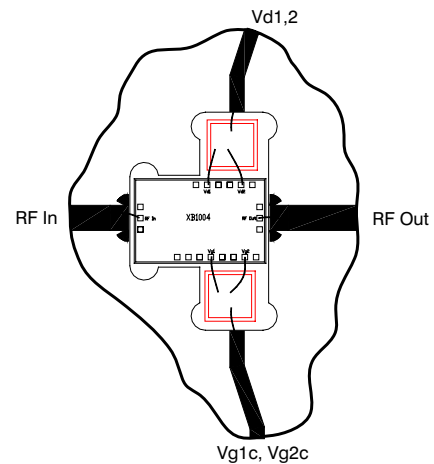
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
 Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
 All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).
 Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
 Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 2.165 mg.

Bond Pad #1 (RF In)	Bond Pad #3 (Vd2)	Bond Pad #5 (Vg2c)	Bond Pad #7 (Vg2a)	Bond Pad #9 (Vg1b)
Bond Pad #2 (Vd1)	Bond Pad #4 (RF Out)	Bond Pad #6 (Vg2b)	Bond Pad #8 (Vg1c)	Bond Pad #10 (Vg1a)

Bias Arrangement



Bypass Capacitors - See App Note [2]



16.0-30.0 GHz GaAs MMIC Buffer Amplifier

April 2005 - Rev 01-Apr-05

App Note [1] Biasing - As shown in the bonding diagram, this device can be operated with all three stages in parallel, and can be biased for low noise performance or high power performance. Low noise bias is nominally $V_d=4V, I_d=90mA$. More controlled performance will be obtained by separately biasing V_{d1} and V_{d2} each at $4.0V, 45mA$. Power bias may be as high as $V_d=6.0V, I_d=180mA$ with all stages in parallel, or most controlled performance will be obtained by separately biasing V_{d1} and V_{d2} each at $6.0V, 90mA$. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is $-0.3V$. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -

For Parallel Stage Bias (Recommended for general applications) -- The same as Individual Stage Bias but all the drain or gate pad DC bypass capacitors ($\sim 100-200$ pf) can be combined. The suggested configuration is to connect $V_{d1,2}$ and $V_{g1c,2c}$. Additional DC bypass capacitance (~ 0.01 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads.

For Individual Stage Bias (Low Input Drive applications only) -- Each DC pad ($V_{d1,2}$ and $V_{g1a,2a,2b}$) needs to have DC bypass capacitance ($\sim 100-200$ pf) as close to the device as possible. Additional DC bypass capacitance (~ 0.01 uF) is also recommended.

For Individual Stage Bias (High Input Drive applications only) -- Each DC pad ($V_{d1,2}$ and $V_{g1c,2c}$) needs to have DC bypass capacitance ($\sim 100-200$ pf) as close to the device as possible. Additional DC bypass capacitance (~ 0.01 uF) is also recommended.

MTTF Tables

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	83.4 deg Celsius	78.8° C/W	5.36E+10	1.87E-02
75 deg Celsius	105.5 deg Celsius	84.7° C/W	3.52E+09	2.84E-01
95 deg Celsius	127.4 deg Celsius	90.0° C/W	3.20E+08	3.13E+00

Bias Conditions: $V_{d1}=V_{d2}=4.0V, I_{d1}=45$ mA, $I_{d2}=45$ mA

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	108.3 deg Celsius	76.1° C/W	2.56E+09	3.91E-01
75 deg Celsius	132.1 deg Celsius	81.5° C/W	1.99E+08	5.04E+00
95 deg Celsius	155.5 deg Celsius	86.4° C/W	2.12E+07	4.72E+01

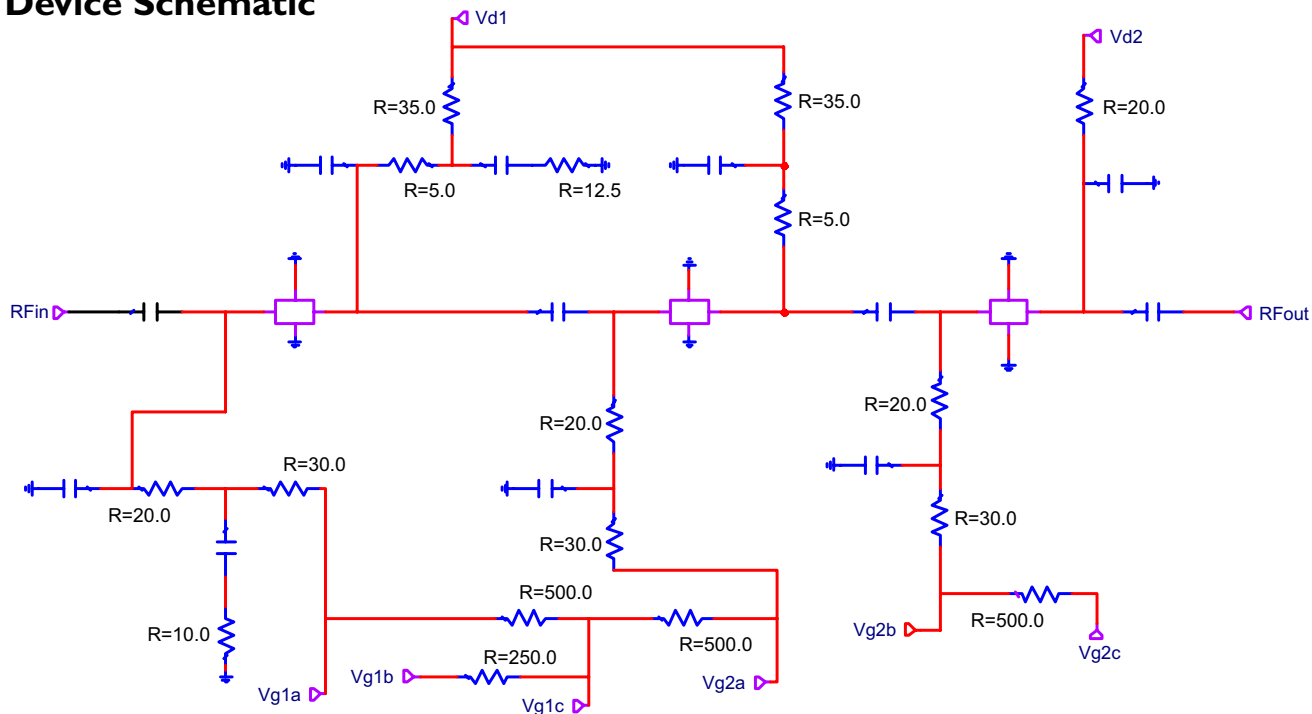
Bias Conditions: $V_{d1}=V_{d2}=5.0V, I_{d1}=70$ mA, $I_{d2}=70$ mA

Backplate Temperature	Channel Temperature	Rth	MTTF Hours	FITs
55 deg Celsius	138.1 deg Celsius	77.0° C/W	1.08E+08	9.22E+00
75 deg Celsius	163.7 deg Celsius	82.1° C/W	1.02E+07	9.82E+01
95 deg Celsius	188.8 deg Celsius	86.8° C/W	1.29E+06	7.73E+02

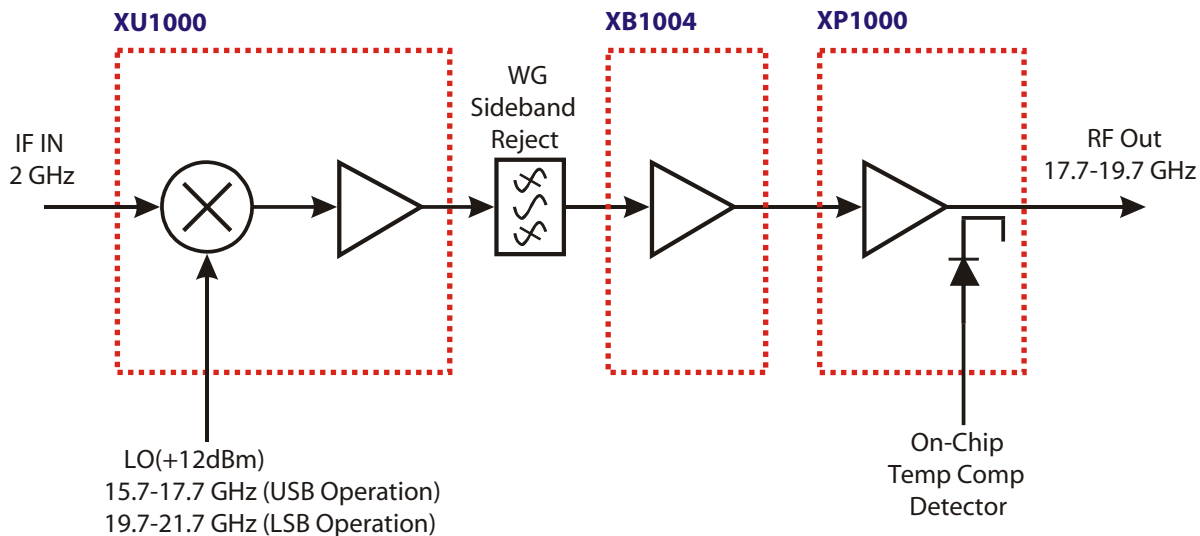
Bias Conditions: $V_{d1}=V_{d2}=6.0V, I_{d1}=90$ mA, $I_{d2}=90$ mA

16.0-30.0 GHz GaAs MMIC Buffer Amplifier

Device Schematic



Typical Application



Mimix Broadband MMIC-based 17.0-27.0 GHz Transmitter Block Diagram

(Changing LO and IF frequencies as required allows design to operate as high as 27 GHz)

16.0-30.0 GHz GaAs MMIC Buffer Amplifier

April 2005 - Rev 01-Apr-05

Handling and Assembly Information

CAUTION! - Mimix Broadband MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- *Do not ingest.*
- *Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.*
- *Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.*

Life Support Policy - Mimix Broadband's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of Mimix Broadband. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from Mimix Broadband are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001² thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium should be avoided). The work station temperature should be 310°C ± 10°C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.