# XB1008-QT

## Buffer Amplifier
## 10 - 21 GHz

Rev. V2

### Features

- Excellent Transmit LO/Output Buffer Stage
- 17 dB Small Signal Gain
- 20 dBm Psat
- 32 dBm Output IP3
- 4.5 dB Noise Figure
- Variable Gain with Adjustable Bias
- 100% RF, DC and Output Power Testing
- Lead-Free 3 mm 16-Lead QFN Package
- RoHS* Compliant

### Description

The XB1008-QT is a two stage 10 - 21 GHz GaAs MMIC buffer amplifier that has a small signal gain of 17 dB with a 18 dBm P1dB output compression point. The device also provides variable gain regulation with adjustable bias.

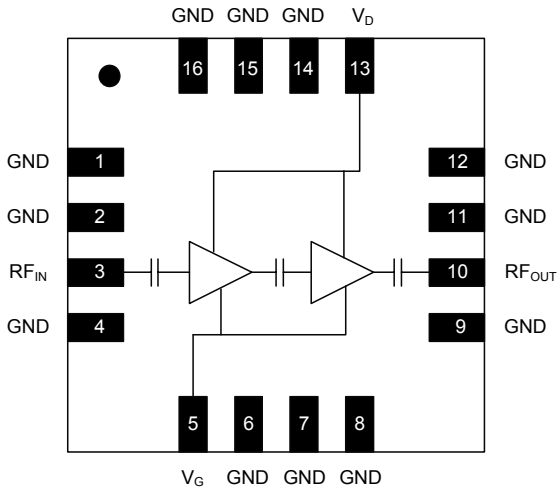
The device is ideally suited as an LO or RF buffer stage with broadband performance at a very low cost. The device comes in an RoHS compliant 3 mm QFN surface mount package offering excellent RF and thermal properties. This device is specifically designed for use in PtP radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

### Ordering Information[1]

| Part Number | Package |
|---|---|
| XB1008-QT-0G0T | tape and reel |
| XB1008-QT-EV1 | evaluation module |

1. Reference Application Note M513 for reel size information.

### Functional Block Diagram




### Pin Configuration

| Pin No. | Function |
|---|---|
| 1-2, 4, 6-9, 11, 12, 14-16 | Ground |
| 3 | RF Input |
| 5 | Gate Bias |
| 10 | RF Output |
| 13 | Drain Bias |
| Paddle[2] | Ground |

2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

## Electrical Specifications: 10 - 21 GHz, $T_A$ = +25°C

| Parameter | Units | Min. | Typ. | Max. |
|---|---|---|---|---|
| Input Return Loss (S11) | dB | — | 12 | — |
| Output Return Loss (S22) | dB | — | 12 | — |
| Small Signal Gain (S21) | dB | — | 17 | — |
| Gain Flatness (ΔS21) | dB | — | +/-2 | — |
| Reverse isolation (S12) | dB | — | 65 | — |
| Noise Figure | dB | — | 4.5 | — |
| Output Power for 1dB Compression Point (P1dB) | dBm | — | 18 | — |
| Saturated Output Power ($P_{SAT}$) | dBm | — | 20 | — |
| Output Third Order Intercept | dBm | — | 32 | — |
| Drain Bias Voltage ($V_D$) | VDC | — | 4 | 4 |
| Gate Bias Voltage ($V_G$) | VDC | -1.0 | -0.23 | -0.1 |
| Supply Current ($I_D$) ($V_D$ = +4.0 V, $V_G$2 = -0.5 V Typical) | mA | — | 100 | 130 |

## Absolute Maximum Ratings[3]

| Parameter | Absolute Maximum |
|---|---|
| Supply Voltage | 4.3 VDC |
| Supply Current | 180 mA |
| Gate Bias Voltage | 0 V |
| Input Power | 20 dBm |
| Storage Temperature | -65°C to +165°C |
| Operating Temperature | -55°C to +85°C |
| Channel Temperature | 150°C |

3. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

## Handling Procedures

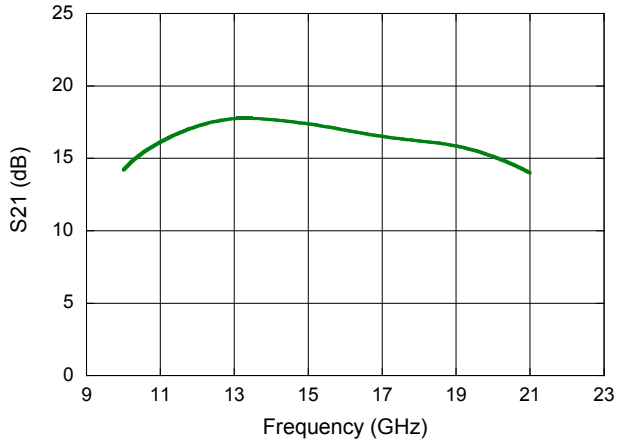
Please observe the following precautions to avoid damage:

## Static Sensitivity

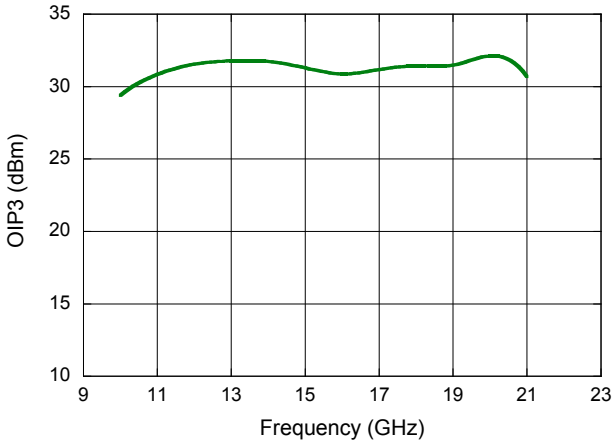
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices, MM Class A devices.

## Typical Performance Curves

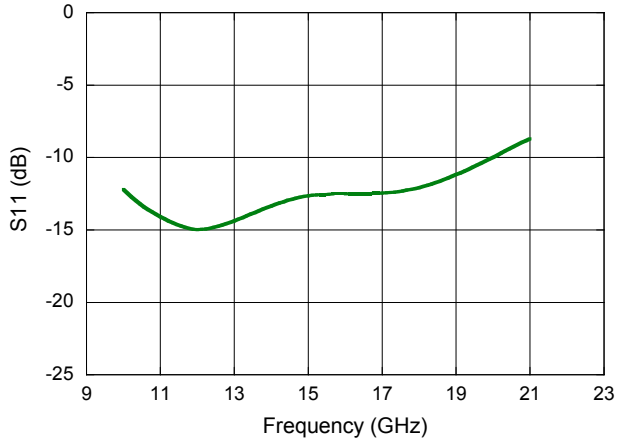
***Small Signal Gain, $V_D$ = 4 V, 100 mA***



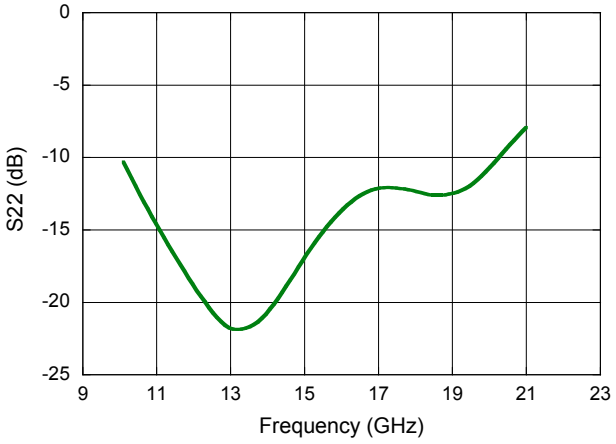

***OIP3, $V_D$ = 4 V, 90 mA, $P_{IN}$ = 15 dBm***



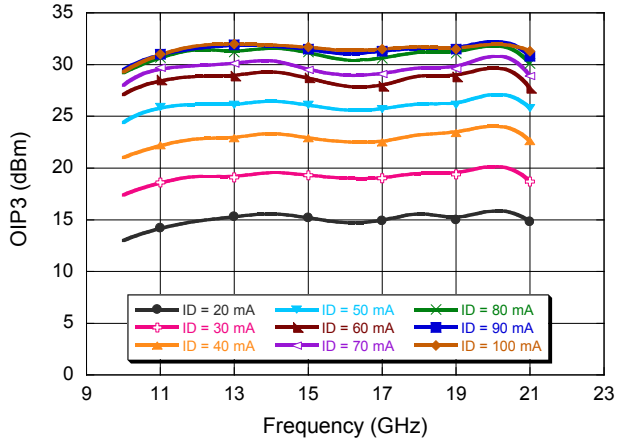

***Input Return Loss, $V_D$ = 4 V, 100 mA***




***Output Return Loss, $V_D$ = 4 V, 100 mA***

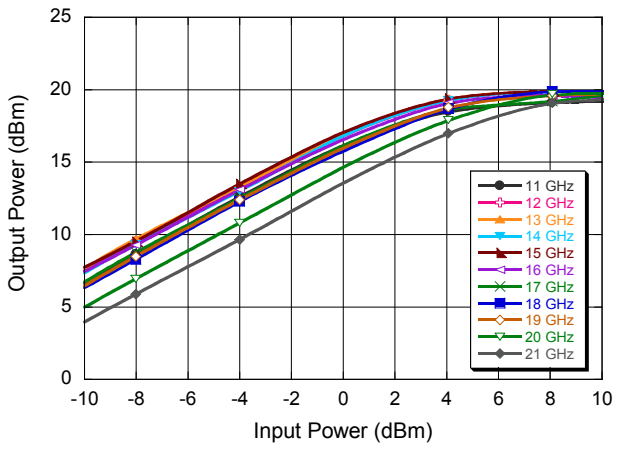



***OIP3, $V_D$ = 4 V, 20 - 100 mA, $P_{IN}$ = -15 dBm***

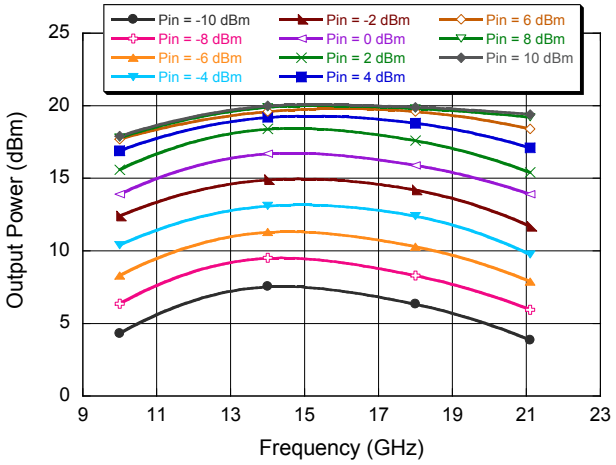


## Typical Performance Curves (cont.)

***Output Power vs. Input Power, $V_D$ = 4 V, 100 mA***



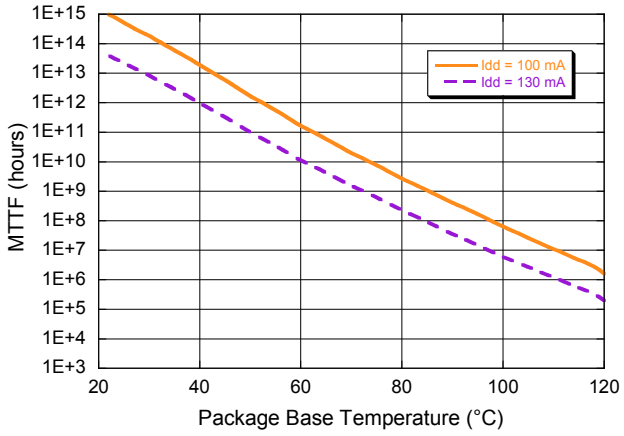

***Output Power vs. Frequency, $V_D$ = 4 V, 100 mA***



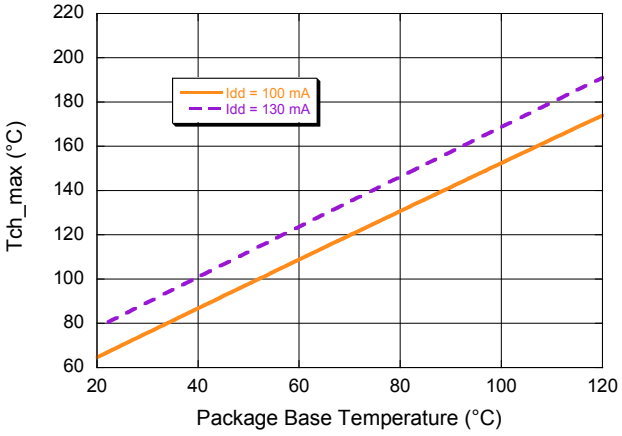

## MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.

***MTTF Hours vs. Package Base Temperature, $V_{DD}$ = 4 V***



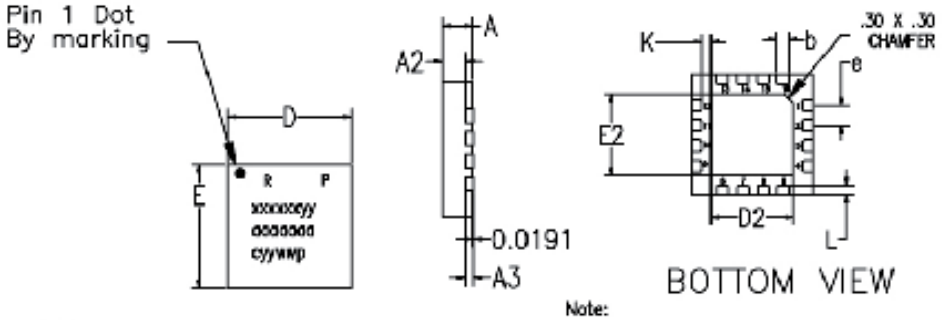

***Tch (max.) vs. Package Base Temperature, $V_{DD}$ = 4 V***



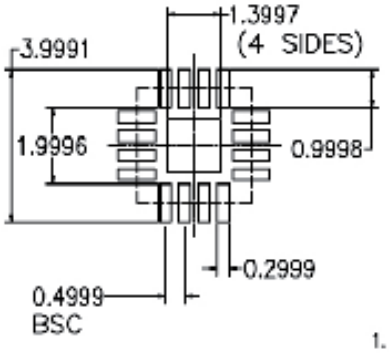
**App Note [1] Biasing -** The device provides variable gain with adjustable bias regulation. For optimum linearity performance, it is recommended to bias this device at $V_D$ = 4 V with $I_D$ = 90 mA. It is also recommended to use active biasing to control the drain currents because this gives the most reproducible results over temperature or RF level variations. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.5 V. Typically the gate is protected with silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

## Lead-Free Package Dimensions/Layout†

**QT** (3x3 mm)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




| | MIN | TYP | MAX |
|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 |
| A3 | | 0.20 REF | |
| A2 | 0.00 | 0.65 | 1.00 |
| b | 0.20 | 0.25 | 0.30 |
| K | 0.20 | – | – |
| D | | 3.00 BSC | |
| E | | 3.00 BSC | |
| e | | 0.50 | |
| D2 | 1.50 | 1.65 | 1.80 |
| E2 | 1.50 | 1.65 | 1.80 |
| L | 0.16 | 0.26 | 0.36 |

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.