XC9254R Series

ETR0529-003

600mA Driver Tr. Built-In, Synchronous Step-Down DC/DC Converter

☆GreenOperation Compatible

■GENERAL DESCRIPTION

The XC9254R series is a group of synchronous-rectification type DC/DC converters with a built-in 0.42Ω P-channel MOS driver transistor and 0.52Ω N-channel MOS switching transistor, designed to allow the use of ceramic capacitors. Operating voltage range is from 2.0V to 6.0V. The XC9254R001 type has a fixed output voltage of 1.2V (accuracy: ±2.0%). The device provides a high efficiency, stable power supply with an output current of 600mA to be configured using only a coil and two capacitors connected externally. With the built-in oscillator, 1.2MHz is fixed internally. As for operation mode, the XC9254R series is automatic PWM/PFM switching control allowing fast response, low ripple and high efficiency over the full range of loads (from light load to heavy load).

The soft start and current control functions are internally optimized. During stand-by, all circuits are shutdown to reduce current consumption to as low as 1.0μA or less. With the built-in UVLO (Under Voltage Lock Out) function, the internal P-channel MOS driver transistor is forced OFF when input voltage becomes 1.4V or lower.

Two types of package SOT-25 and USP-6C are available.

■APPLICATIONS

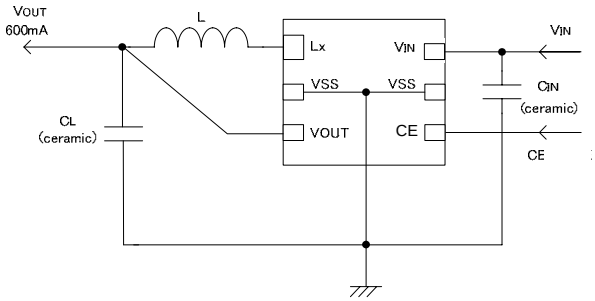
- ●Smart phones / Mobile phones
- ●Bluetooth
- ●Mobile devices / terminals
- ●Portable game consoles
- ●Digital still cameras / Camcorders
- ●Digital audio equipments
- ●Note PCs / Tablet PCs

■FEATURES

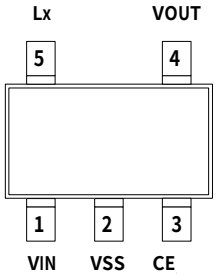
Driver Transistor Built-In	: 0.42Ω P-ch driver transistor 0.52Ω N-ch switch transistor
Input Voltage	: 2.0V ~ 6.0V
Output Voltage	: 1.2V
High Efficiency	: 92% (TYP.)
Output Current	: 600mA
Oscillation Frequency	: 1.2MHz (±15%)
Maximum Duty Cycle	: 100%
Control Methods	: PWM/PFM Auto
Function	: Current Limiter Circuit Built-In (Constant Current & Latching) C_L Discharge
Capacitor	: Low ESR Ceramic Capacitor
Operating Ambient Temperature	: -40℃ ～ +85℃
Packages	: SOT-25, USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

* Performance depends on external components and wiring on the PCB.

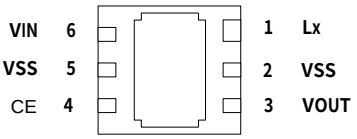
■TYPICAL APPLICATION CIRCUIT



■PIN CONFIGURATION



SOT-25
(Top View)



USP-6C
(BOTTOM VIEW)

* Please short the V_{SS} pin (No. 2 and 5).
* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the V_{SS} (No. 5) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
1	6	V_{IN}	Power Input
2	2, 5	V_{SS}	Ground
3	4	CE	High Active Enable
4	3	V_{OUT}	Fixed Output Voltage Pin
5	1	Lx	Switching Output

■PRODUCT CLASSIFICATION

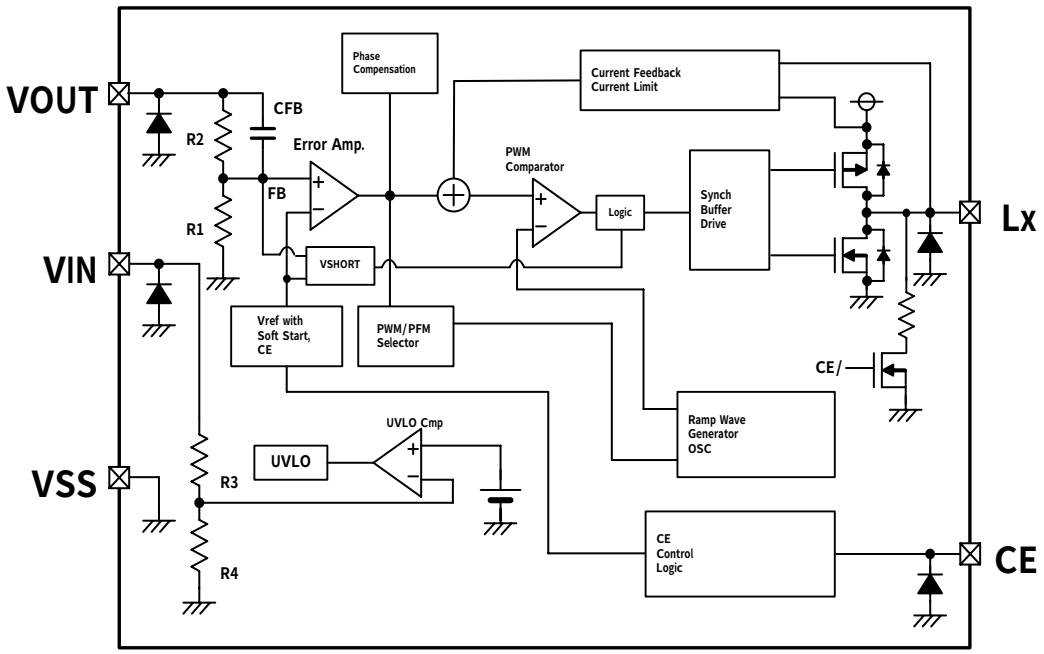
●Ordering Information

PWM / PFM automatic switching control

PRODUCT NAME	PACKAGE (ORDER UNIT)
XC9254R001MR-G (*1)	SOT-25 (3,000/Reel)
XC9254R001ER-G (*1)	USP-6C (3,000/Reel)

(*1) The “-G” suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

■BLOCK DIAGRAM



NOTE:
The signal from CE Control Logic to PWM/PFM Selector is being fixed to "H" level inside, and XC9254R series chooses only PWM/PFM automatic switching control.
Diodes inside the circuit are ESD protection diodes and parasitic diodes.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNIT
V_{IN} Pin Voltage		V_{IN}	- 0.3 ~ 6.5	V
Lx Pin Voltage		V_{Lx}	- 0.3 ~ V_{IN} + 0.3 ≦ 6.5V	V
V_{OUT} Pin Voltage		V_{OUT}	- 0.3 ~ 6.5	V
CE Pin Voltage		V_{CE}	- 0.3 ~ 6.5	V
Lx Pin Current		I_{Lx}	±1500	mA
Power Dissipation (*Ta=25℃)	SOT-25	Pd	250	mW
	USP-6C		100	
Operating Ambient Temperature		Topr	- 40 ~ + 85	°C
Storage Temperature		Tstg	- 55 ~ + 125	°C

■ELECTRICAL CHARACTERISTICS (Continued)

XC9254R Series, V_{OUT}=1.2V, f_{OSC}=1.2MHz, Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Output Voltage	V_{OUT}	When connected to external components, V_{IN}=V_{CE}=5.0V, I_{OUT}=30mA	1.176	1.200	1.224	V	①
Operating Voltage Range	V_{IN}		2.0	-	6.0	V	①
Maximum Output Current	I_{OUTMAX}	V_{IN}=$V_{OUT(E)}$+2.0V, V_{CE}=1.0V, When connected to external components (*8)	600	-	-	mA	①
UVLO Voltage	V_{UVLO}	V_{CE} =V_{IN}, V_{OUT}=$V_{OUT(E)}$×0.5V (*11) Voltage which Lx pin holding "L" level (*1, *10)	1.00	1.40	1.78	V	②
Supply Current	I_{DD}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(E)}$×1.1V	-	15	33	μA	③
Stand-by Current	I_{STB}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}=$V_{OUT(E)}$×1.1V	-	0	1.0	μA	③
Oscillation Frequency	f_{OSC}	When connected to external components, V_{IN}=$V_{OUT(E)}$+2.0V, V_{CE} =1.0V, I_{OUT}=100mA	1020	1200	1380	kHz	①
PFM Switching Current	I_{PFM}	When connected to external components, V_{IN}=$V_{OUT(E)}$+2.0V, V_{CE} =V_{IN}, I_{OUT}=1mA	140	180	240	mA	①
PFM Duty Limit	DTY_{LIMIT_PFM}	V_{CE}=V_{IN}=2.0V, I_{OUT}=1mA		200		%	①
Maximum Duty Cycle	DTY_{MAX}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(E)}$×0.9V	100	-	-	%	②
Minimum Duty Cycle	DTY_{MIN}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(E)}$×1.1V	-	-	0	%	②
Efficiency (*2)	EFFI	When connected to external components, V_{CE}=V_{IN}=$V_{OUT(E)}$+1.2V, I_{OUT}=100mA	-	92	-	%	①
Lx SW "H" ON Resistance 1	R_{LxH}	V_{IN}=V_{CE}=5.0V, $V_{OUT(E)}$×0.9V , I_{Lx}=100mA (*3)	-	0.35	0.55	Ω	④
Lx SW "H" ON Resistance 2	R_{LxH}	V_{IN}=V_{CE}=3.6V, $V_{OUT(E)}$×0.9V , I_{Lx}=100mA (*3)	-	0.42	0.67	Ω	④
Lx SW "L" ON Resistance 1	R_{LxL}	V_{IN}=V_{CE}=5.0V (*4)	-	0.45	0.66	Ω	④
Lx SW "L" ON Resistance 2	R_{LxL}	V_{IN}=V_{CE}=3.6V (*4)	-	0.52	0.77	Ω	-
Lx SW "H" Leak Current (*5)	I_{LeakH}	V_{IN}=V_{OUT}=5.0V, V_{CE}=0V, Lx=0V	-	0.01	1.0	μA	⑤
Current Limit (*9)	I_{LIM}	V_{IN}=V_{CE}=5.0V, V_{OUT}=$V_{OUT(E)}$×0.9V (*7)	900	1050	1350	mA	⑥
Output Voltage Temperature Characteristics	$\triangle V_{OUT}$/ (V_{OUT} • $\triangle$Topr)	I_{OUT}=30mA, -40℃≦Topr≦85℃	-	±100	-	ppm/℃	①
CE "H" Voltage	V_{CEH}	V_{OUT}= $V_{OUT(E)}$×0.9V, Applied voltage to V_{CE}, Voltage changes Lx to "H" level (*10)	0.65	-	6.0	V	③
CE "L" Voltage	V_{CEL}	V_{OUT}= $V_{OUT(E)}$×0.9V, Applied voltage to V_{CE} , Voltage changes Lx to "L" level (*10)	V_{SS}	-	0.25	V	③
CE "H" Current	I_{CEH}	V_{IN}=V_{CE}=5.0V, V_{OUT}= $V_{OUT(E)}$×0.9V	- 0.1	-	0.1	μA	⑤
CE "L" Current	I_{CEL}	V_{IN}=5.0V, V_{CE}=0V, V_{OUT}= $V_{OUT(E)}$×0.9V	- 0.1	-	0.1	μA	⑤
Soft Start Time	t_{SS}	When connected to external components, V_{CE}=0V → V_{IN}, I_{OUT}=1mA	0.5	1.0	2.5	ms	①
Latch Time	t_{LAT}	V_{IN}=V_{CE}=5.0V, V_{OUT}=0.8×$V_{OUT(E)}$, Short Lx at 1Ω resistance (*6)	1.0	-	20.0	ms	⑦
Short Protection Threshold Voltage	V_{SHORT}	Sweeping V_{OUT}, V_{IN}=V_{CE}=5.0V, Short Lx at 1Ω resistance, V_{OUT} voltage which Lx becomes "L" level within 1ms	0.675	0.900	1.150	V	⑦
C_L Discharge	R_{DCHG}	V_{IN}=5.0V, L_X=5.0V, V_{CE}=0V, V_{OUT}=open	200	300	450	Ω	⑧

Test conditions: Unless otherwise stated, V_{IN}=5.0V, $V_{OUT(E)}$=Nominal Voltage, applied voltage sequence is V_{OUT}→V_{IN}→V_{CE}

NOTE:

*1: Including hysteresis operating voltage range.

*2: EFFI = { (output voltage×output current) / (input voltage×input current) }×100

*3: ON resistance (Ω)= (V_{IN} - Lx pin measurement voltage) / 100mA

*4: R&D value

*5: When temperature is high, a current of approximately 10μA (maximum) may leak.

*6: Time until it short-circuits V_{OUT} with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

*7: When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.

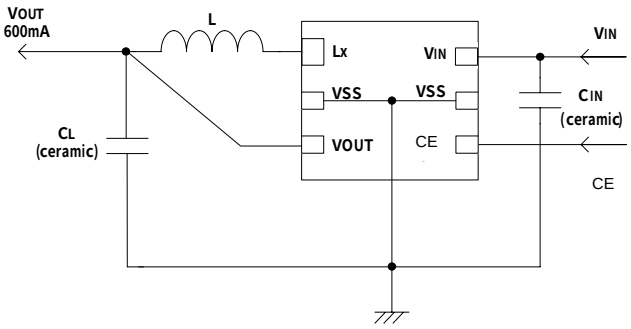
*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

*9: Current limit denotes the level of detection at peak of coil current.

*10: "H"=V_{IN}~V_{IN}-1.2V, "L"=+0.1V~-0.1V

*11: V_{IN} is applied when $V_{OUT(E)}$ x 0.5V becomes more than V_{IN}.

■TYPICAL APPLICATION CIRCUIT



●f_{OSC}=1.2MHz

L:	4.7μH	(NR4018, TAIYO YUDEN)
C_{IN}:	4.7μF	(Ceramic)
C_L:	10μF	(Ceramic)

■OPERATIONAL DESCRIPTION

The XC9254R series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOS driver transistor, N-channel MOS switching transistor for the synchronous switch, current limiter circuit, UVLO circuit and others. (See the block diagram above.) The series ICs compare, using the error amplifier, the voltage of the internal voltage reference source with the feedback voltage from the VOUT pin through split resistors, R1 and R2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage. The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor such as a ceramic capacitor is used ensuring stable output voltage.

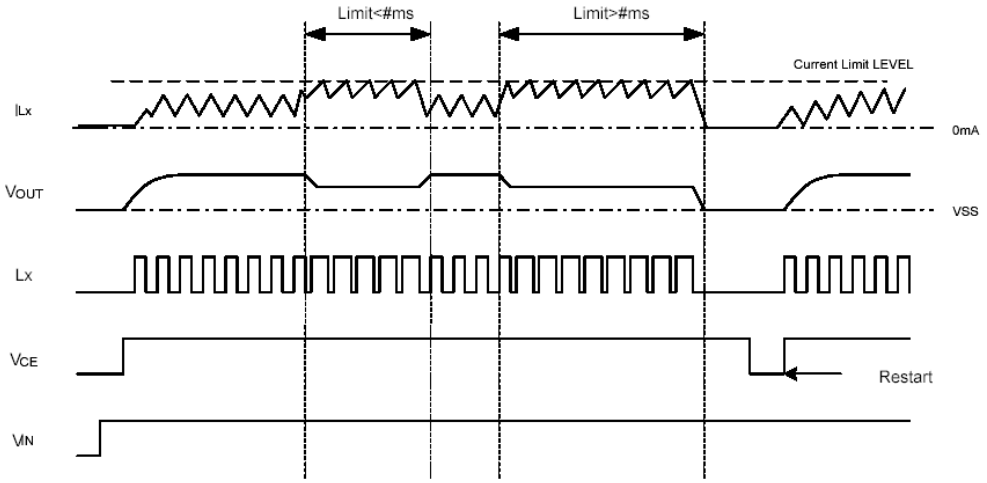
<Reference Voltage Source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally as 1.2MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R1 and R2. When a voltage lower than the reference voltage is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

<Current Limit>
The current limiter circuit of the XC9254R series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the operation suspension mode.

① When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing.
② When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③ At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
④ When the over current state is eliminated, the IC resumes its normal operation.
The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for a few ms and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor, and goes into operation suspension mode. Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the CE/MODE pin, or by restoring power to the V_{IN} pin. The suspension mode does not mean a complete shutdown, but a state in which pulse output is suspended; therefore, the internal circuitry remains in operation. The current limit of the XC9254R series can be set at 1050mA at typical. Besides, care must be taken when laying out the PC Board, in order to prevent misoperation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.



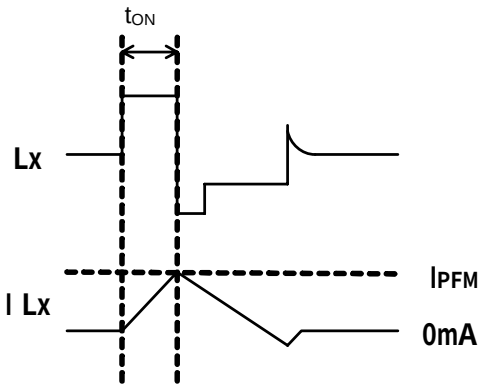
■OPERATIONAL DESCRIPTION (Continued)

<Short-Circuit Protection>
The short-circuit protection circuit monitors the internal R1 and R2 divider voltage from the V_{OUT} pin (refer to FB point in the block diagram shown in the previous page). In case where output is accidentally shorted to the Ground and when the FB point voltage decreases less than half of the reference voltage (Vref) and a current more than the I_{LIM} flows to the Pch MOS driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor. In latch mode, the operation can be resumed by either turning the IC off and on via the CE pin, or by restoring power supply to the V_{IN} pin.
When sharp load transient happens, a voltage drop at the V_{OUT} is propagated to the FB point through C_{FB}, as a result, short circuit protection may operate in the voltage higher than 1/2 V_{OUT} voltage.

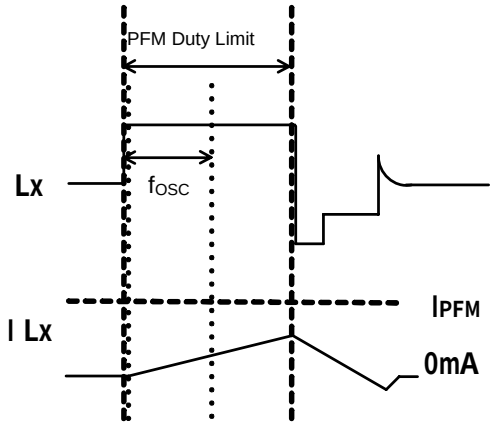
<UVLO Circuit>
When the V_{IN} pin voltage becomes 1.4V or lower, the Pch MOS driver transistor output driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage becomes 1.8V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the V_{IN} pin voltage falls momentarily below the UVLO operating voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

<PFM Switch Current>
In PFM control operation, until coil current reaches to a specified level (I_{PFM}), the IC keeps the Pch MOS driver transistor on. In this case, time that the Pch MOS driver transistor is kept on (t_{ON}) can be given by the following formula.
$t_{ON} = L \times I_{PFM} / (V_{IN} - V_{OUT})$ →I_{PFM}①

< PFM Duty Limit >
In PFM control operation, the PFM duty limit (DTY_{LIMIT_PFM}) is set to 200% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-down ratio is small), it's possible for Pch MOS driver transistor to be turned off even when coil current doesn't reach to I_{PFM}. →I_{PFM}②



IPFM ①



IPFM ②

■OPERATIONAL DESCRIPTION (Continued)

＜C_L High Speed Discharge＞

The XC9254R series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the Nch MOS switch transistor located between the L_X pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value (R) and an output capacitor value (C_L) as τ (τ =C x R), discharge time of the output voltage after discharge via the N channel transistor is calculated by the following formulas.

$V = V_{OUT(E)} \times e^{-t/\tau}$ or $t = \tau \ln (V_{OUT(E)} / V)$

V : Output voltage after discharge

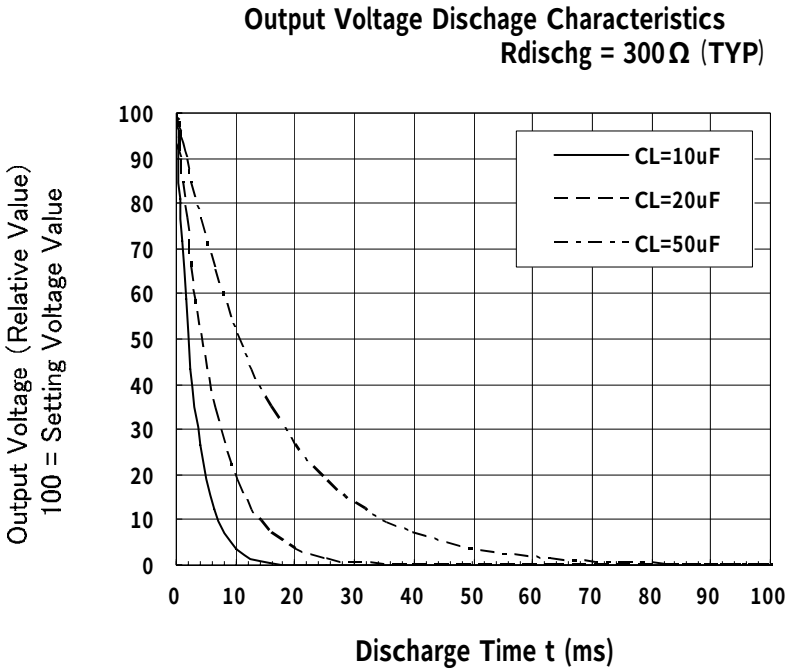
$V_{OUT(E)}$: Output voltage

t: Discharge time,

τ : C x R

C= Capacitance of Output capacitor (C_L)

R= C_L auto-discharge resistance



■OPERATIONAL DESCRIPTION (Continued)

<CE Pin Function>
The operation of the XC9254R series will enter into the shut down mode when a low level signal is input to the CE pin. During the shutdown mode, the current consumption of the IC becomes 0μA (TYP.), with a state of high impedance at the Lx pin and VOUT pin. The IC starts its operation by inputting a high level signal to the CE pin. The input to the CE pin is a CMOS input and the sink current is 0μA (TYP.).

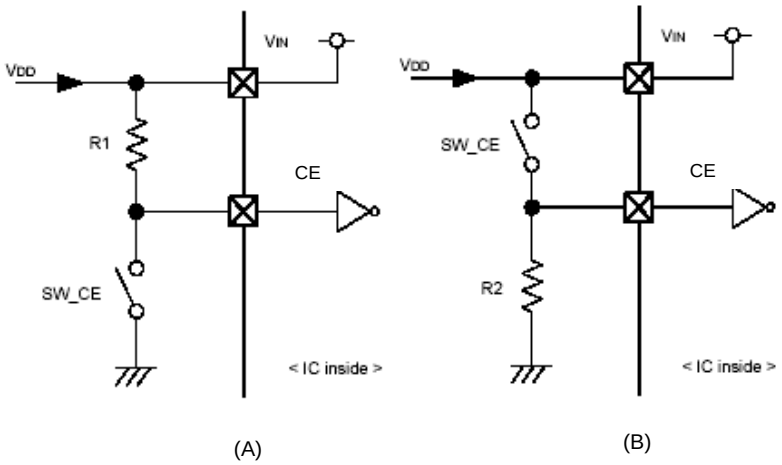
●Examples of how to use CE pin

(A)

SW_CE	STATUS
ON	Stand-by
OFF	Operation

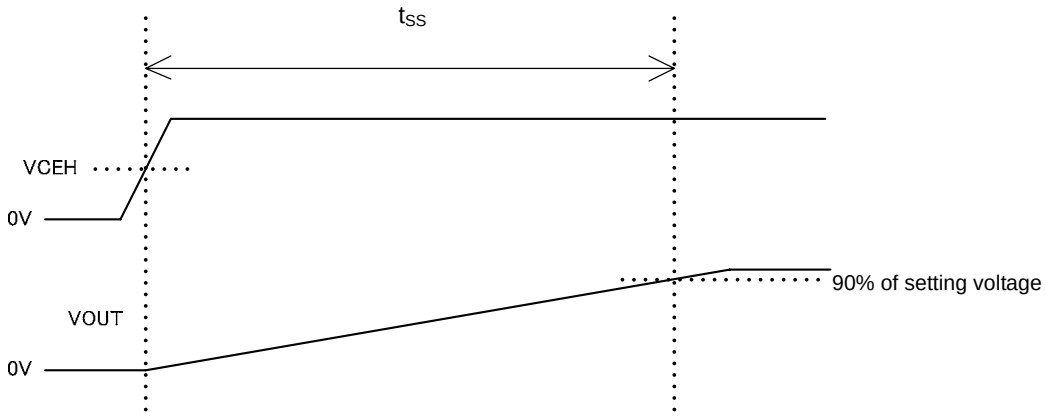
(B)

SW_CE	STATUS
ON	Operation
OFF	Stand-by



(A) (B)

<Soft Start>
The XC9254R series provide 1.0ms (TYP).
Soft start time is defined as the time interval to reach 90% of the output voltage from the time when the CE pin is turned on.

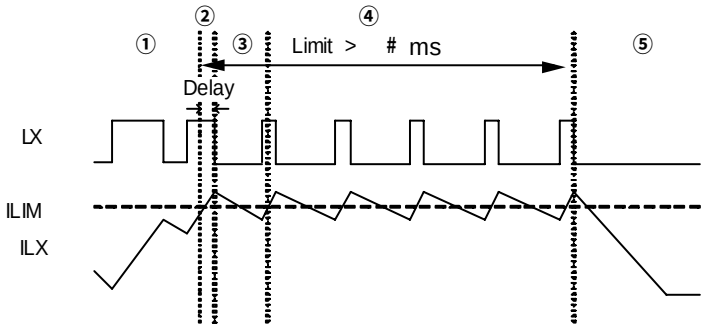


■FUNCTION CHART

CE VOLTAGE LEVEL	OPERATIONAL STATES
H Level	Synchronous PWM/PFM Automatic Switching
L Level	Stand-by

■NOTE ON USE

1. The XC9254R series is designed for use with ceramic output capacitors. If, however, the potential difference is too large between the input voltage and the output voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.
2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.
3. Depending on the input-output voltage differential, or load current, some pulses may be skipped, and the ripple voltage may increase.
4. When the difference between V_{IN} and V_{OUT} is large in PWM control, very narrow pulses will be outputted, and there is the possibility that some cycles may be skipped completely.
5. When the difference between V_{IN} and V_{OUT} is small, and the load current is heavy, very wide pulses will be outputted and there is the possibility that some cycles may be skipped completely.
6. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operation, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:
   $Ipk = (V_{IN} - V_{OUT}) \times OnDuty / (2 \times L \times f_{OSC}) + I_{OUT}$
   L: Coil Inductance Value
   f_{OSC}: Oscillation Frequency
7. When the peak current which exceeds limit current flows within the specified time, the built-in Pch MOS driver transistor turns off. During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the external components such as a coil.
8. When V_{IN} is less than 2.4V, limit current may not be reached because voltage falls caused by ON resistance.
9. Care must be taken when laying out the PC Board, in order to prevent misoperation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.
10. Use of the IC at voltages below the recommended voltage range may lead to instability.
11. This IC should be used within the stated absolute maximum ratings in order to prevent damage to the device.
12. When the IC is used in high temperature, output voltage may increase up to input voltage level at no load because of the leak current of the driver transistor.
13. The current limit is set to 1350mA (MAX.) at typical. However, the current of 1350mA or more may flow. In case that the current limit functions while the V_{OUT} pin is shorted to the GND pin, when Pch MOS driver transistor is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when Nch MOS driver transistor is ON, there is almost no potential difference at both ends of the coil since the V_{OUT} pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. Even in this case, however, after the over current state continues for several ms, the circuit will be latched. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.
   ①Current flows into Pch MOS driver transistor to reach the current limit (I_{LIM}).
   ②The current of I_{LIM} or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of Pch MOS driver transistor.
   ③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
   ④Lx oscillates very narrow pulses by the current limit for several ms.
   ⑤The circuit is latched, stopping its operation.



■NOTE ON USE (Continued)

14. In order to stabilize V_{IN}'s voltage level and oscillation frequency, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} & V_{SS} pins.
15. High step-down ratio and very light load may lead an intermittent oscillation.
16. During PWM / PFM automatic switching mode, operating may become unstable at transition to continuous mode. Please verify with actual parts.
17. Please note the inductance value of the coil. The IC may enter unstable operation if the combination of ambient temperature, setting voltage, oscillation frequency, and L value are not adequate.
    In the operation range close to the maximum duty cycle, The IC may happen to enter unstable output voltage operation even if using the L values listed below.

●The Range of L Value

f_{OSC}	V_{OUT}	L Value
1.2MHz	V_{OUT}=1.2V	3.3μH～6.8μH

*When a coil less value of 4.7μH is used at f_{OSC}=1.2MHz, peak coil current more easily reach the current limit I_{LMI}. In this case, it may happen that the IC can not provide 600mA output current.

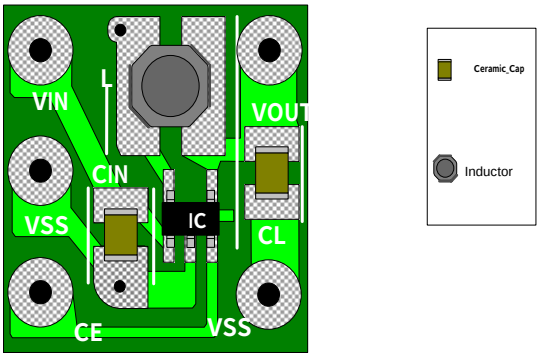
18. It may happen to enter unstable operation when the IC operation mode goes into continuous operation mode under the condition of small input-output voltage difference. Care must be taken with the actual design unit.

■NOTE ON USE (Continued)

●Instructions of pattern layouts

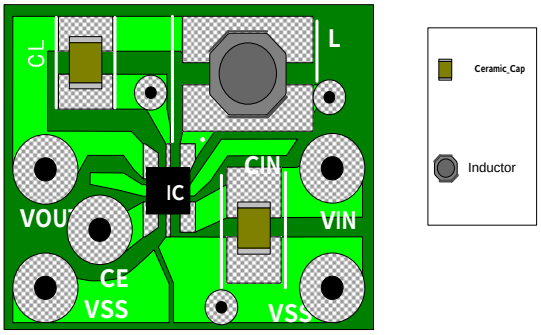
1. In order to stabilize VIN voltage level, we recommend that a by-pass capacitor (CIN) be connected as close as possible to the VIN & VSS pins.
2. Please mount each external component as close to the IC as possible.
3. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. Make sure that the PCB GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
5. This series' internal driver transistors bring on heat because of the output current and ON resistance of driver transistors.

(PKG:SOT-25)



For the V_{IN}, V_{OUT}, V_{SS}/CE, please put the wire.

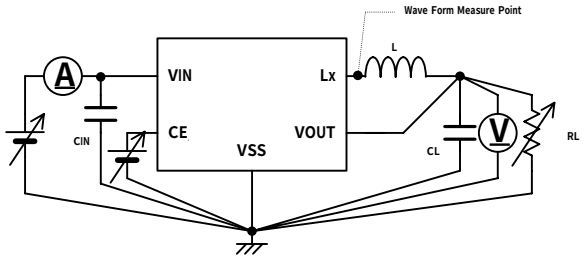
(PKG: USP-6C)



For the V_{IN}, V_{OUT}, V_{SS}/CE, please put the wire.

■TEST CIRCUITS

< Circuit No.1 >

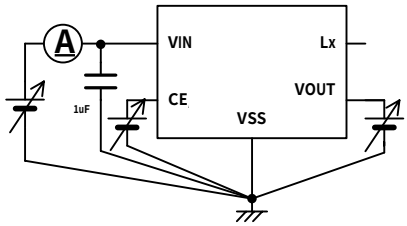


※ External Components

L : 1.5uH(NR3015) 3.0MHz
4.7uH(NR4018) 1.2MHz

CIN : 4.7μF(ceramic)
CL :10μF(ceramic)

< Circuit No.2 >



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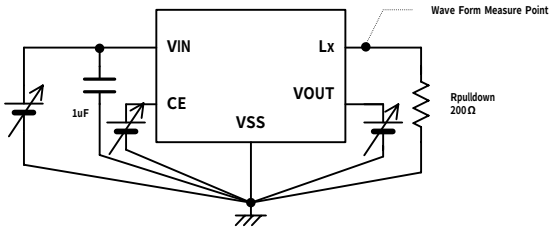

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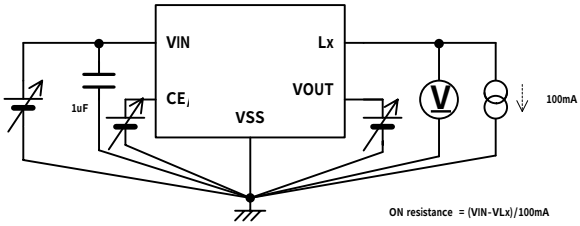
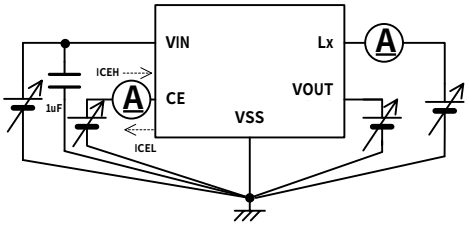


ON resistance = (VIN-VLx)/100mA

< Circuit No.5 >



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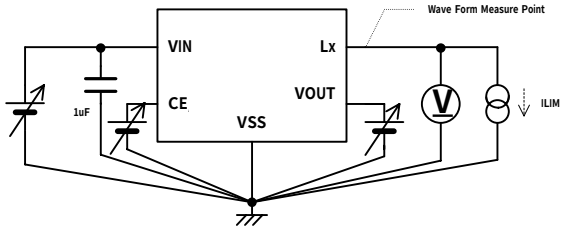

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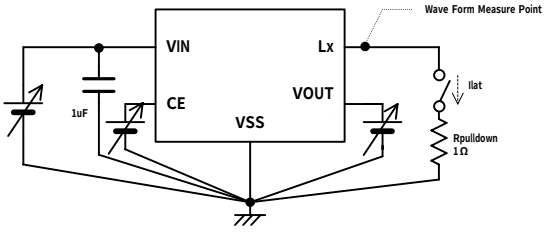

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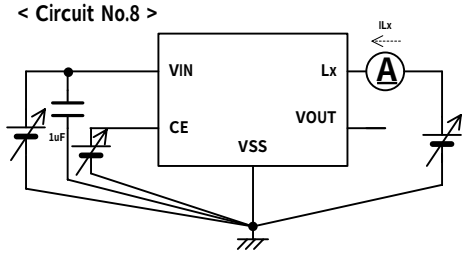

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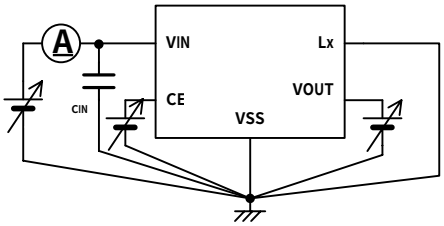
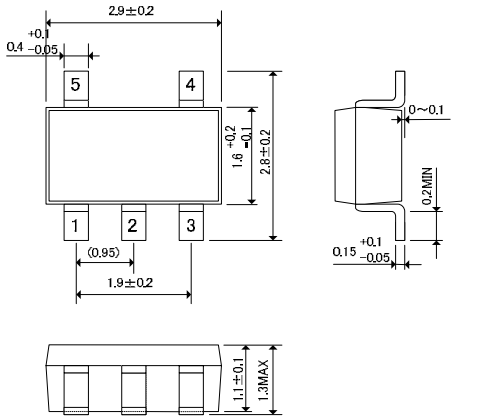


■PACKAGING INFORMATION

●SOT-25

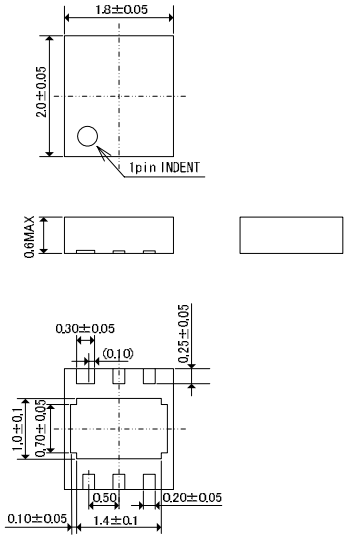
(unit : mm)



SOT−25 Package

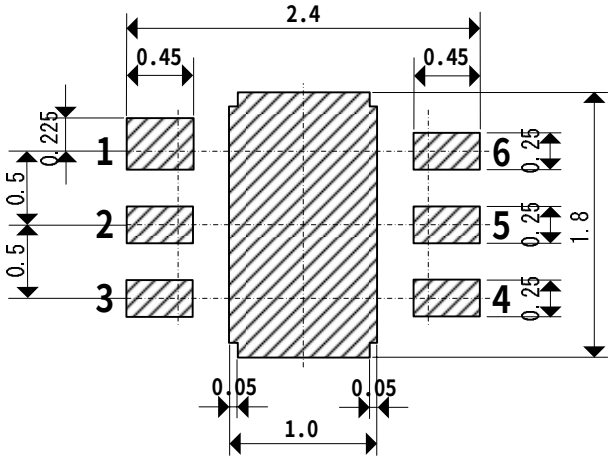
●USP-6C

(unit : mm)

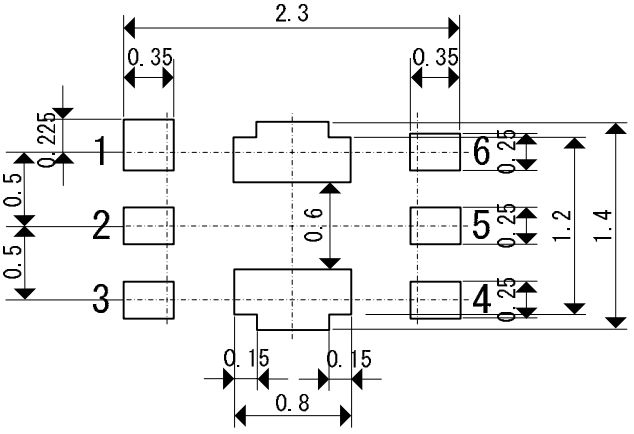


USP−6C Package

●USP-6C Reference Pattern Layout

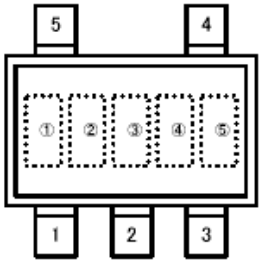


●USP-6C Reference Metal Mask Design

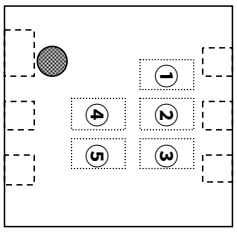


■MARKING RULE

●SOT-25, USP-6C



SOT-25
(TOP VIEW)



USP-6C
(TOP VIEW)

① represent product series

PRODUCT SERIES	MARK
XC9254R	L

② represents integer number of output voltage and oscillation frequency

OUTPUT VOLTAGE (V)	MARK
	f_{OSC}=1.2MHz
1.X	B

③ represents decimal point of output voltage

V_{OUT} (V)	MARK
X.20	2

④⑤ represents production lot number
Order of 01, …09, 10, 11, …99, 0A, …0Z, 1A, …9Z, A0, …Z9, AA, …ZZ.
(G, I, J, O, Q, W excluded)
*No character inversion used.

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