XCR5128C: 128 Macrocell CPLD with Enhanced Clocking

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Product Specification

Features

- Industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- 5V, In-System Programmable (ISP) using a JTAG interface
  - On-chip supervoltage generation
  - ISP commands include: Enable, Erase, Program, Verify
  - Supported by multiple ISP programming platforms
  - Four pin JTAG interface (TCK, TMS, TDI, TDO)
  - JTAG commands include: Bypass, Idcode
- High speed pin-to-pin delays of 7.5 ns
- Ultra-low static power of less than 100 µA
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Up to 20 clocks available
- Support for complex asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Xilinx CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-state buffer
  - Asynchronous macrocell register preset/reset
  - Up to two asynchronous clocks
- Programmable global 3-state pin facilitates `bed of nails' testing without using logic resources
- Available in TQFP and LQFP packages
- Available in both Commercial and Industrial grades

Description

The XCR5128C CPLD (Complex Programmable Logic Device) is a member of the CoolRunner® family of CPLDs from Xilinx. These devices combine high speed and zero power in a 128 macrocell CPLD. With the FZP design technique, the XCR5128C offers true pin-to-pin speeds of 7.5 ns, while simultaneously delivering power that is less than 100 µA at standby without the need for “turbo bits” or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. These devices are the first TotalCMOS PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP design technique.

The Xilinx FZP CPLDs utilize the patented XPLA (eXtended Programmable Logic Array) architecture. The XPLA architecture combines the best features of both PLA and PAL type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA structure in each logic block provides a fast 7.5 ns PAL path with five dedicated product terms per output. This PAL path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 9.5 ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The XCR5128C CPLDs are supported by industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses Xilinx developed tools including WebFITTER.

The XCR5128C CPLD is electrically reprogrammable using industry standard device programmers from vendors such

as Data I/O, BP Microsystems, SMS, and others. The XCR5128C also includes an industry-standard, IEEE 1149.1, JTAG interface through which In-System Programming (ISP) and reprogramming of the device are supported.

XPLA Architecture

Figure 1 shows a high level block diagram of a 128 macrocell device implementing the XPLA architecture. The XPLA architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

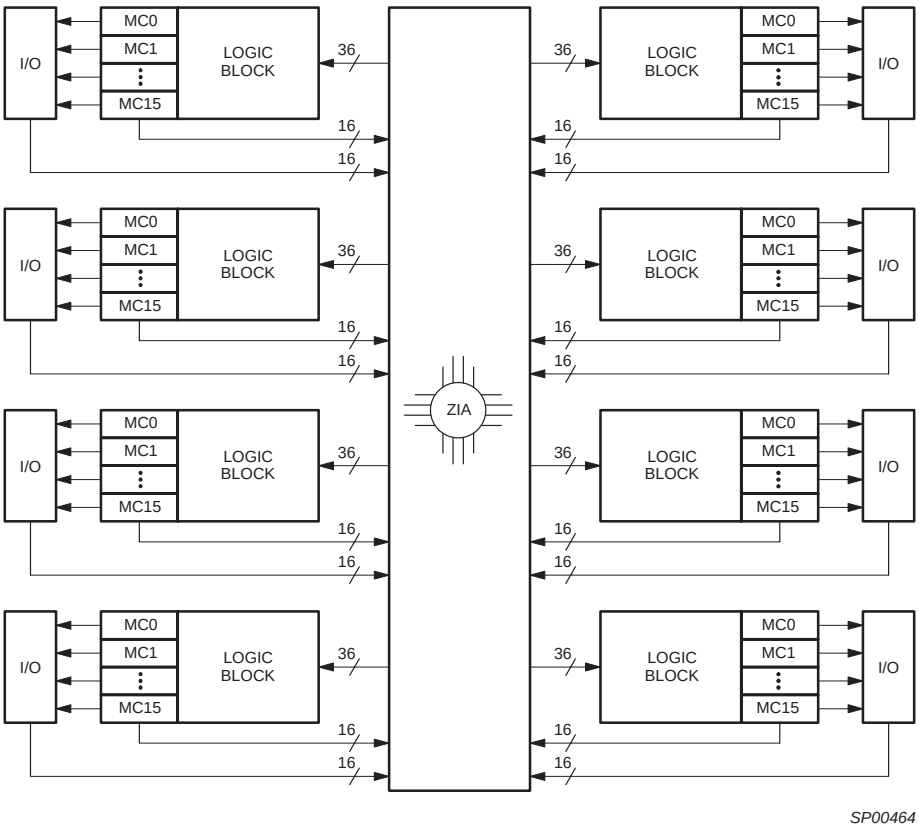


Figure 1: Xilinx XPLA CPLD Architecture

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. The six control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. In addition, two of the control terms can be used as clock signals (see Macrocell Architecture section for details). The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has five dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the XCR5128C device through the PAL array is 7.5 ns. If a macrocell needs more than five product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using one or all 32 PLA product terms is just 2 ns. So the total pin-to-pin t_{PD} for the XCR5128C using six to 37 product terms is 9.5 ns (7.5 ns for the PAL + 2 ns for the PLA).

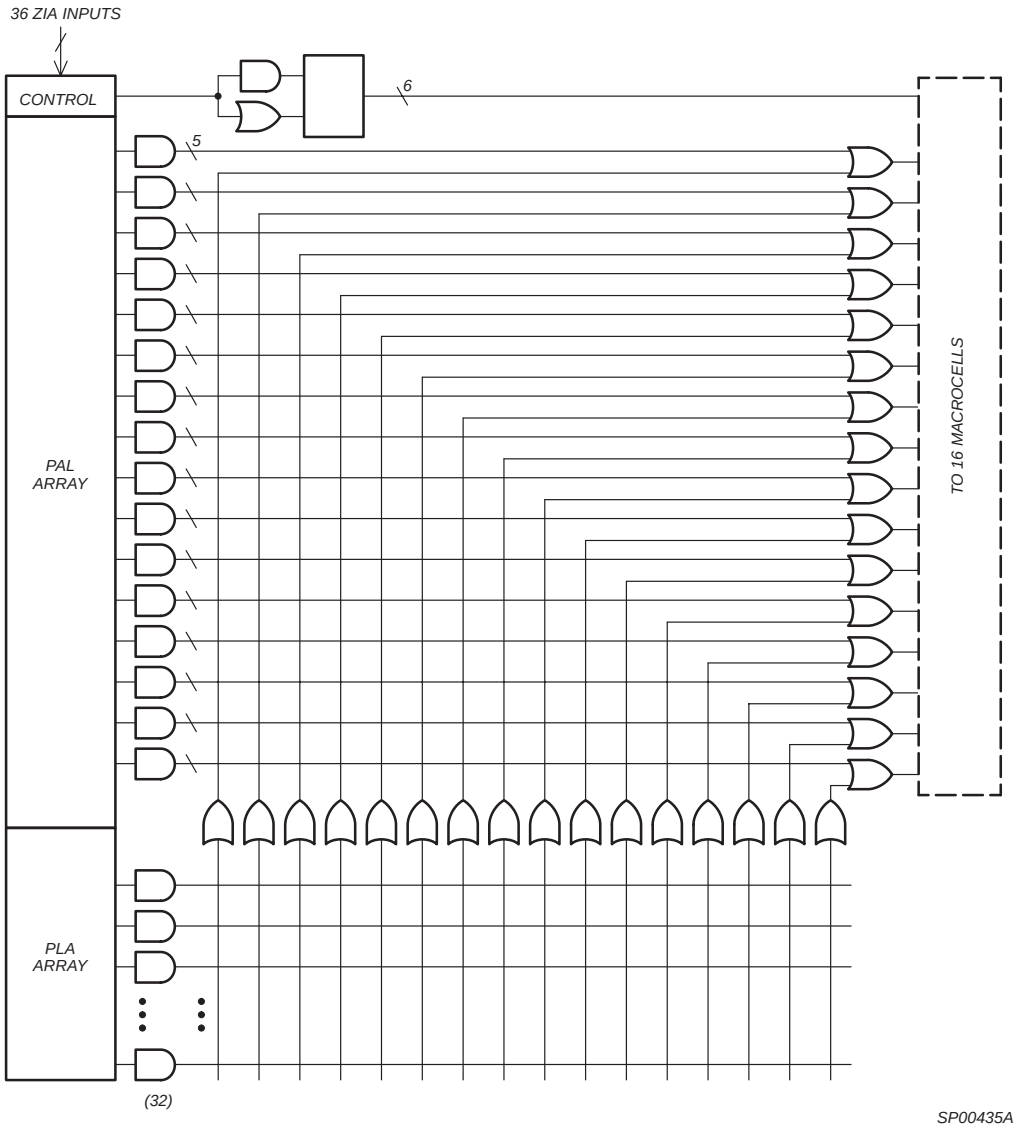


Figure 2: Xilinx XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner XCR5128C. The macrocell can be configured as either a D- or T-type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of six sources. Four of the clock sources (CLK0, CLK1, CLK2, CLK3) are connected to low-skew, device-wide clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. Clock 0 (CLK0) is designated as a “synchronous” clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can be used as “synchronous” clocks that are driven by an external source, or as “asynchronous” clocks that are driven by a macrocell equation. CLK0, CLK1, CLK2 and CLK3 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are two of the six control terms (CT2 and CT3) provided in each logic block. These clocks can be individually configured as either a PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. The timing for asynchronous and control term clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced.

The six control terms of each logic block are used to control the asynchronous Preset/Reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1 are used to control the asynchronous Preset/Reset of the macrocell's flip-flop. Note that the Power-on Reset leaves all macrocells in the “zero” state when power is properly applied, and that the Preset/Reset feature for each macrocell can also be disabled. Control terms CT2 and CT3 can be used as a clock signal to the flip-flops of the macrocells, and as the Output Enable of the macrocell's output buffer. Control terms CT4 and CT5 can be used to control the Output Enable of the macrocell's output buffer. Having four dedicated Output Enable control terms ensures that the CoolRunner devices are PCI compliant. The output buffers can also be always enabled or always disabled. All CoolRunner devices also provide a Global 3-State (GTS) pin, which, when enabled and pulled Low, will 3-state all the outputs of the device. This pin is provided to support “In-Circuit Testing” or “Bed-of-Nails Testing”.

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin feedback path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated (See the section on terminations in this data sheet and the application note *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs*).

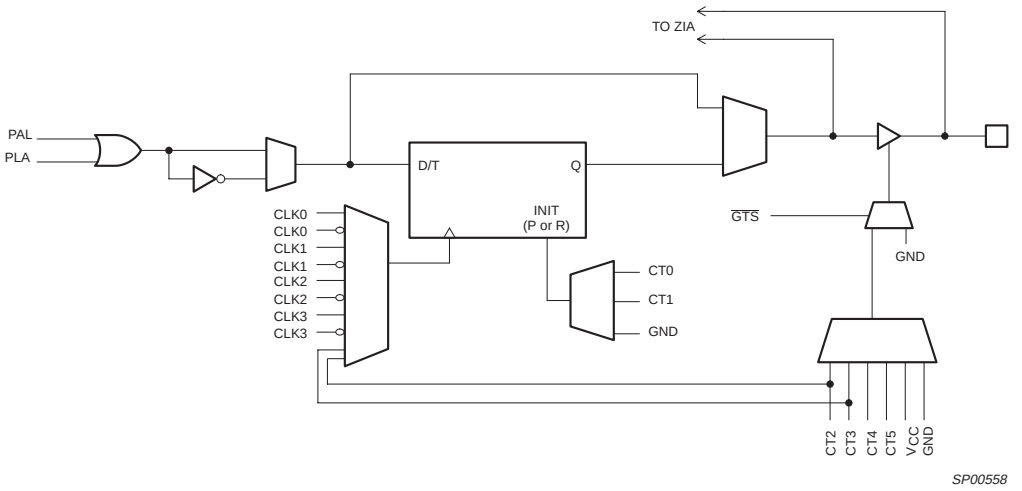


Figure 3: XCR5128C Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner Timing Model. The CoolRunner timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

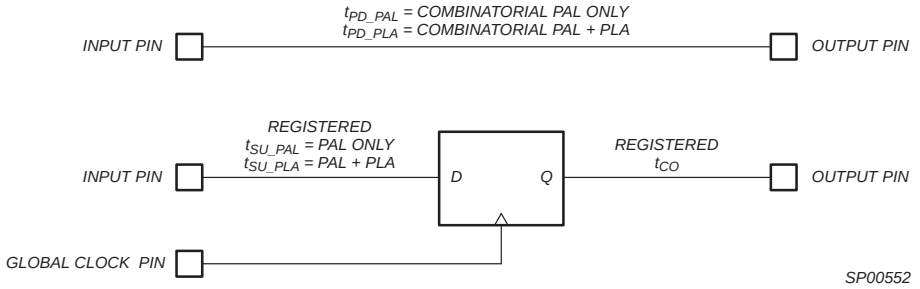


Figure 4: CoolRunner Timing Model

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 1 showing the I_{CC} vs. Frequency of our XCR5128C TotalCMOS CPLD (data taken w/eight up/down, loadable 16 bit counters at 5V, 25°C).

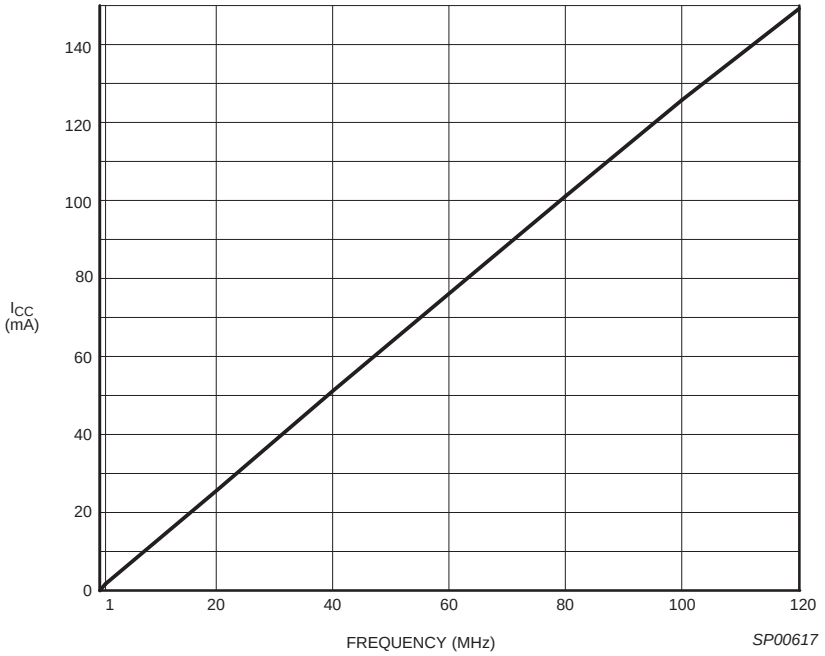


Figure 5: I_{CC} vs. Frequency at V_{CC} = 5.0V, 25°C

Table 1: V_{CC} vs. Frequency (V_{CC} = 5.V, 25°C)

Frequency (MHz)	0	1	20	40	60	80	100	120
Typical I_{CC} (mA)	0.048	1.281	23.55	46.93	70.05	92.45	114.4	136.2

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. The Xilinx XCR5128C devices use the JTAG Interface for In-System Programming/Reprogramming. Although only a subset of the full JTAG command set is implemented (see Table 4), the devices are fully capable of sitting in a JTAG scan chain.

The Xilinx XCR5128C's JTAG interface includes a TAP Port defined by the IEEE 1149.1 JTAG Specification. As implemented in the Xilinx XCR5128C, the TAP Port includes four of the five pins (refer to Table 2) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Xilinx XCR5128C saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Xilinx XCR5128C supports the test reset functionality through the use of its power up reset circuit, which is included in all Xilinx CPLDs. The pins associated with the TAP Port should connect to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

In the Xilinx XCR5128C, the four mandatory JTAG pins each require a unique, dedicated pin on the device. The devices come from the factory with these I/O pins set to perform JTAG functions, but through the software, the final function of these pins can be controlled. If the end application will require the device to be reprogrammed at some future time with ISP, then the pins can be left as dedicated JTAG functions, which means they are not available for use as general purpose I/O pins. However, unlike competing CPLDs, the Xilinx XCR5128C allow the macrocells associated with these pins to be used as buried logic when the JTAG/ISP function is enabled. This is the default state for the software, and no action is required to leave these pins enabled for the JTAG/ISP functions. If, however, JTAG/ISP is not required in the end application, the software can specify that this function be turned off and that these pins be used as general purpose I/O. Because the devices initially have the JTAG/ISP functions enabled, the JEDEC file can be downloaded into the device once, after which the JTAG/ISP pins will become general purpose I/O. This feature is good for manufacturing because the devices can be programmed during test and assembly of the end product and yet still use all of the I/O pins after the programming is done. It eliminates the need for a costly, separate programming step in the manufacturing process. Of course, if the JTAG/ISP function is never required, this feature can be turned off in the software and the device can be programmed with an industry-standard programmer, leaving the pins available for I/O functions. Table 3 defines the dedicated pins used by the four mandatory JTAG signals for each of the XCR5128C package types.

Table 2: JTAG Pin Description

Pin	Name	Description
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 3: XCR5128C JTAG Pinout by Package Type

Device XCR5128C	(Pin Number / Macrocell #)			
	TCK	TMS	TDI	TDO
100-pin VQFP	62/F15	15/C15	4/B15	73/G15
128-pin TQFP	82/F15	21/C15	8/B15	95/G15

Table 4: XCR5128C Low-Level JTAG Boundary-Scan Commands

INSTRUCTION (Instruction Code) Register Used	DESCRIPTION
Bypass (1111) Bypass Register	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
Idcode (0001) Boundary-Scan Register	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.

5V, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-Functional hardware
  - Reconfigurability for Test
  - Eliminates handling of “fine lead-pitch” components for programming
  - Reduced Inventory and manufacturing costs
  - Improved quality and reliability
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, re-configuration, and customization

The Xilinx XCR5128C allows for 5V, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided supervoltages, so that the XCR5128C may be easily programmed on the circuit board using only the 5V supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the XCR5128C enable this feature. The ISP commands implemented in the Xilinx XCR5128C are specified in Table 5 Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command.

Terminations

The CoolRunner XCR5128C CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The XCR5128C CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-downs are automatically activated by the fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. Xilinx recommends that any unused I/O pins on the XCR5128C device be left unconnected.

There are no on-chip pull-down structures associated with the dedicated input pins. Xilinx recommends that any unused dedicated inputs be terminated with external 10kΩ pull-up resistors. These pins can be directly connected to V_{CC} or GND, but using the external pull-up resistors maintains maximum design flexibility should one of the unused dedicated inputs be needed due to future design changes.

When using the JTAG/ISP functions, it is also recommended that 10kΩ pull-up resistors be used on each of the pins associated with the four mandatory JTAG signals. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times. See the application notes *JTAG and ISP Overview for Xilinx XPLA1 and XPLA2 CPLDs* and *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs* for more information.

Table 5: Low Level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	1001	Enables the Erase, Program, and Verify commands.
Erase (ISP Shift Register)	1010	Erases the entire EEPROM array.
Program (ISP Shift Register)	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row.
Verify (ISP Shift Register)	1100	Transfers the data from the addressed row to the ISP Shift Register.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Xilinx XCR5128C supports the following methods:

- PC parallel port
- Workstation or PC serial port
- Embedded processor
- Automated test equipment
- Third party programmers
- High-End ISP Tools

For more details on JTAG and ISP for the XCR5128C, refer to the related application note: *JTAG and ISP Overview for Xilinx XPLA1 and XPLA2 CPLDs*.

Table 6: Programming Specifications

Symbol	Parameter	Min.	Max.	Unit
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	4.5	5.5	V
I_{CCP}	I_{CC} limit program/verify		200	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{SOL}	Output voltage (Low)		0.5	V
V_{SOH}	Output voltage (High)	2.4		V
TDO_I_{OL}	Output current (Low)	12		mA
TDO_I_{OH}	Output current (High)	-12		mA
AC Parameters				
f_{MAX}	TCK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		µs
INIT	Initialization time	100		µs
TMS_SU	TMS setup time before TCK ↑	10		ns
TDI_SU	TDI setup time before TCK ↑	10		ns
TMS_H	TMS hold time after TCK ↑	20		ns
TDI_H	TDI hold time after TCK ↑	20		ns
TDO_CO	TDO valid after TCK ↓		30	ns

Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage[2]	-0.5	7.0	V
V_I	Input voltage	-1.2	V_{CC} +0.5	V
V_{OUT}	Output voltage	-0.5	V_{CC} +0.5	V
I_{IN}	Input current	-30	30	mA
I_{OUT}	Output current	-100	100	mA
T_J	Maximum junction temperature	-40	150	°C
T_{str}	Storage temperature	-65	150	°C

Notes:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to +70°C	5.0V +5%
Industrial	-40 to +85°C	5.0V +10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 4.75V ≤ V_{CC} ≤ 5.25V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.75V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.25V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.75V, I_{OL} = 12 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.75V, I_{OH} = -12 mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 5.25V, T_{AMB} = 0°C		100	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 5.25V, T_{AMB} = 0°C at 1 MHz		3	mA
		V_{CC} = 5.25V, T_{AMB} = 0°C at 50 MHz		75	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-200	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 7 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 4.75V ≤ V_{CC} ≤ 5.25V

Symbol	Parameter	7		10		12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	2	12	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	9.5	3	12	3	14.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	5.5	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	4.5		7		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	6.5		9		10.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		4		ns
t_{CL}	Clock Low time	3		4		4		ns
t_R	Input Rise time		20		20		20	ns
t_F	Input Fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	167		125		125		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	111		80		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	95		71		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	6	2	8.5	2	10.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	8	3	10.5	3	13	ns
t_{CF}	Clock to internal feedback node delay time		4		5.5		6.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50		50	µs
t_{ER}	Input to output disable[2, 3]		9		12		15	ns
t_{EA}	Input to output valid[2]		9		12		15	ns
t_{RP}	Input to register preset[2]		11		12.5		15	ns
t_{RR}	Input to register reset[2]		11		12.5		15	ns

Notes:

1. Specifications measured with one output switching. See Figure 6and Table 6 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

DC Electrical Characteristics For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 4.5V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 5.5V	2.0		V
V_I	Input clamp voltage	V_{CC} = 4.5V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 4.5V, I_{OL} = 12 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 4.5V, I_{OH} = -12 mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 5.5V, T_{AMB} = -40°C		125	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 5.5V, T_{AMB} = -40°C at 1MHz		4	mA
		V_{CC} = 5.5V, T_{AMB} = -40°C at 50 MHz		80	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-230	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		10	pF

Notes:

1. See Table 1 on page 7 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] for Industrial Grade Devices

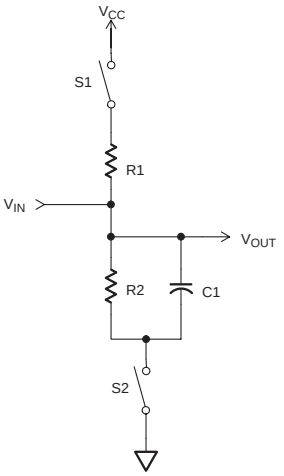
Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 4.5V ≤ V_{CC} ≤ 5.5V

Symbol	Parameter	10		15		Unit
		Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	15	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	12	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	8		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	10		10.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	5		5		ns
t_{CL}	Clock Low time	5		5		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	100		100		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	71		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	66		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	8.5	2	13.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL + PLA	3	10.5	3	16	ns
t_{CF}	Clock to internal feedback node delay time		6		6.5	ns
t_{INIT}	Delay from valid V_C to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		15		15	ns
t_{EA}	Input to output valid[2]		15		15	ns
t_{RP}	Input to register preset[2]		15		17	ns
t_{RR}	Input to register reset[2]		15		17	ns

Notes:

1. Specifications measured with one output switching. See Figure 6 and Table 7 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5pF.

Switching Characteristics



COMPONENT	VALUES
R1	390Ω
R2	390Ω
C1	35 pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Closed
t_P	Closed	Closed

Note: For t_{PHZ} and t_{PLZ} C = 5 pF, and 3-state levels are measured 0.5V from steady state active level.

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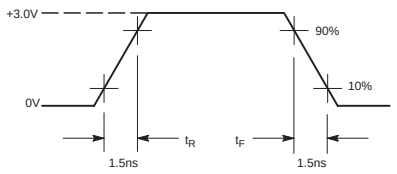
Voltage Waveform



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MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

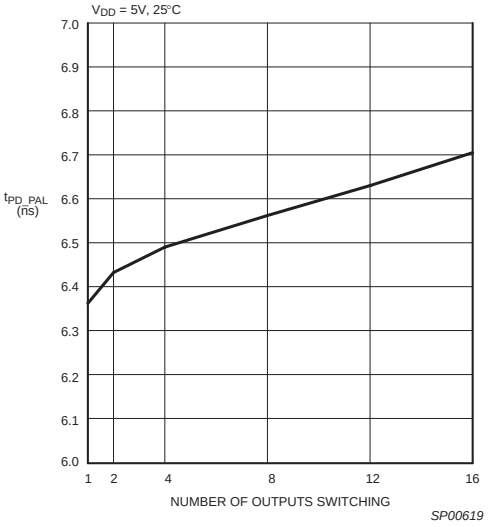

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Figure 6: t_{PD_PAL} vs. Outputs Switching

Table 7: t_{PD_PAL} vs. Number of Outputs Switching (V_{CC} = 5V, 25°C)

Number Of Outputs	1	2	4	8	12	16
Typical (ns)	6.362	6.432	6.49	6.562	6.63	6.705

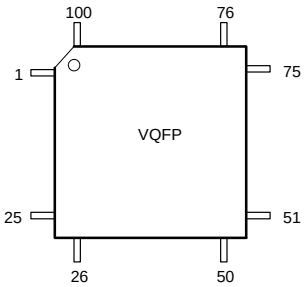
Pin Functions and Layouts

Pin Functions

XCR5128C - 100-pin VQFP and 128-pin TQFP Function Table

Pin #	Function		Pin #	Function		Pin #	Function		Pin #	Function	
	VQFP	TQFP		VQFP	TQFP		VQFP	TQFP		VQFP	TQFP
1	I/O-A2	I/O-A3	33	I/O-D5	NC	65	I/O-G4	I/O-E15	97	I/O-A8	NC
2	I/O-A0	I/O-A2	34	V_{CC}	NC	66	V_{CC}	V_{CC}	98	I/O-A7	NC
3	V_{CC}	I/O-A0	35	I/O-D4	NC	67	I/O-G5	I/O-F0	99	I/O-A5	NC
4	I/O-B15 (TDI)	NC	36	I/O-D2	I/O-C0	68	I/O-G7	NC	100	I/O-A4	I/O-H0
5	I/O-B13	NC	37	I/O-D0/CLK2	GND	69	I/O-G8	NC	101	-	I/O-H2
6	I/O-B12	NC	38	GND	I/O-D15	70	I/O-G10	NC	102	-	I/O-H3
7	I/O-B10	V_{CC}	39	V_{CC}	I/O-D13	71	I/O-G12	I/O-F2	103	-	I/O-H4
8	I/O-B8	I/O-B15 (TDI)	40	I/O-E0/CLK1	I/O-D12	72	I/O-G13	I/O-F3	104	-	I/O-H5
9	I/O-B7	I/O-B13	41	I/O-E2	I/O-D11	73	I/O-G15 (TDO)	I/O-F4	105	-	I/O-H7
10	I/O-B5	I/O-B12	42	I/O-E4	I/O-D10	74	GND	I/O-F5	106	-	I/O-H8
11	GND	I/O-B11	43	GND	I/O-D8	75	I/O-H0	I/O-F7	107	-	I/O-H10
12	I/O-B4	I/O-B10	44	I/O-E5	I/O-D7	76	I/O-H2	I/O-F8	108	-	V_{CC}
13	I/O-B2	I/O-B8	45	I/O-E7	I/O-D5	77	I/O-H4	I/O-F10	109	-	I/O-H11
14	I/O-B0	I/O-B7	46	I/O-E8	V_{CC}	78	I/O-H5	GND	110	-	I/O-H12
15	I/O-C15 (TMS)	I/O-B5	47	I/O-E10	I/O-D4	79	I/O-H7	I/O-F11	111	-	I/O-H13
16	I/O-C13	GND	48	I/O-E12	I/O-D3	80	I/O-H8	I/O-F12	112	-	I/O-H15
17	I/O-C12	I/O-B4	49	I/O-E13	I/O-D2	81	I/O-H10	I/O-F13	113	-	GND
18	V_{CC}	I/O-B3	50	I/O-E15	I/O-D0/CLK2	82	V_{CC}	I/O-F15 (TCK)	114	-	IN0/CLK0
19	I/O-C10	I/O-B2	51	V_{CC}	GND	83	I/O-H12	I/O-G0	115	-	IN2/gtsn
20	I/O-C8	I/O-B0	52	I/O-F0	V_{CC}	84	I/O-H13	I/O-G2	116	-	IN1
21	I/O-C7	I/O-C15 (TMS)	53	I/O-F2	I/O-E0/CLK1	85	I/O-H15	I/O-G3	117	-	IN3
22	I/O-C5	I/O-C13	54	I/O-F4	I/O-E2	86	GND	I/O-G4	118	-	V_{CC}
23	I/O-C4	I/O-C12	55	I/O-F5	I/O-E3	87	IN0/CLK0	V_{CC}	119	-	I/O-A15/CLK3
24	I/O-C2	I/O-C11	56	I/O-F7	I/O-E4	88	IN2/gtsn	I/O-G5	120	-	I/O-A13
25	I/O-C0	V_{CC}	57	I/O-F8	GND	89	IN1	I/O-G7	121	-	I/O-A12
26	GND	I/O-C10	58	I/O-F10	I/O-E5	90	IN3	I/O-G8	122	-	I/O-A12
27	I/O-D15	I/O-C8	59	GND	I/O-E7	91	V_{CC}	I/O-G10	123	-	GND
28	I/O-D13	I/O-C7	60	I/O-F12	I/O-E8	92	I/O-A15/CLK3	I/O-G11	124	-	I/O-A10
29	I/O-D12	I/O-C5	61	I/O-F13	I/O-E10	93	I/O-A13	I/O-G12	125	-	I/O-A8
30	I/O-D10	I/O-C4	62	I/O-F15 (TCK)	I/O-E11	94	I/O-A12	I/O-G13	126	-	I/O-A7
31	I/O-D8	I/O-C3	63	I/O-G0	I/O-E12	95	GND	I/O-G15 (TDO)	127	-	I/O-A5
32	I/O-D7	I/O-C2	64	I/O-G2	I/O-E13	96	I/O-A10	GND	128	-	I/O-A4

100-Pin VQFP



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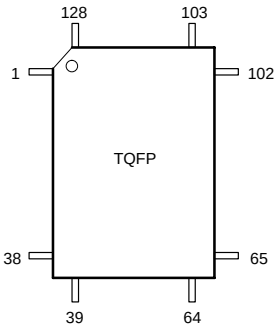
128-pin TQFP



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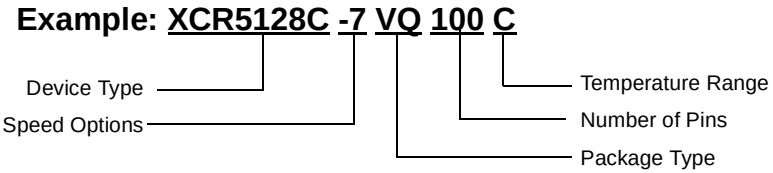
Ordering Information



Speed Options
-15: 15 ns pin-to-pin delay
-12: 12 ns pin-to-pin delay
-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
VQ100: 100-pin VQFP
TQ128: 128-pin TQFP

Component Availability

Pins		100	128
Type		Plastic VQFP	Plastic TQFP
Code		VQ100	TQ128
XCR5128C	-15	I	I
	-12	C	C
	-10	C, I	C, I
	-7	C	C

Revision History

Date	Version #	Revision
9/16/99	1.0	Initial Xilinx release.
2/10/00	1.1	Converted to Xilinx format and updated.
8/10/00	1.2	Updated Figure 3 and pinout table.