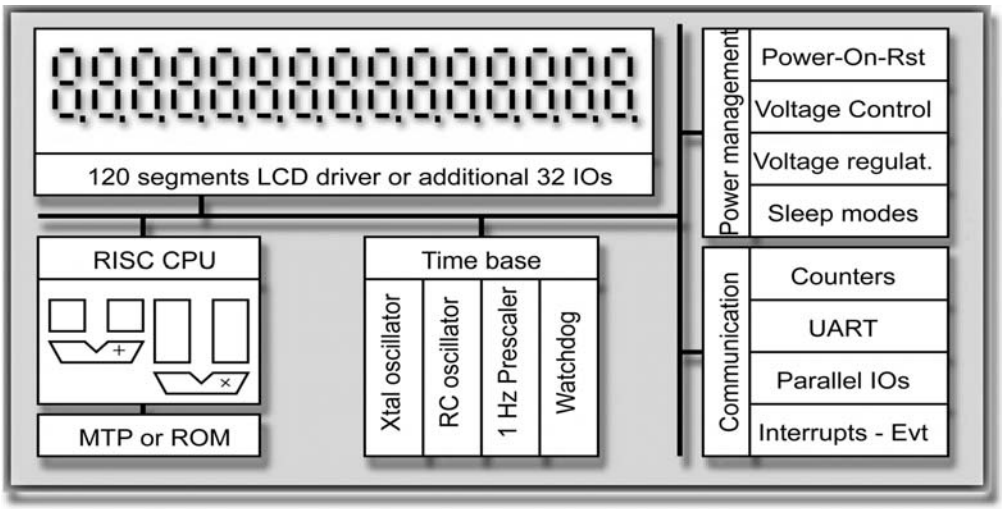

XE88LC04

Ultra low-power MCU with LCD driver

General Description

- The XE88LC04 is an ultra low-power low-voltage microcontroller unit (MCU) with extremely high efficiency, allowing for 1 MIPS at 300uA and 2.4 V, and 8 x 8 bits multiplying in one clock cycle at 1.2 V.
- The XE88LC04 includes an LCD driver for up to 120 segments. The LCD lines can be used as additional IOs.
- XE88LC04 is available with on chip ROM or Multiple-Time-Programmable (MTP) program memory.

Applications

- Portable, battery operated instruments
- RF system supervisor
- Remote control
- HVAC control
- Watches

Key product Features

- Low-voltage low-power controller operation
  - 4 MIPS at 2.4 V to 5.5 V supply (ROM)
  - 2 MIPS at 2.4 V to 5.5 V supply (MTP)
  - 300 µA at 1 MIPS, 2.4 V to 5.5 V supply
- 22 kByte (8 kInstruction) MTP, 1032 Byte RAM
- RC and crystal oscillators
- 5 reset, 16 interrupt, 8 event sources
- 120 segments LCD driver
- 100 years MTP Flash retention at 55°C

Ordering Information

Product	Temperature range	Memory type	Package
XE88LC04MI03x	-40°C to 85 °C	MTP	BGA

1 Detailed Pin Description

To be added

2 Absolute maximum ratings

Stresses beyond these listed in this chapter may cause permanent damage to the device. No functional operation is implied at or beyond these conditions. Exposure to these conditions for an extended period may affect the device reliability.

Parameter	Valéue
VBAT with respect to VSS	-0.3V to 6.0V
Input voltage on any input pin	VSS-0.3V to VBAT+0.3V
Storage temperature	-55°C to 125°C
Storage temperature for programmed MTP devices	-40°C to 85°C

Table 2.1: Absolute maximum ratings

These devices are ESD sensitive. Although these devices feature proprietary ESD protection structures, permanent damage may occur on devices subjected to high energy electrostatic discharges. Proper ESD precautions have to be taken to avoid performance degradation or loss of functionality.

3 Electrical Characteristics

All specification are -40°C to 85°C unless otherwise noted. ROM operates up to 125°C.

Operation conditions		min	typ	max	Unit	Remarks
Power supply	ROM version	2.4		5.5	V	
	MTP version	2.4		5.5	V	
Operating speed	2.4 V to 5.5 V	0.032		4	MHz	
Instruction cycle	any instruction		250		ns	7
Current requirement	CPU running at 1 MIPS			310	uA	1
	CPU running at 32 kHz on Xtal, RC off			10	uA	1
	CPU halt, timer on Xtal, RC off			1	uA	1
	CPU halt, timer on Xtal, RC ready			1.7	uA	1
	CPU halt, Xtal off timer on RC at 100 kHz			1.4	uA	1
	Voltage level detection			15	uA	
MTP Flash instruction memory	Prog. voltage	10.3		10.8	V	
	Erase time	0.2		1	s	8
	Write/Erase cycles	10	100			5
	Data retention	10			years	85°C, 2
		100			years	55°C, 2

Table 3.1: Specifications and current requirement of the XE88LC04

Note:
1) Power supply: 2.4 V - 5.5 V, temperature is 27°C.
2) < 10 erase cycles.
3) Output not loaded.
4) Current requirement can be divided by a factor of 2 or 4 by reducing the speed accordingly.
5) More cycles possible during development, with restraint retention
6) Power supply: 3.0V, at 27°C;
7) With 4 MHz clock, all instructions are using exactly 1 clock cycle
8) Longer erase time may degrade retention

4 CPU

The XE88LC06 CPU is a low power RISC core. It has 16 internal registers for efficient implementation of the C compiler. Its instruction set is made of 35 generic instructions, all coded on 22 bits, with 8 addressing modes. All instructions are executed in one clock cycle, including conditional jumps and 8x8 multiplication, therefore the XE88LC06 runs at 1 MIPS on a 1 MHz clock.

The CPU description with its instruction set can be found in the XE8000 databook.

The good code efficiency of the XE8000 core makes it possible to compute a polynomial like

$Z = (A_0 + A_1 \cdot Y) \cdot X + B_0 + B_1 \cdot Y$ in less than 300 clock cycles (code generated by the XEMICS C-compiler, all numbers are Signed Integers on 16 bits).

5 Memory organisation

The CPU uses a Harvard architecture, so that memory is organised in two separated fields: program memory and data memory. As both memory are separated, the central processing unit can read/write data at the same time it loads an instruction. Peripherals and system control registers are mapped on data memory space.

Program memory is made in one page. Data is made of several 256 bytes pages.

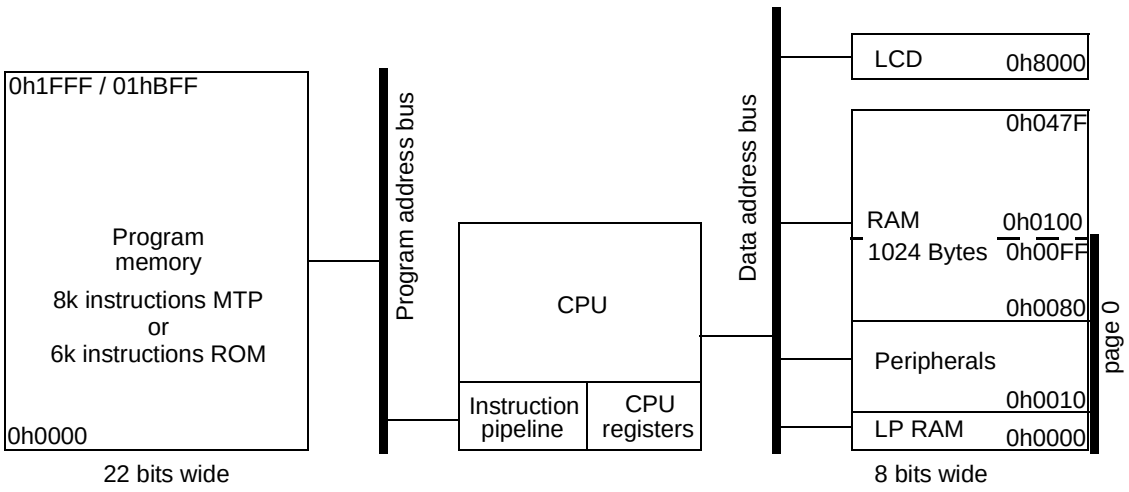

Figure 5.1: Memory organization

5.1 Program memory

The program memory is implemented as Multiple Time Programmable (MTP) Flash memory. The power consumption of MTP memory is linear with the access frequency (no significant static current).

- Size of the MTP Flash memory is 8192 x 22 bits (= 22 kBytes)
- Size of the ROM memory is 6144 x 22 bits (= 17 kBytes)

block	size	address
MTP	8192 x 22	H0000 - H1FFF
ROM	6144 x 22	H0000 - H1BFF

Table 5.1: Program addresses for MTP or ROM memory

5.2 Data memory

The data memory is implemented as static Random-Access Memory (RAM). The RAM size is 512 x 8 bits plus 8 low power RAM bytes that require very low current when addressed. Programs using the low-power RAM instead of RAM will use even less current.

block	size	address
LP RAM	8 x 8	H0000 - H0007
RAM	1024 x 8	H0080 - H047F

Table 5.2: RAM addresses

6 Registers list

Left column include register name and address.

Right columns include bit name, access (r: read, r0: always 0 when read, w: write, c: cleared by writing any value, c1: cleared by writing 1), and reset status (0 or 1) and signal. Empty bits are reserved for future use and should not be written, neither should their read value be used for any purpose as it may change without notice.

6.1 Peripherals mapping

block	size	address	Page
LP RAM	8x8	H0000-H0007	
System control	16x8	H0010-H001F	
Port A	8x8	H0020-H0027	
Port B	8x8	H0028-H002F	
Port C	4x8	H0030-H0033	
Port D	4x8	H0034-H0037	
MTP	4x8	H0038-H003B	
Event	4x8	H003C-H003F	
Interrupts control	8x8	H0040-H0047	Page 0
reserved	8x8	H0048-H004F	
UART	8x8	H0050-H0057	
Counters	8x8	H0058-H005F	
Reserved	8x8	H0060-H0067	
SPI	8x8	H0068-H006F	
Reserved	12x8	H0070-H007B	
VLD	4x8	H007C-H007F	
RAM1	128x8	H0080 - H00FF	
RAM2	256x8	H0100 - H01FF	
RAM3	256x8	H0200 - H02FF	
RAM4	256x8	H0300 - H03FF	
RAM5	128x8	H0400 - H047F	
LCD	32x8	H8000-H803F	

Table 6.1: Peripherals addresses

6.2 Resets

The reset source name is simplified in the following registers description. Name mapping is in the next table.

reset source	name in this document
nresetglobal	global
nresetcold	cold
nresetpconf	pconf
nresetsleep	sleep

Table 6.2: Reset signal name mapping

6.3 Low power RAM

Low power RAM is a small additionnal RAM area with extremely low power requirement.

Name Address	7	6	5	4	3	2	1	0
h0000	rw	rw	rw	rw	rw	rw	rw	rw
h0001	rw	rw	rw	rw	rw	rw	rw	rw
h0002	rw	rw	rw	rw	rw	rw	rw	rw
h0003	rw	rw	rw	rw	rw	rw	rw	rw
h0004	rw	rw	rw	rw	rw	rw	rw	rw
h0005	rw	rw	rw	rw	rw	rw	rw	rw
h0006	rw	rw	rw	rw	rw	rw	rw	rw
h0007	rw	rw	rw	rw	rw	rw	rw	rw

Table 6.3: Low power RAM

6.4 System, oscillators, prescaler and watchdog

Name Address	7	6	5	4	3	2	1	0
RegSysCtrl h0010	SleepEn rw, 0 cold	EnReset-PConf rw, 0 cold	EnBus-Error rw, 0 cold	EnResWD rw, 0 cold				
RegSysReset h0011	Sleep w, 0 global	SleepFlag rc, 0 cold	ResBus-Error rc, 0 cold	ResWD rc, 0 cold	ResPortA rc, 0 cold			
RegSysClock h0012		ExtClk r, 0 cold	EnExtClk rw, 0 cold	BiasRC rw, 1 cold	ColdXtal r, 1 sleep		EnableXtal rw, 0 sleep	EnableRC rw, 1 sleep
RegSysMisc h0013							Output16k rw, 0 sleep	Output-CkCPU rw, 0 sleep
RegSysWD h0014					WatchDog(3) special	WatchDog(2) special	WatchDog(1) special	WatchDog(0) special
RegSysPre0 h0015								ResPre ClearLow-Prescal (*) w, 0 cold
RegSysRCTrim1 h001B				RCFreq-Range rw, 0 cold	RCFreq-Coarse(3) rw, 0 cold	RCFreq-Coarse(2) rw, 0 cold	RCFreq-Coarse(1) rw, 0 cold	RCFreq-Coarse(0) rw, 0 cold
RegSysRCTrim2 h001C			RCFreq-Fine(5) rw, 1 cold	RCFreq-Fine(4) rw, 0 cold	RCFreq-Fine(3) rw, 0 cold	RCFreq-Fine(2) rw, 0 cold	RCFreq-Fine(1) rw, 0 cold	RCFreq-Fine(0) rw, 0 cold
RegSysVIReg h001D								

Table 6.4: System control registers

6.5 PortA

Name Address	7	6	5	4	3	2	1	0
RegPAIn h0020	PAIn(7) r	RegPAIn(6) r	PAIn(5) r	PAIn(4) r	PAIn(3) r	PAIn(2) r	PAIn(1) r	PAIn(0) r
RegPADebounce h0021	PADeb(7) rw, 0 pconf	PADeb(6) rw, 0 pconf	PADeb(5) rw, 0 pconf	PADeb(4) rw, 0 pconf	PADeb(3) rw, 0 pconf	PADeb(2) rw, 0 pconf	PADeb(1) rw, 0 pconf	PADeb(0) rw, 0 pconf
RegPAEdge h0022	PAEdge(7) rw, 0 global	PAEdge(6) rw, 0 global	PAEdge(5) rw, 0 global	PAEdge(4) rw, 0 global	PAEdge(3) rw, 0 global	PAEdge(2) rw, 0 global	PAEdge(1) rw, 0 global	PAEdge(0) rw, 0 global
RegPAPullup h0023	PAPullUp(7) rw, 1 pconf	PAPullUp(6) rw, 1 pconf	PAPullUp(5) rw, 1 pconf	PAPullUp(4) rw, 1 pconf	PAPullUp(3) rw, 1 pconf	PAPullUp(2) rw, 1 pconf	PAPullUp(1) rw, 1 pconf	PAPullUp(0) rw, 1 pconf
RegPARes0 h0024	PARes0(7) rw, 0 global	PARes0(6) rw, 0 global	PARes0(5) rw, 0 global	PARes0(4) rw, 0 global	PARes0(3) rw, 0 global	PARes0(2) rw, 0 global	PARes0(1) rw, 0 global	PARes0(0) rw, 0 global
RegPARes1 h0025	PARes1(7) rw, 0 global	PARes1(6) rw, 0 global	PARes1(5) rw, 0 global	PARes1(4) rw, 0 global	PARes1(3) rw, 0 global	PARes1(2) rw, 0 global	PARes1(1) rw, 0 global	PARes1(0) rw, 0 global
RegSysPACtrl h0026								DebFast rw, 0 pconf
RegSysPASnap h0027	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd

Table 6.5: Port A registers

6.6 PortB

Name Address	7	6	5	4	3	2	1	0
RegPBOut h0028	PBOut(7) rw, 0 pconf	PBOut(6) rw, 0 pconf	PBOut(5) rw, 0 pconf	PBOut(4) rw, 0 pconf	PBOut(3) rw, 0 pconf	PBOut(2) rw, 0 pconf	PBOut(1) rw, 0 pconf	PBOut(0) rw, 0 pconf
RegPBIn h0029	PBIn(7) r	PBIn(6) r	PBIn(5) r	PBIn(4) r	PBIn(3) r	PBIn(2) r	PBIn(1) r	PBIn(0) r
RegPBDir h002A	PBDir(7) rw, 0 pconf	PBDir(6) rw, 0 pconf	PBDir(5) rw, 0 pconf	PBDir(4) rw, 0 pconf	PBDir(3) rw, 0 pconf	PBDir(2) rw, 0 pconf	PBDir(1) rw, 0 pconf	PBDir(0) rw, 0 pconf
RegPBOpen h002B	PBOpen(7) rw, 0 pconf	PBOpen(6) rw, 0 pconf	PBOpen(5) rw, 0 pconf	PBOpen(4) rw, 0 pconf	PBOpen(3) rw, 0 pconf	PBOpen(2) rw, 0 pconf	PBOpen(1) rw, 0 pconf	PBOpen(0) rw, 0 pconf
RegPBPullup h002C	PBPullUp(7) rw, 1 pconf	PBPullUp(6) rw, 1 pconf	PBPullUp(5) rw, 1 pconf	PBPullUp(4) rw, 1 pconf	PBPullUp(3) rw, 1 pconf	PBPullUp(2) rw, 1 pconf	PBPullUp(1) rw, 1 pconf	PBPullUp(0) rw, 1 pconf
RegPBAna h002D					PBAna(3) rw, 0 pconf	PBAna(2) rw, 0 pconf	PBAna(1) rw, 0 pconf	PBAna(0) rw, 0 pconf

Table 6.6: Port B registers

6.7 PortC

Name Address	7	6	5	4	3	2	1	0
RegPCOut h0030	PCOut(7) rw, 0 pconf	PCOut(6) rw, 0 pconf	PCOut(5) rw, 0 pconf	PCOut(4) rw, 0 pconf	PCOut(3) rw, 0 pconf	PCOut(2) rw, 0 pconf	PCOut(1) rw, 0 pconf	PCOut(0) rw, 0 pconf
RegPCIn h0031	PCIn(7) r	PCIn(6) r	PCIn(5) r	PCIn(4) r	PCIn(3) r	PCIn(2) r	PCIn(1) r	PCIn(0) r
RegPCDir h0032	PCDir(7) rw, 0 pconf	PCDir(6) rw, 0 pconf	PCDir) rw, 0 pconf	PCDir(4) rw, 0 pconf	PCDir(3) rw, 0 pconf	PCDir(2) rw, 0 pconf	PCDir(1) rw, 0 pconf	PCDir(0) rw, 0 pconf
RegPCPullup h0033	PCPullup(7) rw, 1 pconf	PCPullup(6) rw, 1 pconf	PCPullup(5) rw, 1 pconf	PCPullup(4) rw, 1 pconf	PCPullup(3) rw, 1 pconf	PCPullup(2) rw, 1 pconf	PCPullup(1) rw, 1 pconf	PCPullup(0) rw, 1 pconf

Table 6.7: Port C registers

6.8 MTP

Name Address	7	6	5	4	3	2	1	0
RegEEP h0038	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP1 h0039	rw	rw	rw	rw	rw	rw	rw	rw
RegEEP2 h003A	special	special	special	special	special	special	special	special
RegEEP3 h003B	special	special	special	special	special	special	special	special

Table 6.8: MTP control registers

6.9 Events

Name Address	7	6	5	4	3	2	1	0
RegEvn h003C	EvnCntA rc1, 0 global	EvnCntC rc1, 0 global	EvnPre1 rc1, 0 global	EvnPA(1) rc1, 0 global	EvnCntB rc1, 0 global	EvnCntD rc1, 0 global	EvnPre2 rc1, 0 global	EvnPA(0) rc1, 0 global
RegEvnEn h003D	EvnEnCntA rw, 0 global	EvnEnCntC rw, 0 global	EvnEnPre1 rw, 0 global	EvnEnPA(1) rw, 0 global	EvnEnCntB rw, 0 global	EvnEnCntD rw, 0 global	EvnEnPre2 rw, 0 global	EvnEnPA(0) rw, 0 global
RegEvnPriority h003E	EvnPriority(7) r,1 global	EvnPriority(6) r,1 global	EvnPriority(5) r,1 global	EvnPriority(4) r,1 global	EvnPriority(3) r,1 global	EvnPriority(2) r,1 global	EvnPriority(1) r,1 global	EvnPriority(0) r,1 global
RegEvnEvn h003F							EvnHigh r, 0 global	EvnLow r, 0 global

Table 6.9: Events control registers

6.10 Interrupts

Name Address	7	6	5	4	3	2	1	0
RegIrqHig h0040		IrqPre1 rc1, 0 global		IrqCntA rc1, 0 global	IrqCntC rc1, 0 global	IrqCmpd rc1, 0 global	IrqUartTx rc1, 0 global	IrqUartRx rc1, 0 global
RegIrqMid h0041	IrqUsrtCond2 rc1, 0 global	IrqUsrtCond1 rc1, 0 global	IrqPA(5) rc1, 0 global	IrqPA(4) rc1, 0 global	IrqPre2 rc1, 0 global	IrqVld rc1, 0 global	IrqPA(1) rc1, 0 global	IrqPA(0) rc1, 0 global
RegIrqLow h0042	IrqPA(7) rc1, 0 global	IrqPA(6) rc1, 0 global	IrqCntB rc1, 0 global	IrqCntD rc1, 0 global	IrqPA(3) rc1, 0 global	IrqPA(2) rc1, 0 global		
RegIrqEnHig h0043		IrqEnPre1 rw, 0 global		IrqEnCntA rw, 0 global	IrqEnCntC rw, 0 global	IrqEnCmpd rw, 0 global	IrqEnUartTx rw, 0 global	IrqEnUartRx rw, 0 global
RegIrqEnMid h0044	IrqEnUsr-tCond2 rw, 0 global	IrqEnUsrt-Cond1 rw, 0 global	IrqEnPA(5) rw, 0 global	IrqEnPA(4) rw, 0 global	IrqEnPre2 rw, 0 global	IrqEnVld rw, 0 global	IrqEnPA(1) rw, 0 global	IrqEnPA(0) rw, 0 global
RegIrqEnLow h0045	IrqEnPA(7) rw, 0 global	IrqEnPA(6) rw, 0 global	IrqEnCntB rw, 0 global	IrqEnCntD rw, 0 global	IrqEnPA(3) rw, 0 global	IrqEnPA(2) rw, 0 global		
RegIrqPriority h0046	IrqPriority(7) r, 1 global	IrqPriority(6) r, 1 global	IrqPriority(5) r, 1 global	IrqPriority(4) r, 1 global	IrqPriority(3) r, 1 global	IrqPriority(2) r, 1 global	IrqPriority(1) r, 1 global	IrqPriority(0) r, 1 global
RegIrqIrq h0047						IrqHig r, 0 global	IrqMid r, 0 global	IrqLow r, 0 global

Table 6.10: Interrupts control registers

6.11 USRT

Name Address	7	6	5	4	3	2	1	0
RegUsrtS1 h0048								UsrtS1 rw, 1 global
RegUsrtS0 h0049								UsrtS0 rw, 1 global
RegUsrtCtrl h004A					UsrtWaitS0 r, 0 global	UsrtEnWait-Cond1 rw, 0 global	UsrtEnWaitS0 rw, 0 global	UsrtEnable rw, 0 global
RegUsrtCond1 h004B								UsrtCond1 rc, 0 global
RegUsrtCond2 h004C								UsrtCond2 rc, 0 global
RegUsrtBufferS1 h004D								UsrtBufferS1 r
RegUsrtEdgeS0 h004E								UsrtEdgeS0 r, 0 global
Reserved h004F								

Table 6.11: USRT control registers

6.12 UART

Name Address	7	6	5	4	3	2	1	0
RegUartCtrl h0050	UartEcho rw, 0 global	UartEnRx rw, 0 global	UartEnTx rw, 0 global	UartXRx rw, 0 global	UartXTx rw, 0 global	UartBR(2) rw, 1 global	UartBR(1) rw, 0 global	UartBR(0) rw, 1 global
RegUartCmd h0051	SelXtal rw, 0 global	UartWakeup rw, 0 global	UartRCSel(2) rw, 0 global	UartRCSel(1) rw, 0 global	UartRCSel(0) rw, 0 global	UartPM rw, 0 global	UartPE rw, 0 global	UartWL rw, 1 global
RegUartTx h0052	UartTx(7) rw, 0 global	UartTx(6) rw, 0 global	UartTx(5) rw, 0 global	UartTx(4) rw, 0 global	UartTx(3) rw, 0 global	UartTx(2) rw, 0 global	UartTx(1) rw, 0 global	UartTx(0) rw, 0 global
RegUartTxSta h0053							UartTxBusy r, 0 global	UartTxFull r, 0 global
RegUartRx h0054	UartRx(7) r	UartRx(6) r	UartRx(5) r	UartRx(4) r	UartRx(3) r	UartRx(2) r	UartRx(1) r	UartRx(0) r
RegUartRxSta h0055			UartRxSErr r	UartRxPErr r	UartRxFErr r	UartRxOErr c	UartRxBusy r	UartRxFull r
Reserved h0056								
Reserved h0057								

Table 6.12: UART control registers

6.13 Counters

Name Address	7	6	5	4	3	2	1	0
RegCntA h0058	CounterA(7) rw	CounterA(6) rw	CounterA(5) rw	CounterA(4) rw	CounterA(3) rw	CounterA(2) rw	CounterA(1) rw	CounterA(0) rw
RegCntB h0059	CounterB(7) rw	CounterB(6) rw	CounterB(5) rw	CounterB(4) rw	CounterB(3) rw	CounterB(2) rw	CounterB(1) rw	CounterB(0) rw
RegCntC h005A	CounterC(7) rw	CounterC(6) rw	CounterC(5) rw	CounterC(4) rw	CounterC(3) rw	CounterC(2) rw	CounterC(1) rw	CounterC(0) rw
RegCntD h005B	CounterD(7) rw	CounterD(6) rw	CounterD(5) rw	CounterD(4) rw	CounterD(3) rw	CounterD(2) rw	CounterD(1) rw	CounterD(0) rw
RegCntCtrlCk h005C	CntDSel(1) rw	CntDSel(0) rw	CntCSel(1) rw	CntCSel(0) rw	CntBSel(1) rw	CntBSel(0) rw	CntASel(1) rw	CntASel(0) rw
RegCntConfig1 h005D	CntDDownUp rw	CntCDownUp rw	CntBDownUp rw	CntADownUp rw	CascadeCD rw	CascadeAB rw	CntPWM1 rw, 0 global	CntPWM0 rw, 0 global
RegCntConfig2 h005E	CapSel(1) rw, 0 global	CapSel(0) rw, 0 global	CapFunc(1) rw, 0 global	CapFunc(0) rw, 0 global	PWM1Size(1) rw	PWM1Size(0) rw	PWM0Size(1) rw	PWM0Size(0) rw
RegCntOn h005F					CntDEnable rw, 0 global	CntCEnable rw, 0 global	CntBEnable rw, 0 global	CntAEnable rw, 0 global

Table 6.13: Counters control registers

6.14 LP comparators

Name Address	7	6	5	4	3	2	1	0
RegCmpdStat h0072	CmpdStat(3) rc, 0 global	CmpdStat(2) rc, 0 global	CmpdStat(1) rc, 0 global	CmpdStat(0) rc, 0 global	CmpdOut(3) r, 0 global	CmpdOut(2) r, 0 global	CmpdOut(1) r, 0 global	CmpdOut(0) r, 0 global
RegCmpdCtrl h0073	IrqOnRising-Ch(2) rw, 0 global	IrqOnRising-Ch(1) rw, 0 global	IrqOnRising-Ch(0) rw, 0 global	EnIrqCh(3) rw, 0 global	EnIrqCh(2) rw, 0 global	EnIrqCh(1) rw, 0 global	EnIrqCh(0) rw, 0 global	Enable rw, 0 global

Table 6.14: LP comparators control registers

6.15 Vmult and Vld registers

Name Address	7	6	5	4	3	2	1	0
RegVldCtrl h007E					VldMult rw, 0 cold	VldTune(2) rw, 0 cold	VldTune(1) rw, 0 cold	VldTune(0) rw, 0 cold
RegVldStat h007F						VldIrq r, 0 global	VldValid r, 0 global	VldEn rw, 0 global

Table 6.15: Vmult and Vld control registers

6.16 LCD driver registers

Name Address	7	6	5	4	3	2	1	0
starts h8000								

Table 6.16: LCD driver registers

7 Peripherals

The XE88LC04 includes usual microcontroller peripherals and some other blocks more specific to low-voltage or mixed-signal operation. They are 3 parallel ports, one input port (A), one IO and analog port (B) with analog switching capabilities and one general purpose IO port (C). A watchdog is available, connected to a prescaler. Four 8-bit counters, with capture, PWM and chaining capabilities are available. The UART can handle transmission speeds as high as 115kbaud.

Low-power low-voltage blocks include a voltage level detector, two oscillators (one internal 0.1-4 MHz RC oscillator and a 32 kHz crystal oscillator) and a specific regulation scheme that largely uncouples current requirement from external power supply (usual CMOS ASICs require much more current at 5.5 V than they need at 2.4 V. This is not the case for the XE88LC04).

7.1 Counters

- 4 8-bit counters
- Daisy chain on 16 bits
- PWM on 8-16 bits
- Capture - compare on 16 bits
- Events and interrupts generation

7.2 Prescaler

- Interrupt generated with 1 second period for ultra low power hibernation mode

7.3 Watchdog

- 2 seconds watchdog

7.4 UART

- full duplex operation with buffered receiver and transmitter.
- Internal baudrate generator with programmable baudrate (300 - 115000 bauds).
- 7 or 8 bits word length.
- even, odd, or no-parity bit generation and detection
- 1 stop bit
- error receive detection : Start, Parity, Frame and Overrun
- receiver echo mode
- 2 interrupts (receive full and transmit empty)
- enable receive and/or transmit
- invert pad Rx and/or Tx

7.5 Xtal clock

The Xtal Oscillator operates with an external crystal of 32’768 Hz.

symbol	description	min	typ	max	unit	comments
f_clk32k	nominal frequency		32768		Hz	
st_x32k	oscillator start-up time		1	2	s	for full precision
duty_clk32k	duty cycle on the digital output	30	50	70	%	
fstab_1	relative frequency deviation from nominal, for a crystal with CL=8.2 pF and temperature between -40° and +85°C	-100		+300	ppm	not included: crystal frequency tolerance and aging crystal frequency - temperature depen

Table 7.1: Xtal oscillator specifications.

Note: Board layout recommendations for safer crystal oscillation and lower current consumption:
Keep lines xtal_in and xtal_out short and insert a VSS line between them.
Connect package of the crystal to VSS.
No noisy or digital lines near xtal_in and xtal_out.
Insert guards at VSS where needed.

7.6 RC oscillator

The RC Oscillator is always turned on at power-on reset and can be turned off after the optional Xtal oscillator has been started. The RC oscillator has two frequency ranges: sub-MHz (100KHz to 1MHz) and above-MHz (1MHz to max MCU frequency). Inside a range, the frequency can be tuned by software for coarse and fine adjustment.

Note: No external component is required for the RC oscillator.

The RC oscillator can be in 3 modes. In mode 1(RC on), the RC oscillator and its bias are on. In mode 2 (RC ready), the RC oscillator is off and the bias is on. In mode 3 (RC off), the RC oscillator and the bias are off. RC ready mode is a compromise between power consumption and start-up time.

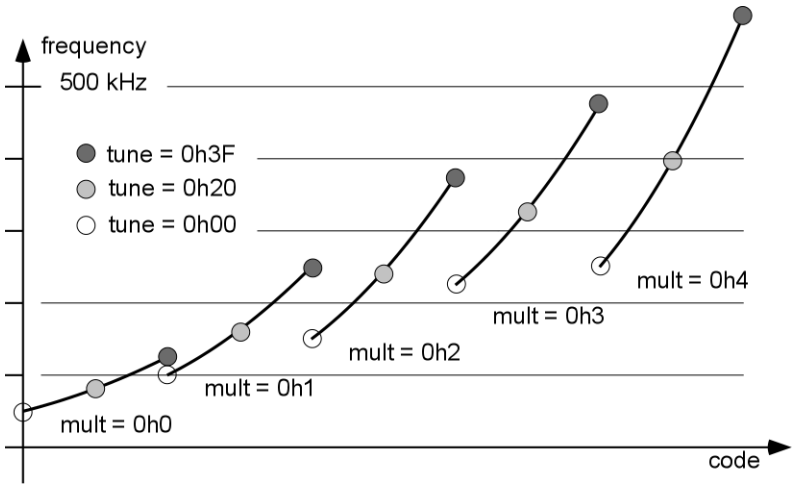

Figure 7.1: RC frequencies programming example for low range (typical values)

symbol	description	min	typ	max	unit	comments
F_{st}	frequency at start-up	50	80	110	kHz	
range	range selection	1		10		multiplies F_{st}
mult[3:0]	coarse tuning range	1		16		4 bits, multiplies F_{st} * range
tune[5:0]	fine tuning range	0.65		1.5		6 bits, multiplies F_{st} * range * mult
	fine tuning step		1.4	2	%	
T_{st}	start-up time		30	50	µs	bias current is off (RC off)
O_{st}	overshoot at start-up			50	%	bias current is off (RC off)
T_{wu}	wakeup time		3	5	µs	bias current is on (RC ready)
O_{wu}	overshoot at wakeup			50	%	bias current is on (RC ready)
jit	jitter rms		2		$^{o}/_{oo}$	

Table 7.2: RC specifications

7.7 Parallel IO ports

- 8 bit input port A with interrupt, reset and event generation.
- 8 bit input-output-analog port B with analog switching capabilities.

- 8 bit input-output port C.

sym	description	condition	min	typ	max	unit	Comments
	Port A: low threshold limit	Vbat = 1.2 V				V	
	Port A: high threshold limit					V	
	output drop when sinking 1 mA				0.4	V	
	output drop when sourcing 1 mA				0.4	V	
	Port A: low threshold limit	Vbat = 2.4 V		1		V	
	Port A: high threshold limit			1.5		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	Port A: low threshold limit	Vbat = 5.0 V		2		V	
	Port A: high threshold limit			3		V	
	output drop when sinking 1 mA					V	
	output drop when sinking 8 mA				0.4	V	
	output drop when sourcing 1 mA					V	
	output drop when sourcing 8 mA				0.4	V	
	pull-up, pull-down resistor		50		150	kohm	

Table 7.3: IO pins performances

7.8 Voltage level detector

- Can be switched off, on or simultaneously with CPU activities
- Generates an interrupt if power supply is below a pre-determined level

The Voltage Level Detector monitors the state of the system battery. It returns a logical high value (an interrupt) in the status register if the supplied voltage drops below the user defined level.

symbol	description	min	typ	max	unit	comments	
Vth	Threshold voltage	Note 1			V	trimming values:	
						VldRange	Vld
			1.53			0	0
			1.44			0	0
			1.36			0	0
			1.29			0	0
			1.22			0	1
			1.16			0	1
			1.11			0	1
			1.06			0	1
			3.06			1	0
			2.88			1	0
			2.72			1	0
			2.57			1	0
			2.44			1	1
			2.33			1	1
			2.22			1	1
			2.13			1	1
T_{EOM}	duration of measurement		2.0	2.5	ms	Note 2	
T_{PW}	Minimum pulse width detected		875	1350	us	Note 2	

Table 7.4: Voltage level detector operation

Note: **1)** Absolute precision of the threshold voltage is ±10%.
2) This timing is respected in case the internal RC or crystal oscillators are selected. Refer to the clock block documentation in case the external clock is used.

8 LCD drivers

The XE88LC04 includes LCD drivers for up to 120 segments. Multiplex can be chosen between 1 and 4. Intermediate voltages for multiplex signals can be generated on chip, even at very low power supply, thanks to a 1.2 V voltage reference and to 2 voltage multipliers.

The voltage generator of the XE88LC04 can be used in a multitude of ways: for generating absolute voltages (above or below Vbat), for generating voltages relative to Vbat, or for generating voltages relative to an external reference. This great variety of possibilities make possible to have devices compensated for temperature, or to operate LCD with good contrast even with limited voltage supply.

Registers h0068 to h0076 carry the segment value, register h0077 carries the Vref setup (on-off), Vref multiplier setup (on-off), LCD update frequency (off, 16 Hz, 32 Hz, 64 Hz), LCD size (25 lines or 30 lines) and multiplex selection (1, 2, 3 or 4).

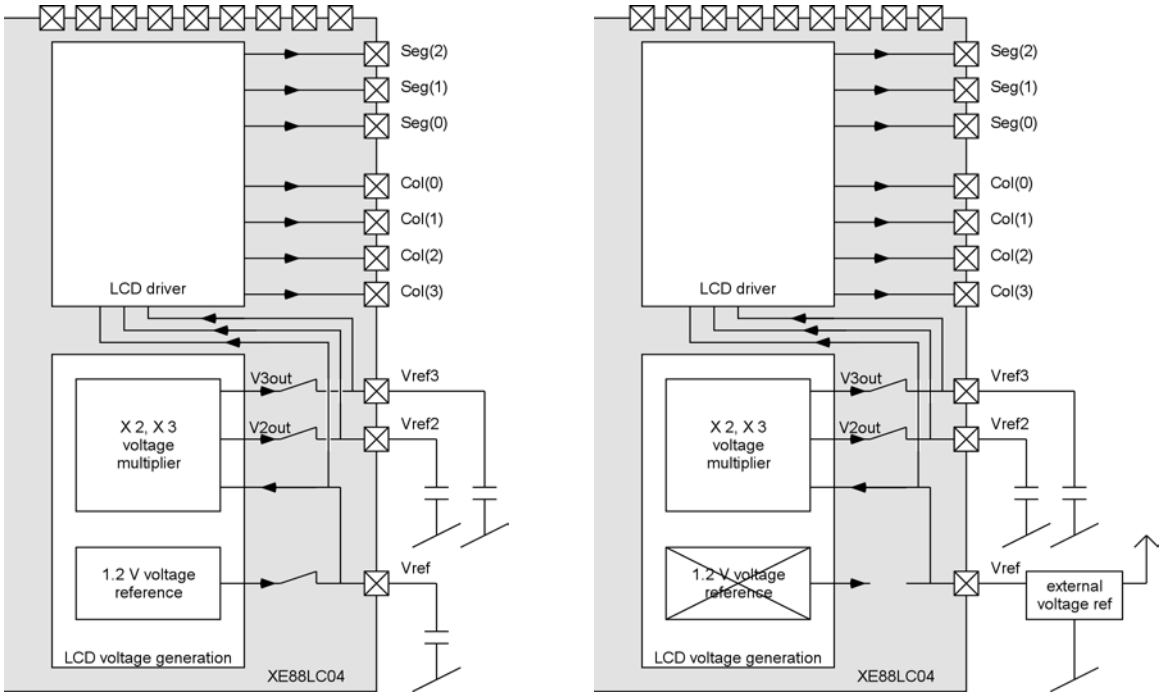

Figure 8.1: Generating absolute voltages for the LCD driver, either with internal reference (left) or

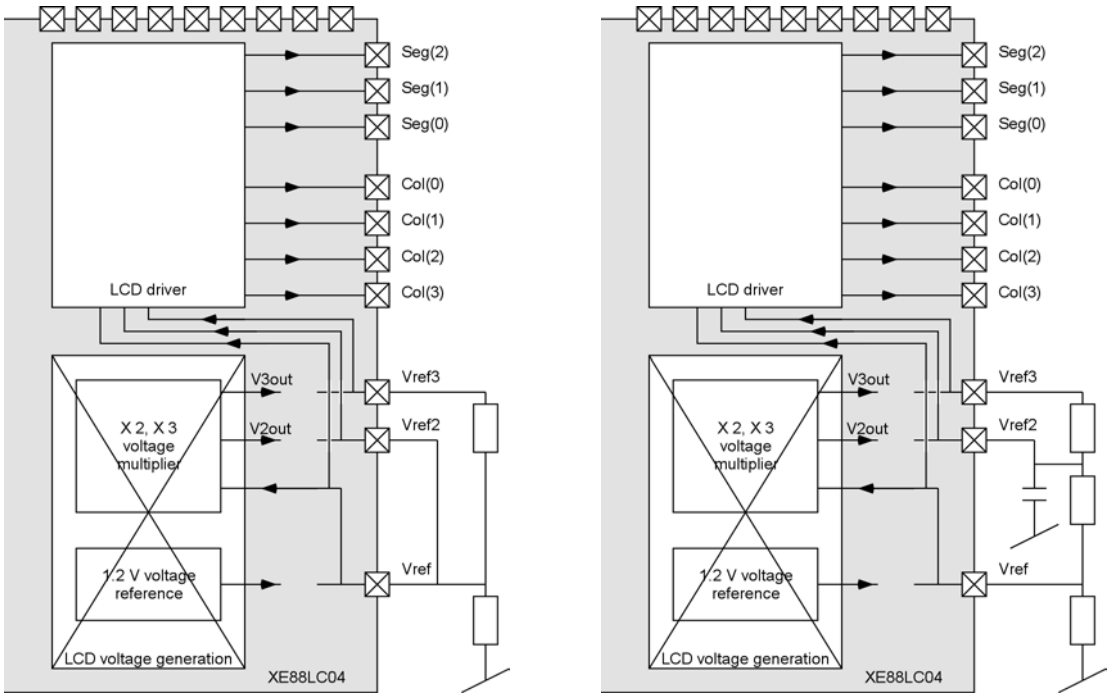

Figure 8.2: Using voltages proportional to Vbat (power supply) for multiplex by two (left) or three or four

9 Physical description

9.1 BGA package

Figure 9.1:

10 Contacting XEMICS

You will find more information about the XE88LC04 and other XEMICS products, as well as the addresses of our representatives and distributors for your region on http://www.xemics.com.