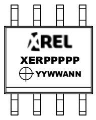
XER2N0525

Extended Temperature 35V P-Channel Power MOSFET

Rev 2 – August 2021 (DS-00988-18)

Data Sheet

PRODUCTION



PSOIC8
XER2N0525

FEATURES

- Minimum BV_{DSS} =-40V.
- Allowed V_{GS} range –5.5V to +5.5V.
- Operational beyond the -60°C to +175°C temperature range.
- Low $R_{DS(on)}$
  - XER2N0525: 2.3 Ω @ 175°C
- Maximum Peak I_D:
  - XER2N0525: 5.3 A @ 175°C
- On-time ($t_{d(on)}$+t_r):
  - XER2N0525: 26 nsec @ 175°C
- Off-time ($t_{d(off)}$+t_f):
  - XER2N0525: 76 nsec @ 175°C
- Plastic SOIC8 package.

APPLICATIONS

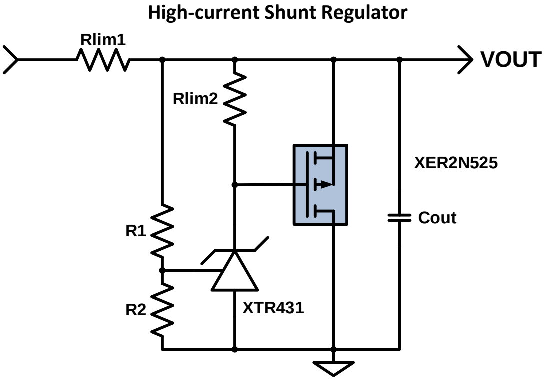
- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- DC/DC converters, point-of-load power converters, switching power supplies, PWM control.

DESCRIPTION

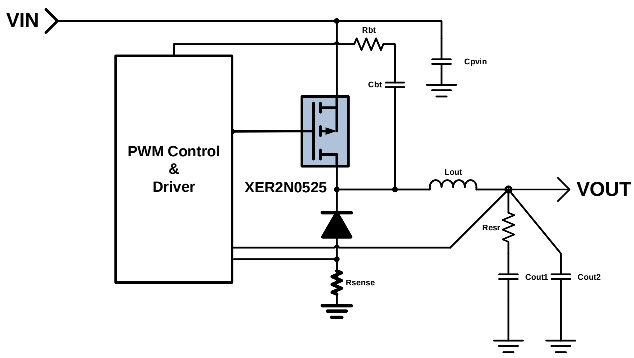
XER2N0525 is a family of 35V P-channel power MOSFETs designed to reliably operate over a wide range of temperatures. Full functionality is guaranteed from -60°C to +175°C, though operation well below and above this temperature range is achieved.
Fabricated in a Silicon-on-Insulator (SOI) process, XER2N0525 family parts offer reduced leakage currents while providing high drain currents and low $R_{DS(on)}$. These features allow XER2N0525 parts to be ideally suited for switching and linear applications.
XER2N0525 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.
Parts from the XER2N0525 family are available in plastic SOIC8 packages.

PRODUCT HIGHLIGHT

High-current Shunt Regulator



DC-DC Converter



ORDERING INFORMATION

X	ER	2N	0525
Source : X = X-REL Semi	Process: ER = Extended Temp, HiRel	Part family	Part number

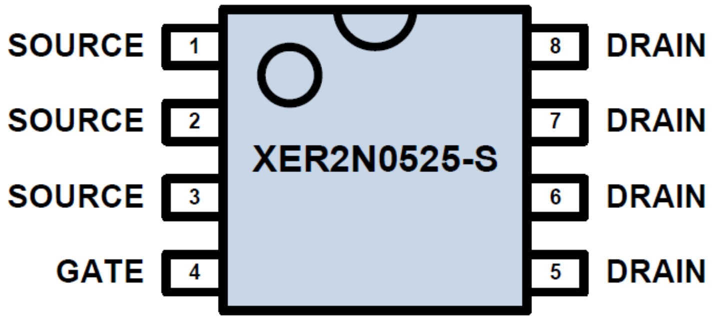
Product Reference	Temperature Range	Package	Pin Count	Marking
XER2N0525-S	-60°C to +175°C	High-Temperature SOIC	8	XER2N0525

ABSOLUTE MAXIMUM RATINGS

Drain-source voltage	--40V to +2V
Gate-source voltage	±6.0V
Storage Temperature Range	-70°C to +175°C
Operating Junction Temperature Range	-70°C to +175°C
ESD Classification	2kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS



RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Drain-source voltage V_{DS}	-35		1.5	V
Gate-source voltage V_{GS}	-5.5		+5.5	V
Junction Temperature[1] T_J	-60		175	°C

[1] *Operation beyond the specified temperature range is achieved. The -60°C to +175°C range for the case temperature is considered for the case where $I_D \leq I_{D(DC)}$ for a given case temperature.*

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for -60°C<Tj<175°C.

Parameter	Condition	Min	Typ	Max	Units
DC Characteristics					
Drain-source breakdown voltage BV_{DSS}	V_{GS}=0V, I_{DS}=-100µA	-40			V
Static drain-source on-state resistance $R_{DS(on)}$	V_{GS}=-5V, I_{DS}=-100mA T_C=-60°C T_C=85°C T_C=175°C		 1.1 1.6 2.3	 1.5 2.1 3.0	□
Continuous drain current $I_{D(DC)}$	V_{GS}=-5V T_J =-60°C T_J =85°C T_J =175°C	 -1.5 -1.1 -0.9	 -2.2 -1.6 -1.3		A
Gate threshold voltage $V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=-1mA T_C=-60°C T_C=85°C T_C=175°		 -1.27 -0.98 -0.60		V
Temperature drift of gate threshold voltage $\Delta V_{GS(TH)}/\Delta T_j$	V_{DS}=V_{GS}, I_{DS}=-1mA		2.31		mV/°C
Off-state drain current I_{DSS}	V_{DS}=-35V, V_{GS}=0V T_C=85°C T_C=175°C		 -0.35 -45	 -10 -200	µA
Gate leakage current I_{GSS}	V_{GS}=±5V, V_{DS}=0V T_C=85°C T_C=175°C		 ±0.6 ±170	 ±5 ±1000	nA
AC Characteristics					
Input capacitance C_{iss}	V_{DS}=-35V, V_{GS}=0V, f=1MHz		160		pF
Output capacitance C_{oss}	V_{DS}=-35V, V_{GS}=0V, f=1MHz		62		pF
Transfer capacitance C_{rss}	V_{DS}=-35V, V_{GS}=0V, f=1MHz		35		pF
Switching Characteristics					
Pulsed drain current I_{DM}	V_{DS}=-20V, $V_{GS\ sweep}$=0 to -5V, d=0.2%, □=1ms T_C=-60°C T_C=85°C T_C=175°C	 -6.1 -4.5 -3.7	 -8.7 -6.4 -5.3		A
Total gate charge Q_g	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V		4.8		nC
Turn-on delay time $t_{d(on)}$	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		9		ns
Rise time t_r	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		17		ns
Turn-off delay time $t_{d(off)}$	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		32		ns
Fall time t_f	V_{DS}=-25V, $V_{GS\ sweep}$=0 to -5V, R_D=47Ω, d=0.2%, □=1ms		44		ns
Drain-Source Diode Characteristics					
Forward diode voltage V_{SD_1A}	V_{GS}=0V, I_{DS}=1A T_C=-60°C T_C=85°C T_C=175°C		 1.34 1.23 1.09		V

XER2N0525 TYPICAL PERFORMANCE

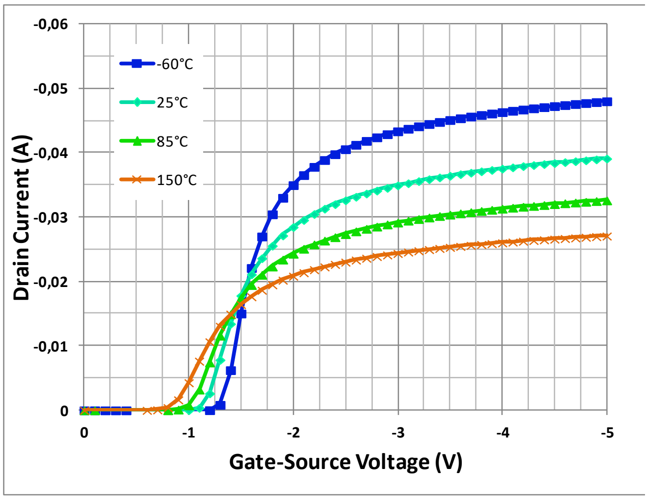


Figure 1. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

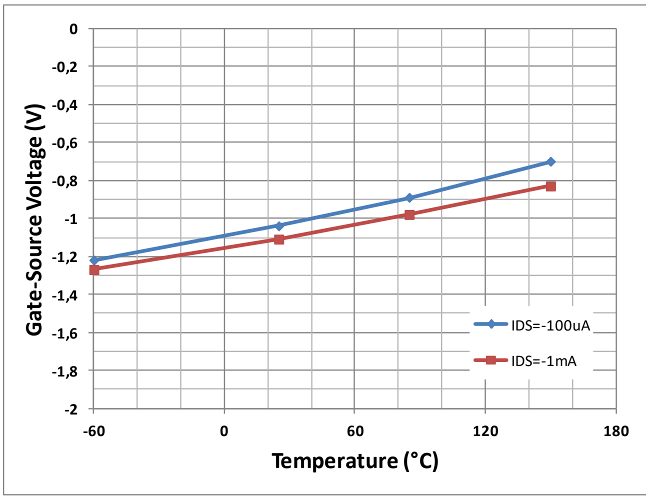


Figure 2. Gate-Source Threshold Voltage ($V_{GS(th)}$) vs Case temperatures. V_{GS}= V_{DS}.

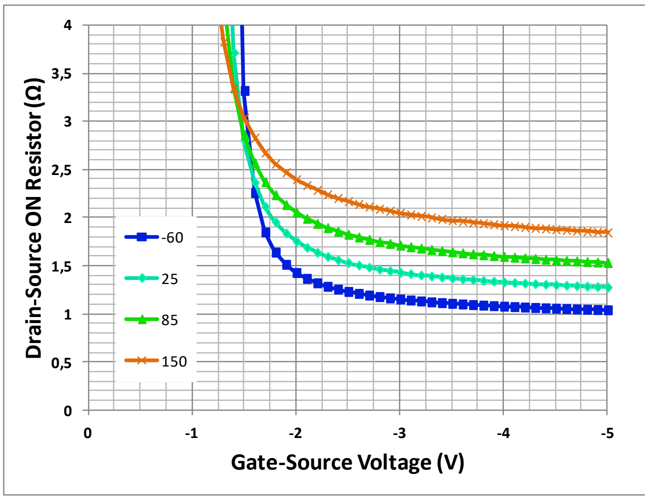


Figure 3. Drain-Source ON Resistance ($R_{DS(on)}$) vs Gate-Source Voltage for several case temperatures. V_{DS}=-50mV.

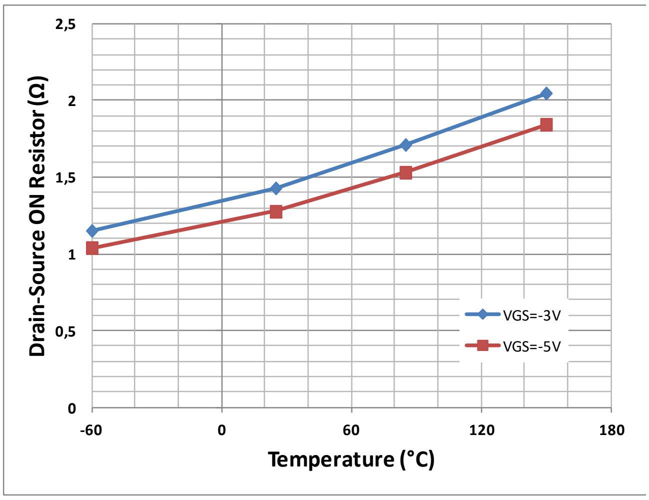


Figure 4. Drain-Source ON Resistance ($R_{DS(on)}$) vs Case Temperature. V_{DS}=-50mV.

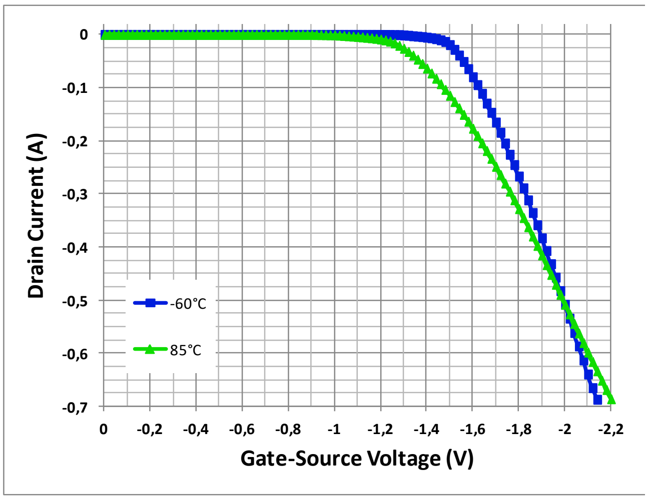


Figure 5. Drain Current (I_{DS}) vs Gate-Source Voltage for several case temperatures. V_{GS}=V_{DS}

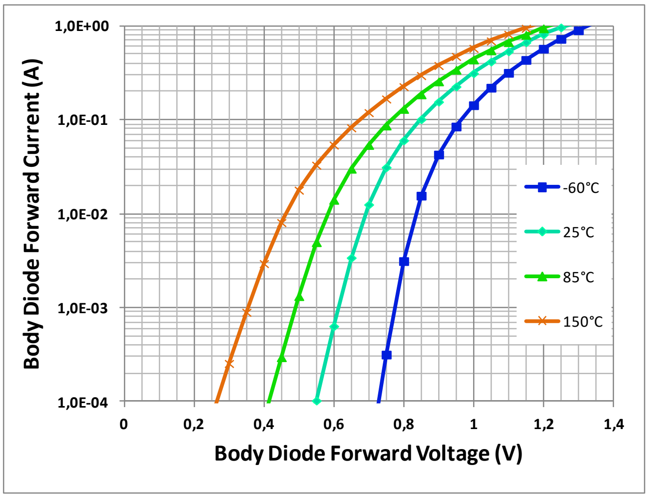


Figure 6. Body Diode Forward Current (I_{FD}) in logarithmic scale vs Forward Voltage for several case temperature. V_{GS}=0V.

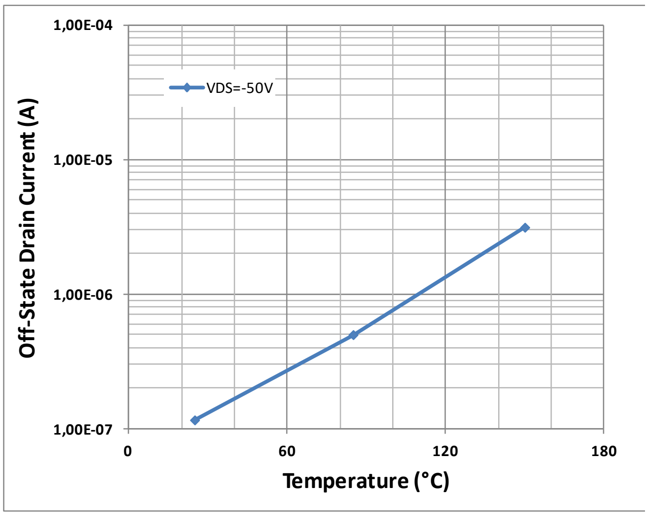


Figure 7. Off-State Drain Current (I_{DSS}) vs Case Temperature. V_{DS}=-50V, V_{GS}=0V.

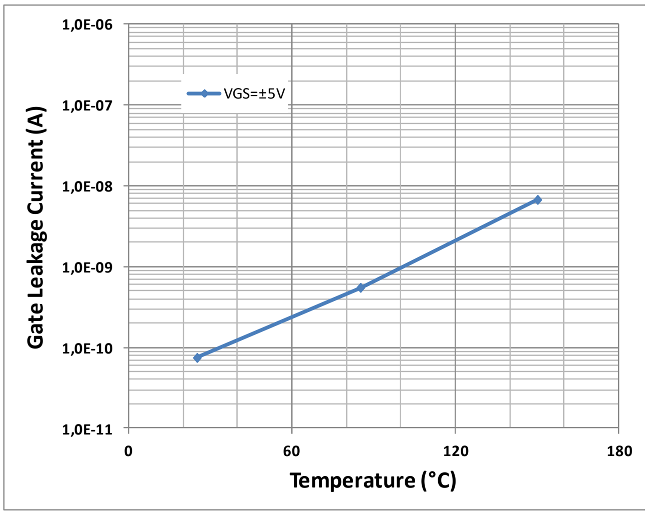


Figure 8. Gate Leakage Current (I_{GSS}) vs Case Temperature. V_{GS}=±5V, V_{DS}=0V.

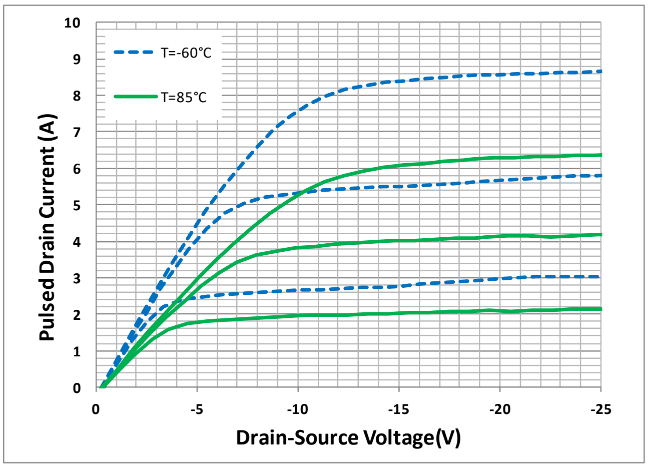


Figure 9. Pulsed Drain Current (I_{DM}) vs Drain-Source Voltage for several case temperatures. V_{GS}=-3V, -4V and -5V.

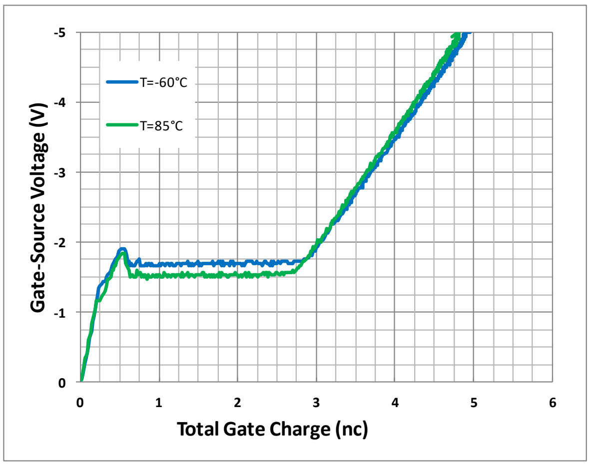


Figure 10. Total Gate Charge (Q_g) vs Gate-Source Voltage for several case temperatures. I_{DS}=-90mA.

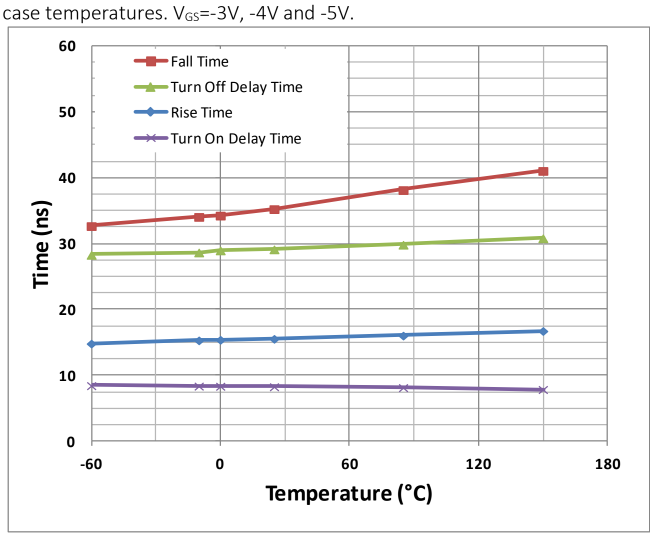


Figure 11. Timing Characteristics vs Case Temperature. V_{DS}=-25V, $V_{GS\ sweep}$= 0 to -5V.

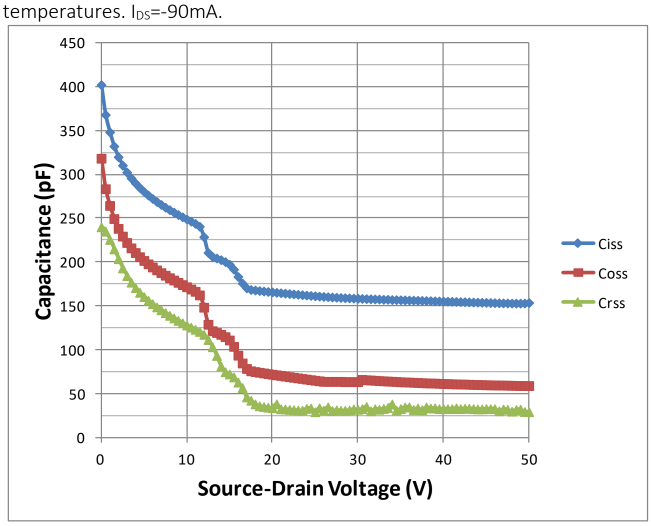


Figure 12. Capacitance vs Source-Drain Voltage at Tc=25°C.

PARAMETER DEFINITION

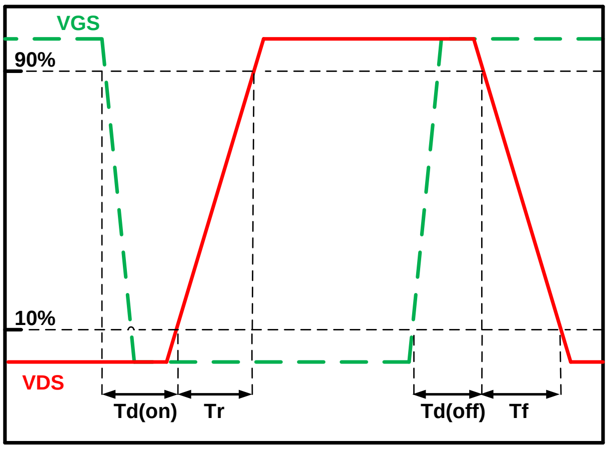
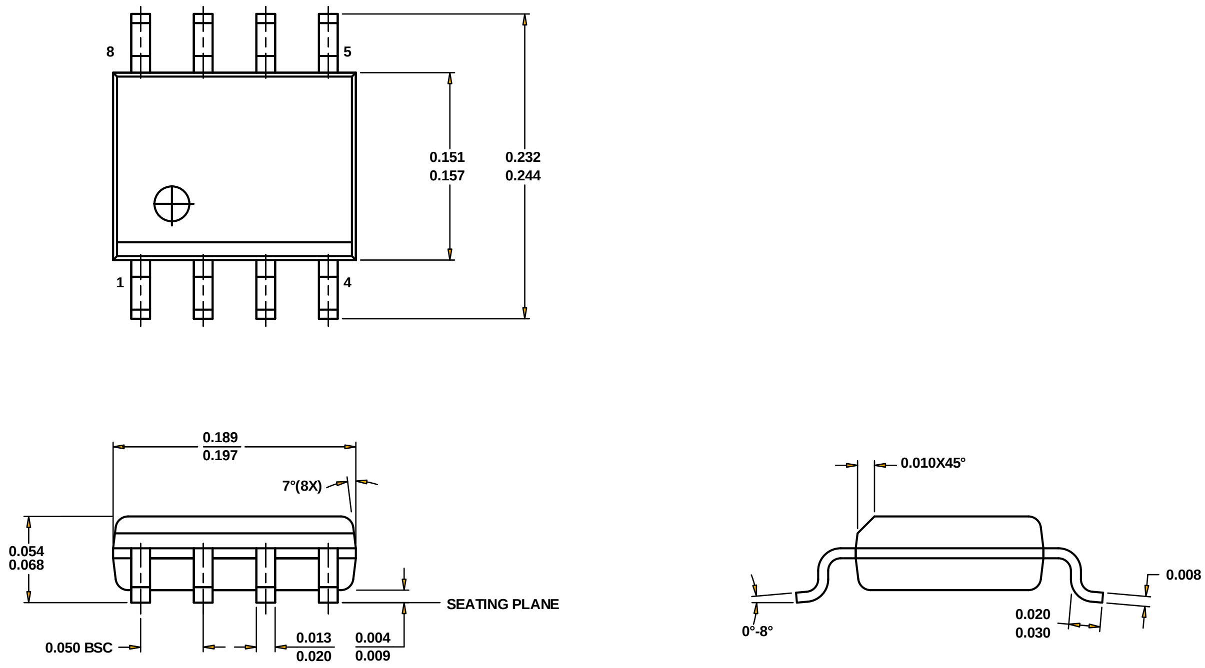


Figure 13. Timing diagram definition.

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise stated.

Plastic SOIC8



FINISHING: PPF

Part Marking Convention	
Part Reference: XERPPPPPP	
XER	X-REL Semiconductor, high-reliability product.
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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