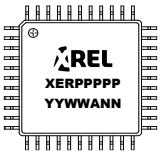
XER30019

Extended Temperature PWM Controllers

Rev 2 – August 2021 (DS-00941-18)

Data Sheet

PROTOTYPE



PQFP44

XER30019

FEATURES

- Supply voltage up to 35V.
- Operational beyond the -50°C to +175°C temperature range.
- Monolithic PWM controller.
- Internal linear regulator with under voltage lockout (ULVO).
- Input voltage feed-forward.
- Selectable asynchronous and pulse-skip modes.
- Selectable output signal polarity: active HIGH or LOW.
- Resistor programmable maximum duty cycle.
- Programmable integrated oscillator with synchronizing capability.
- Resistor-programmable soft-start period.
- Power-good (PGood) flag.
- Programmable over-current protection level.
- Programmable polarity of over-current protection.
- Programmable minimum duty-ratio in pulse-skip mode.
- Voltage tracking capabilities.
- Shut-down mode.
- Interleaved mode for push-pull architectures.
- Forced bootstrap capacitor pre-charge mode.
- Latch-up free.
- Ruggedized SMT
- Also available as bare die.

DESCRIPTION

XER30019 is a family of small footprint PWM controllers designed for extreme reliability and high temperature applications such as DC/DC converters and PWM control. Being able to operate from input voltages as high as 35V, XER30019 PWM controllers can run at frequencies as high as 800kHz, allowing the use of small footprint and low-cost external passive components.

Functionality features include internal oscillator and voltage reference, programmable soft-start, voltage tracking, synchronization capability, over-current protection and power-good flag.

Special design techniques were used to allow the XER30019 parts to offer a precise, robust and reliable operation in critical applications. Full functionality is guaranteed from -50°C to +175°C.

Parts from the XER30019 have all functional features to operate in buck, boost, flyback and push-pull modes.

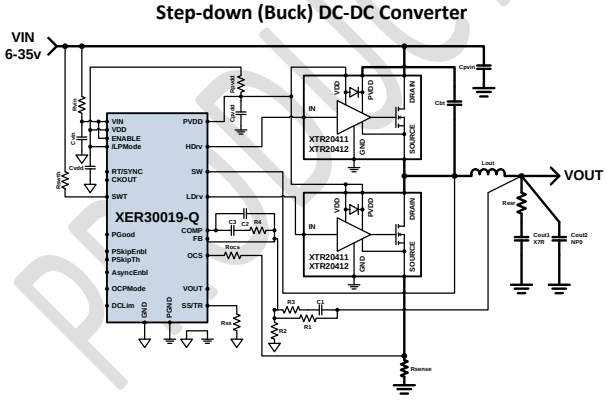
XER30019 parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

APPLICATIONS

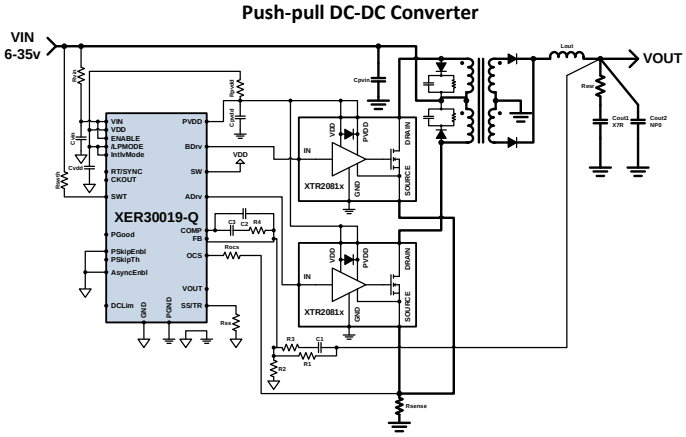
- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- DC/DC converters, point-of-load power converters, switching power supplies, PWM control

PRODUCT HIGHLIGHT

Step-down (Buck) DC-DC Converter



Push-pull DC-DC Converter



ORDERING INFORMATION

X	ER	30	019
Source : X = X-REL Semi	Process: ER = Extended Temp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XER30019-Q	-50°C to +175°C	High-Temperature plastic QFP	44	XER30019

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

AVAILABLE FUNCTIONALITIES

Supported converter architectures for given packaging option

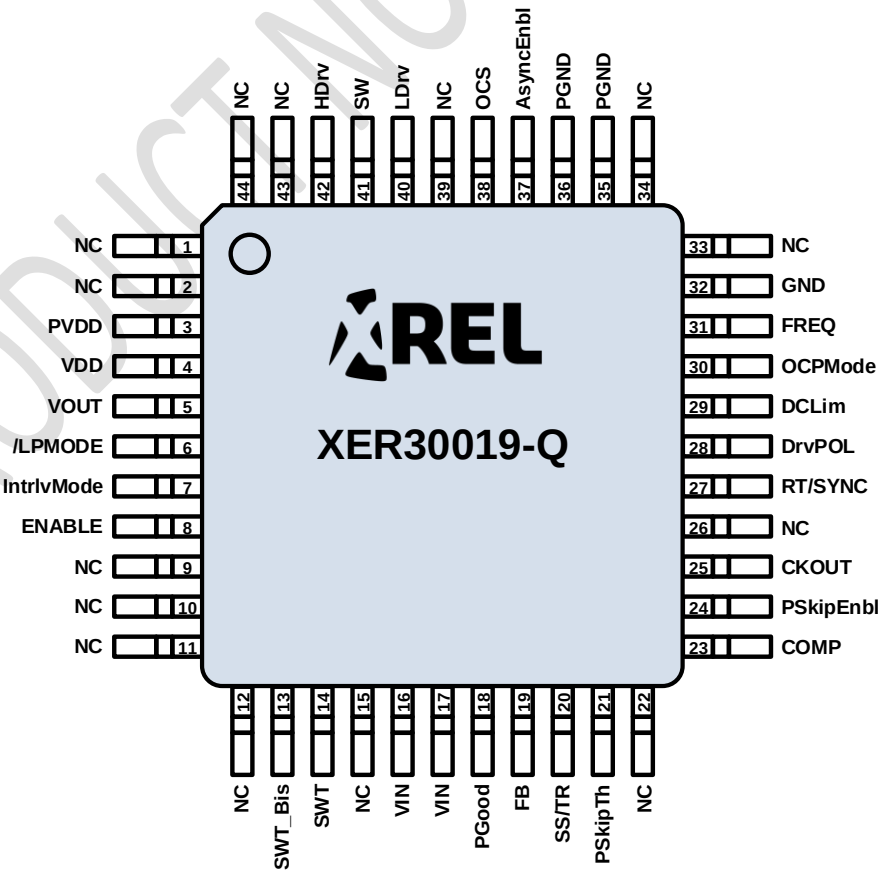
	Pin Count	Buck	Boost	Flyback	Push-pull
XER30019	44	✓	✓	✓	✓

ABSOLUTE MAXIMUM RATINGS

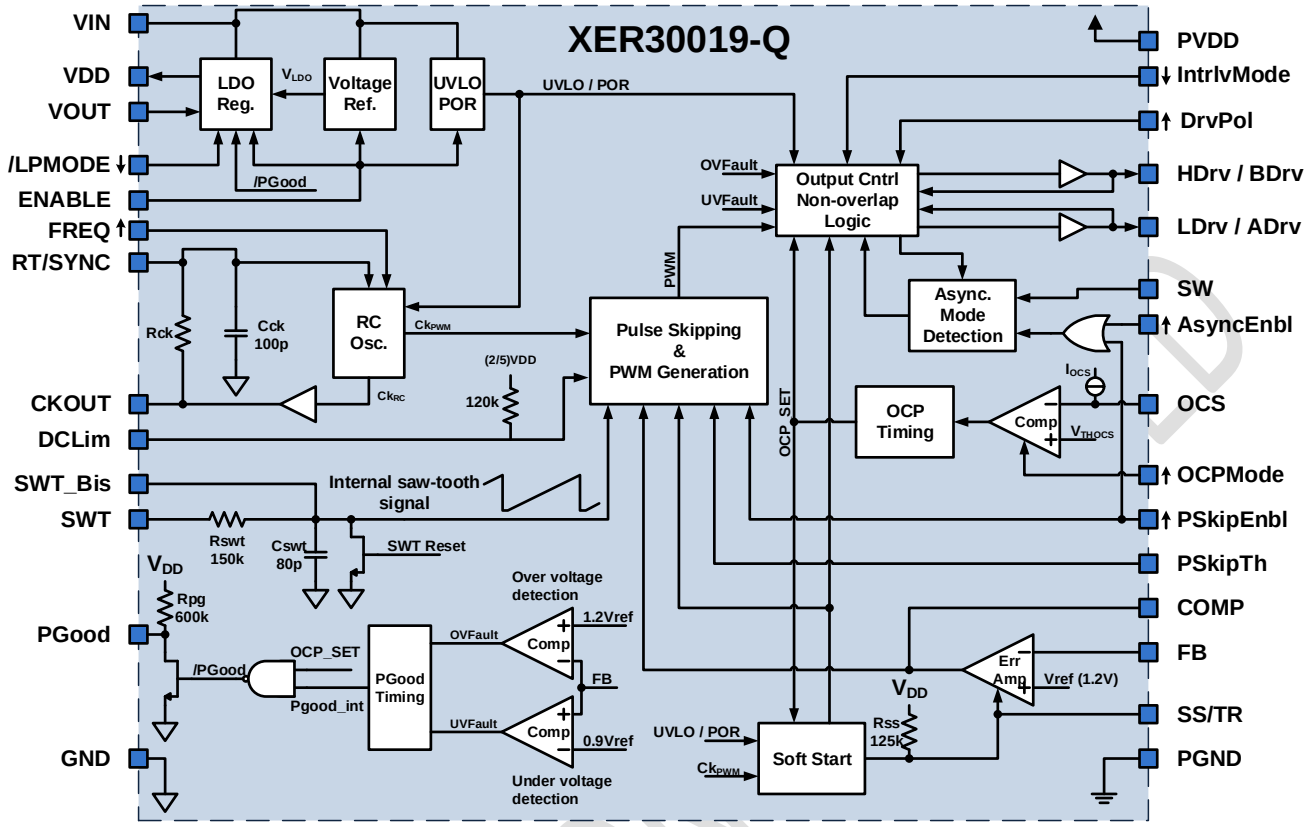
Voltage on VIN, SWT, OCS, SW or ENABLE to ground	-0.5 to 40V
Voltage on any pin to ground	-0.5V to 6.0V
Storage Temperature Range	-70°C to +175°C (tbc)
Operating Junction Temperature Range	-70°C to +175°C (tbc)
ESD Classification	1kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PACKAGING



BLOCK DIAGRAM



Arrows aside pad names indicate whether the input is internally pulled up or down by default.

Die-level block diagram showing all available functionalities and bond-pads.

PIN DESCRIPTION

Name	Description	Pin Number XER30019	
NC		1	
NC		2	
PVDD	Power supply of the output buffers. A minimum capacitor of 0.1µF must be connected from this node to ground.	3	
VDD	Output of the internal linear regulator. This pin supplies the internal circuitry and can supply PVDD if externally connected. A minimum capacitor of 0.1µF must be connected from this node to ground.	4	
VOUT	Auxiliary input to bypass the internal linear regulator in low-power mode whenever an external 5V supply exists. Connect to VDD or leave floating if not used.	5	
/LPMODE	Operation in low-power mode when driven LOW.	6	↓
IntrlvMode	Operation in interleaved mode when driven HIGH.	7	↓
ENABLE	Enables PWM controller operation when driven HIGH. When driven low, the part remains in shutdown mode.	8	
NC		9	
NC		10	
NC		11	
NC		12	
SWT_Bis	Direct access to the saw-tooth slope programming capacitor allowing current mode control. Connect to a positive supply through a current generator or an external resistor.	13	
SWT	Saw-tooth slope programming terminal. Connect to a positive supply directly or through an external resistor. Connection to VIN provides supply feed forward compensation. To connect SWT to VIN, use a minimum 100Ω resistor.	14	
NC		15	
VIN	Supply voltage. A minimum capacitor of 0.1µF must be connected from this node to ground. This pin supplies the internal voltage reference and linear regulator.	16	
VIN	Supply voltage. A minimum capacitor of 0.1µF must be connected from this node to ground. This pin supplies the internal voltage reference and linear regulator.	17	
PGood	Power good flag. Pulled-down when FB is outside a given range or in an overcurrent event and pulled-up to VDD (internal 600k resistor) after soft-start sequence has successfully finished. Pull-up can be reinforced by connecting an external resistor between PGood and VDD.	18	↑
FB	Feedback pin of the control loop. Inverting input of error amplifier.	19	
SS/TR	Soft-start and track input. An external resistor from this node to ground can be used to increase the soft-start period. When driven by an external analog voltage lower than Vref, voltage tracking mode can be used.	20	
PSkipTh	Pulse-skipping threshold. Sets the minimum error amplifier output that makes the controller enter in pulse-skipping mode (PSkipEnbl=1).	21	
NC		22	
COMP	Output of error amplifier. This node should not see any resistive load with a DC path.	23	
PSkipEnbl	Enables operation in pulse-skipping mode when driven HIGH.	24	↑
CKOUT	Output of internal oscillator. It can be used to synchronize cascaded controllers.	25	
NC		26	
RT/SYNC	Sets the switching frequency. When driven by an external square signal, synchronizes the internal oscillator to this signal. Any external parasitic capacitance on this node decreases the nominal frequency.	27	
DrvPOL	Sets the operating polarity of the output drivers. When driven HIGH, HDrv is HIGH when active. When driven LOW, HDrv is LOW when active.	28	↑
DCLim	PWM duty-cycle limiting function. It fixes the upper limit of the error amplifier output "COMP". If COMP exceeds this limit, the input of the error amplifier will be internally clamped to the voltage present on DCLIM. Clamping level can be adjusted with an external resistor to GND. Internally set to 2/5 of VDD across a 100k resistor. Leave it floating for default mode or connect to VDD to disable its functionality.	29	
OCPMode	Sets the polarity of the over-current protection threshold. Negative when driven HIGH (buck) and positive when driven LOW (boost, flyback, push-pull).	30	↑
FREQ	Sets the operating frequency range of the internal oscillator. FREQ=0 => lower range; FREQ=1 => upper range. Only available at bare die level or in packaging upon request.	31	↑
GND	Ground.	32	
NC		33	
NC		34	
PGND	Power ground used by the output drivers. Set to same potential than GND through a star-like connection of the respective planes.	35	
PGND	Power ground used by the output drivers. Set to same potential than GND through a star-like connection of the respective planes.	36	
AsyncEnbl	When OCPMode=1, AsyncEnbl allows operation in asynchronous mode when driven HIGH. When driven LOW, the controller operates only in synchronous mode except if pulse-skipping mode is active. AsyncEnbl also interacts with OCPMode in order to control activity of LDrv. Read a more detailed description of the functionality of this pin in the "Internal Blocks and Functional Features" section of this datasheet.	37	↑
OCS	Sensing input of the over-current protection, referred to PGND. Parasitic capacitance between this node and noisy nodes must be minimized at PCB level. In buck (step-down) mode (OCPMode=1), connect OCS to VDD if not used. In boost, flyback, push-pull modes (OCPMode=0), connect OCS to GND if not used.	38	
NC		39	
LDrv / ADrv	Output for the synchronous rectifier transistor driver. In interleaved mode, ADrv is the output having the first activity.	40	
SW	Feedback from switching node for operation in asynchronous mode, if enabled. It is also used for current sense sampling in buck mode (OCPMode=1). Connect to VIN or VDD or keep floating if not used. Read a more detailed description of the functionality of this pin in the "Internal Blocks and Functional Features" section of this datasheet.	41	
HDrv / BDrv	Output for the main switch transistor driver. In interleaved mode, BDrv is the output having the second activity.	42	
NC		43	
NC		44	

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **V_{IN}**	6[1]		35	V
Voltage on SWT, ENABLE, SW[2], OCS[2]	0		V_{IN}	V
Voltage on digital inputs to GND. /LPMODE, PSkipEnbl, AsyncEnbl, IntrlMode, OCPMode, DrvPOL, FREQ	0		V_{DD}	V
Voltage on VOUT input to GND.	4.5	5	5.5	V
Voltage on DCLim	0.5		2[3] (internally set)	V
Voltage on PSkipTh[4]	0.2 (internally set)		DCLim - 0.3	V
Operating Frequency **F_O** **FREQ=1** **FREQ=0**	50[5]	520 180	1000[5]	kHz
Case Temperature[6] **T_C**	-50		175	°C

[1] Operation with input voltage 5V possible with bypassing of the internal linear regulator (VIN shorted to VDD).
[2] During transient operation, SW and OCS can reach values under 0V and above VIN. Extreme values are limited by internal clamping diodes to GND and to VIN.
[3] Theoretically, DCLim can be set to any voltage from 0.5V (internal threshold) to VDD. DCLim above 2V has no effect on the maximum duty cycle limitation. The default threshold if DCLim leave floating is 2/5VDD. DClim can be connected to VDD to deactivate its functionality (deactivation of the volt-second clamp).
[4] PSkipTh must be at least 300mV below DCLim. PSkipTh has an internally set value of 200mV.
[5] The frequency of the internal clock generator can be changed by the external addition of a capacitors or a resistor.
[6] The -50°C to +175°C range for the case temperature is considered for the case where no current is externally drawn from pin VDD, other than to supply the XER30019-Q part.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for VIN=6V to 35V, VDD=5V, -50°C<Tc<175°C.

Parameter	Condition	Min	Typ	Max	Units
Reference Voltage					
Internal Feedback Reference Voltage **V_{ref}**	V_{IN}=10V, T_c=25°C.	1.186	1.210	1.234	V
Drift with Temperature **$(\Delta V_{REF}/V_{REF})/\Delta T$**	V_{IN}=10V, ΔT from -50°C to +175°C $\Delta V_{REF}=V_{REF\_Max}(\Delta T)-V_{REF\_min}(\Delta T)$	20	60	100	ppm/°C
Line regulation **ΔV_{REF}**	V_{IN} sweep (ΔV_{IN}) from 6V to 35V $\Delta V_{REF}=V_{REF\_Max}(\Delta V_{IN})-V_{REF\_min}(\Delta V_{IN})$ T_c=25°C T_c=175°C		 6.7 10.7	 13 17	mV
Supply Current					
Stand-by Supply Current **I_{VINSB}**	ENABLE=0V. VIN=35V (worst case) T_c=25°C T_c=175°C		 25 52	 40 70	µA
Dynamic Supply Current **I_{VIND}**	F_O=520kHz. C_{load}=50pF on HDrv and LDrv, synchronous mode. T_c=175°C and VIN=35V (worst case)		2.7	3.2	mA
Supply Current Low-Power Mode **I_{VINLP}**	V_{DD}=4V (/LPMODE=0), F_O=520kHz. C_{load}=50pF on HDrv and LDrv, synchronous mode, VIN=35V (worst case).		2.3	2.8	mA
Supply Current Low-Power Mode with External Supply **I_{VINES}**	5V supplied by external source through pin V_{OUT} and /LPMODE=0, F_O=520kHz. C_{load}=50pF on HDrv and LDrv, synchronous mode, VIN=35V (worst case).		0.58	0.75	mA

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for VIN=6V to 35V, VDD=5V, -50°C<Tc<175°C.

Parameter	Condition	Min	Typ	Max	Units
Voltage Regulator					
Output Voltage **V_{DD}**	V_{IN}=10V, I_{LOAD}=1mA, T_c=25°C /LPMODE=0 (default) [1] /LPMODE=1	 3.9 4.875	 4 5	 4.1 5.125	V
Drift with Temperature **$(\Delta V_{DD}/V_{DD})/\Delta T$**	V_{IN}=10V, I_{LOAD}=1mA $\Delta V_{DD}=V_{DD\_Max}(\Delta T)-V_{DD\_min}(\Delta T)$	20	60	100	ppm/°C
Line regulation **$\Delta V_{DD}/V_{DD}$**	V_{IN} sweep (ΔV) from 6V to 35V, V_{DD}=4V or 5V, I_{LOAD}=1mA, T_c=175°C (worst case).		0.73	1.30	%
Load regulation **$\Delta V_{DD}/\Delta I_{VDD}$**	V_{IN}=10V, I_{LOAD}=1mA to 20mA T_c=-50°C T_c=175°C	 -1.8 -3.5	 -1.3 -2.6		mV/mA
Maximum Output Current **I_{VDDMAX}**	V_{IN}=10V, V_{DD}=5V (/LPMODE=1). See Figure 7. T_c=25°C T_c=175°C	 35 20	 45 25		mA
	V_{IN}=10V, V_{DD}=4V (/LPMODE=0). See Figure 8. T_c=25°C T_c=175°C	 40 25	 55 35		mA
PWM Enable Voltage **V_{ENON}**	ENABLE going up. Worst case at T_c=-50°C		1.8	2.2	V
PWM Disable Voltage **V_{ENOFF}**	ENABLE going down. Worst case at T_c=175°C	0.6	0.9		V
ENABLE Hysteresis[2] **V_{ENH}**	ENABLE going up then down	0.2	0.4		V
ENABLE Current **I_{EN}**	V_{EN}=0V V_{EN}=5V	-6 -5		0 1	µA
Load Capacitance[2,3] **C_{VDD}**	Allowed value.	0.3	1	10	µF
Under Voltage Lockout					
V_{DD} Start Voltage **V_{UVLOR}**	VIN going up.	3.8	4	4.2	V
V_{DD} Stop Voltage **V_{UVLOF}**	VIN going down.	3.4	3.7	3.9	V
V_{DD} Start-stop Hysteresis[2] **V_{UVLOH}**	VIN going up then down.	0.25	0.40	0.55	V
Soft Start / Tracking					
Equivalent Resistance[2] **R_{SS}**	T_c=-50°C T_c=25°C T_c=175°C	 	145 113 96	 	kΩ
Tracking Voltage Range[4] **$V_{SS/TR}$**	$V_{SS/TR}$ must remain below the internal Vref (1.2V).	0.25		1.0	V
Tracking Offset on FB[2]Erreur ! Signet non défini. **$V_{FB-SS} = V_{FB} – V_{SS/TR}$**	$V_{SS/TR}$=0.5V T_c=-50°C T_c=175°C	 -20 -60	 -30 -75	 -40 -90	mV
Oscillator					
Free Running Frequency **F_O**	T_c=25°C. No capacitor connected to RT/SYNC. FREQ=1 FREQ=0	 450 140	 510 175	 570 210	kHz
Oscillator accuracy	Oscillator running from internal components.		±6		%
Adjustable Range[2]	With external components.	50		1000	kHz
Recommended Duty Cycles of External Clock	F=520kHz	15		85	%
Minimum Achievable Off-time[2] **t_{Off_Min}**	V_{DD}=5V (/LPMODE=1). T_c=-50°C T_c=175°C	 	 220 160	 	ns
	V_{DD}=4V (/LPMODE=0). T_c=-50°C T_c=175°C	 	 240 180	 	ns
CKOUT Output Strength[2] **I_{CKOUT}**	V_{DD}=5V (/LPMODE=1), T_c=175°C		4		mA

[1] XER30019 parts start-up with V_{DD}=5V even if low-power mode is enabled (/LPMODE=0 or floating). Transition from V_{DD}=5V to V_{DD}=4V occurs when PGood is asserted.

[2] Guaranteed by design and characterization data only. Not tested in production.

[3] VDD must be externally connected to PVDD. The actual load capacitance is the total capacitance connected to VDD and PVDD.

[4] In tracking mode the PWM controller operates in asynchronous mode, except if interleaved mode is active (IntrlvMode=1).

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for V_{IN}=6V to 35V, V_{DD}=5V, -50°C<T_c<175°C.

Parameter	Condition	Min	Typ	Max	Units
Saw-tooth Slope Generator					
Internal Saw-tooth Resistor[5] **R_{SWT}**			150		kΩ
Internal Saw-tooth Capacitor[5] **C_{SWT}**			80		pF
Allowed saw-tooth voltages **V_{SWT}**		4V		V_{IN}	
Allowed current through SWT_Bis terminal[2]			200		µA
Pulse-skipping					
PSkipTh Pull-up Current[3] **I_{PSTh}**	T_c=-50°C T_c=175°C		11.5 13.1		µA
PSkipTh Internal Resistance to GND[3] **R_{PSTh}**		17	20	23	kΩ
Recommended Range on PSkipTh Terminal[4] **V_{PSTh}**		0.2		1	V
Internal PSkipTh Offset[5,6] **V_{PSOff}**		50	160	250	mV
Minimum Recommended On-time **t_{ONPS}**	PSkipEnbl=1.		50		ns
Duty-cycle limit (DCLim)					
Internal DCLim Resistance to VDD[5] **R_{DCLim}**	T_c=-50°C T_c=175°C	130 81	145 90	160 99	kΩ
Internal DCLim Threshold **V_{DCLim}**	Default value when left floating. Recommended operational range using an external resistor to ground.	-2% 0.5[7]	0.4VDD	+2% 0.4VDD[8]	V
Overcurrent Protection					
OCS Current **I_{OCS}**	V_{DD}=5V (/LPMODE=1). T_c=-50°C T_c=25°C T_c=175°C		 37 48 56		µA
	V_{DD}=4V (/LPMODE=0). T_c=-50°C T_c=25°C T_c=175°C		 30 39 45		µA
OCS Threshold Voltage **V_{THOCS}**	V_{DD}=5V (/LPMODE=1). OCPMode = HIGH (Buck) OCPMode = LOW (Boost, Flyback, Push-pull)		 15 370		mV
	V_{DD}=4V (/LPMODE=0). OCPMode = HIGH (Buck) OCPMode = LOW (Boost, Flyback, Push-pull)		 15 290		mV

[2] The reason for this current limit is to guarantee that the SWT_Bis node is completely discharged at the end of the saw-tooth signal.
[3] In production, only the voltage on PSkipTh (product R_{PSTh} x I_{PSTh}) is verified.
[4] It shall always be lower than the voltage on DCLim by at least 300mV. Note that internally, V_{PSOff} (150mV approx.) is removed from this voltage before comparison with the saw-tooth. The crossing defines the minimum t_{on} in pulse skipping mode.
[5] Guaranteed by design and characterization data only. Not tested in production.
[6] The internal effective voltage for pulse skipping operation is the voltage on the PSkipTh terminal minus V_{PSOff}.
[7] It shall always be higher than the voltage on PSkipTh pin by at least 300mV.
[8] DCLim can be connected to VDD in order to inhibit this functionality.

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for V_{IN}=6V to 35V, V_{DD}=5V, -50°C<T_c<175°C.

Parameter	Condition	Min	Typ	Max	Units
Error Amplifier					
Input Bias Current[2] **I_B**	T_c=175°C, V_{IN}=35V (worst case).		50	150	nA
Sinking Output Current[2] **I_{OSnk}**	T_c=-50°C T_c=25°C T_c=175°C		65 115 170		µA
Sourcing Output Current[2] **I_{OSrc}**	V_{IN}=6V (worst case) T_c=-50°C T_c=25°C T_c=175°C		 25 19 14		mA
DC Gain[1,2] **A_O**	R_L=∞		105		dB
Gain Bandwidth Product[2] **GBW**	C_L=90pF	1.1	2		MHz
Digital Inputs (/LPMODE, PSkipEnbl, AsyncEnbl, DrvPOL, IntrlMode, OCPMode)					
HIGH Level Input Voltage **V_{T+}**	V_{DD}=5V (/LPMODE=1). V_{DD}=4V (/LPMODE=0).	2.6 2.1	3.1 2.5	3.6 3.0	V
LOW Level Input Voltage **V_{T-}**	V_{DD}=5V (/LPMODE=1). V_{DD}=4V (/LPMODE=0).	1.3 0.9	1.9 1.4	2.5 1.9	V
Hysteresis Voltage (V_{T+}-V_{T-})[2] **V_{Hys}**	V_{DD}=5V (/LPMODE=1). V_{DD}=4V (/LPMODE=0).	0.7	1.1	1.5	V
Pull-down Strength[2] **I_{PD}**	Pulled-down inputs forced to VDD. V_{DD}=5V. T_c=-50°C T_c=175°C		 60 23	 90 45	µA
Pull-up Strength[2] **I_{PU}**	Pulled-up inputs forced to GND. V_{DD}=5V. T_c=-50°C T_c=175°C		 -75 -36	 -100 -55	µA
Output Drivers					
Pull-up Output Resistance[2] **R_{ONH}**	Output sourcing 10mA. Worst case for V_{IN}=35V and T_c=175°C. See Figure 16. V_{DD}=5V (/LPMODE=1).		78	95	Ω
	Output sourcing 10mA. Worst case for V_{IN}=35V and T_c=175°C. See Figure 15. V_{DD}=4V (/LPMODE=0).		83	100	Ω
Pull-down Output Resistance[2] **R_{ONL}**	Output sinking 10mA. V_{IN}=6V to 35V, T_c=175°C (worst case). See Figure 18. V_{DD}=5V (/LPMODE=1).		29	45	Ω
	Output sinking 10mA. V_{IN}=6V to 35V, T_c=175°C (worst case). See Figure 17. V_{DD}=5V (/LPMODE=1).		33	50	Ω
Peak Sinking Output Current[2] **I_{pDrv_sink}**	V_{DD}=5V (/LPMODE=1). T_c=175°C (worst case). See Figure 20.	35	45		mA
	V_{DD}=4V (/LPMODE=0). T_c=175°C (worst case). See Figure 19.	25	35		mA
Peak Sourcing Output Current[2] **I_{pDrv_source}**	V_{DD}=5V (/LPMODE=1). Worst case for V_{IN}=35V and T_c=175°C. See Figure 22.	35	45		mA
	V_{DD}=4V (/LPMODE=0). Worst case for V_{IN}=35V and T_c=175°C. See Figure 21.	25	35		mA
Non-overlap Time[2,3] **t_{no}**	Time from HDrv / LDrv going down to LDrv / HDrv going up. V_{DD}=5V (/LPMODE=1). T_c=-50°C T_c=175°C	 30 45	 40 60	 60 90	ns
	Time from HDrv / LDrv going down to LDrv / HDrv going up. V_{DD}=4V (/LPMODE=0). T_c=-50°C T_c=175°C	 35 55	 50 75	 75 110	ns

[1] The error amplifier is of type Miller OTA. Avoid connecting any resistive load with a DC path.

[2] Guaranteed by design and characterization data only. Not tested in production.

[3] External drivers must have on-off and off-on delays mismatch lower than t_{no} to avoid any shoot-through on the output transistors.

TYPICAL PERFORMANCE

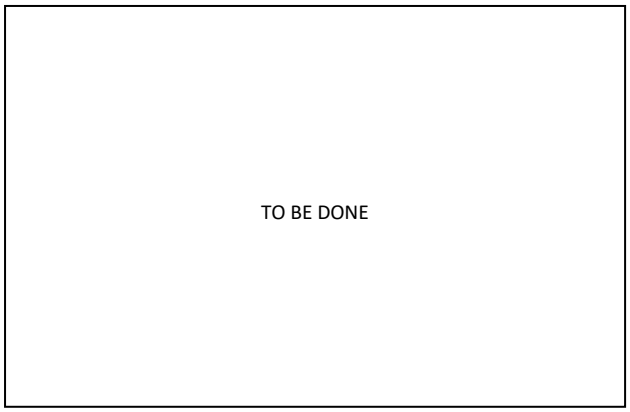


Figure 1. Reference voltage vs temperature for different input voltages (V_{IN}).

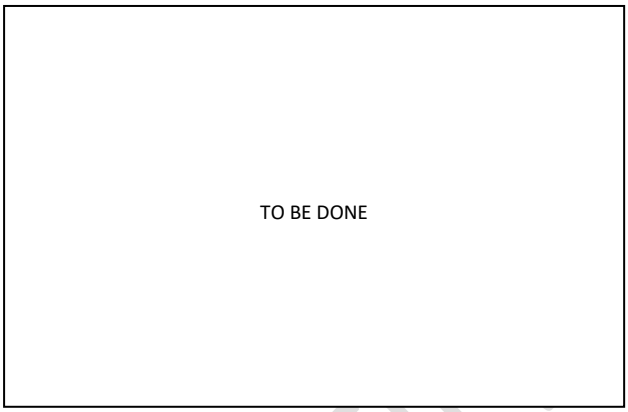


Figure 2. Reference voltage vs input voltage (V_{IN}) for different temperatures.

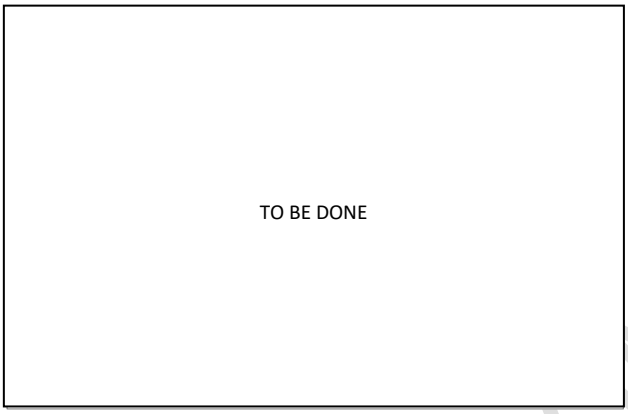


Figure 3. Current through VIN vs input voltage (V_{IN}) for different case temperatures.
Synchronous mode (PSkipEnbl=AsyncEnbl=0), V_{DD}=5V (/LPMODE=1), Freq=520kHz, load capacitance on HDrv and LDrv 200pF.

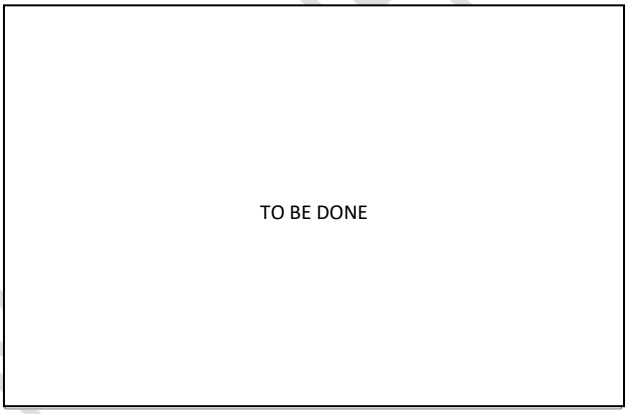


Figure 4. Current through VIN vs input voltage (V_{IN}) for different case temperatures.
Asynchronous mode (AsyncEnbl=1) without pulse slipping (PSkipEnbl=0), V_{DD}=5V (/LPMODE=1), Freq=520kHz, load capacitance on HDrv and LDrv 200pF.

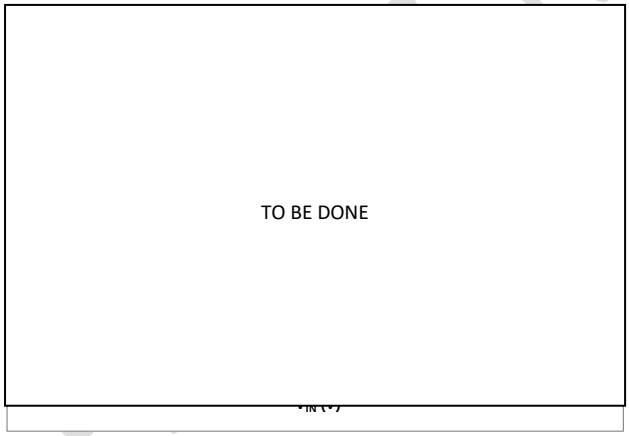


Figure 5. Current through VIN vs input voltage (V_{IN}) for different case temperatures.
Synchronous mode (PSkipEnbl=AsyncEnbl=0), V_{DD}=4V (/LPMODE=0), Freq=510kHz, load capacitance on HDrv and LDrv 200pF.

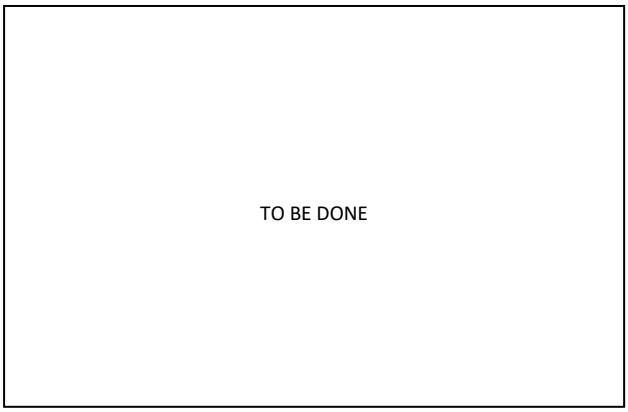


Figure 6. Current through VIN vs input voltage (V_{IN}) for different case temperatures with V_{DD}=5V supplied by external source through pin VOUT.
Synchronous mode (PSkipEnbl=AsyncEnbl=0), /LPMODE=0, Freq=520kHz, load capacitance on HDrv and LDrv 200pF.

TYPICAL PERFORMANCE (CONTINUED)

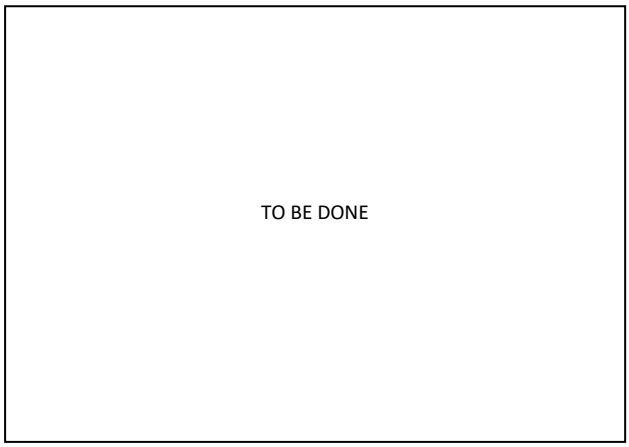


Figure 7. Maximum available output current from VDD vs input voltage (V_{IN}) for several temperatures. V_{DD}=5V (/LPMODE=1).

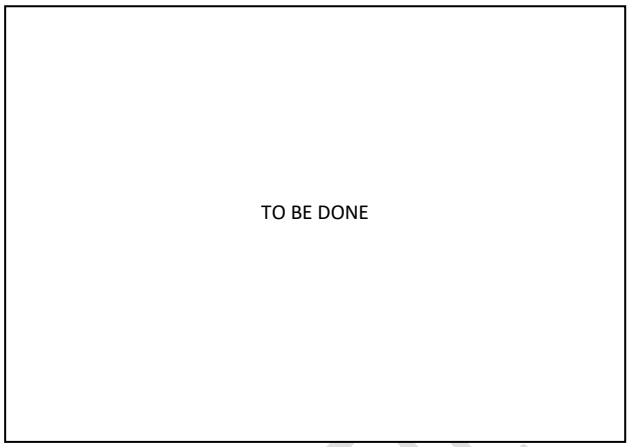


Figure 8. Maximum available output current from VDD vs input voltage (V_{IN}) for several temperatures. V_{DD}=4V (/LPMODE=0).

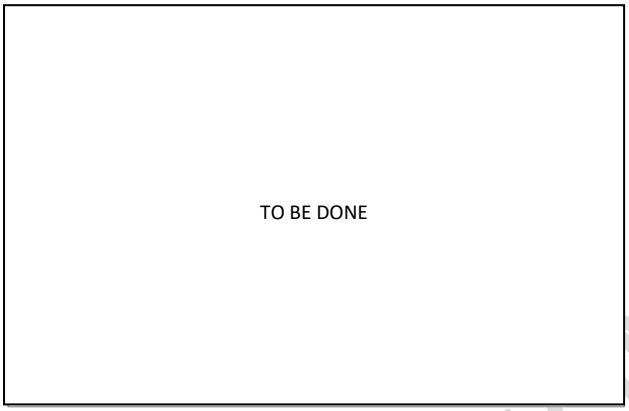


Figure 9. Free running frequency vs input voltage (V_{IN}) for different case temperatures. V_{DD}=5V (/LPMODE=1 and FREQ=1).

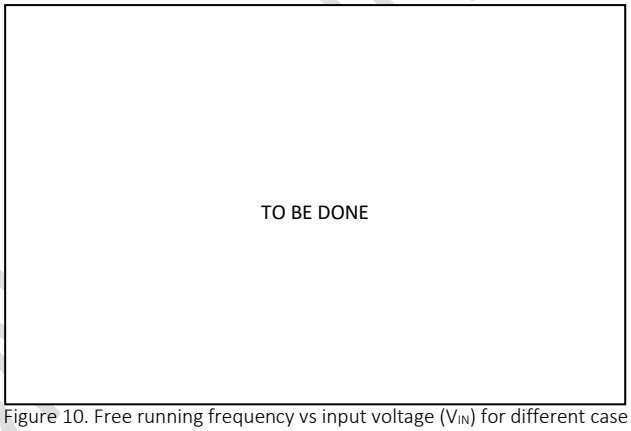


Figure 10. Free running frequency vs input voltage (V_{IN}) for different case temperatures. V_{DD}=4V (/LPMODE=0 and FREQ=1).

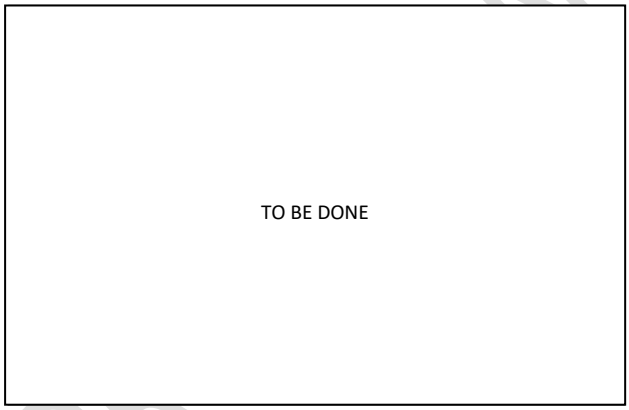


Figure 11. Free running frequency vs input voltage (V_{IN}) for different case temperatures. V_{DD}=5V (/LPMODE=1 and FREQ=0).

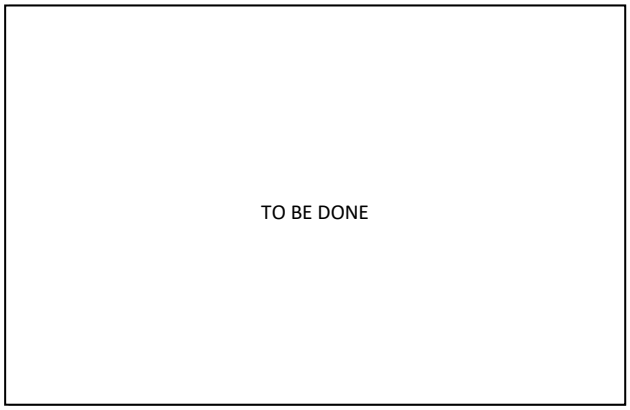


Figure 12. Free running frequency of parts vs input voltage (V_{IN}) for different case temperatures. V_{DD}=4V (/LPMODE=0 and FREQ=0).

TYPICAL PERFORMANCE (CONTINUED)

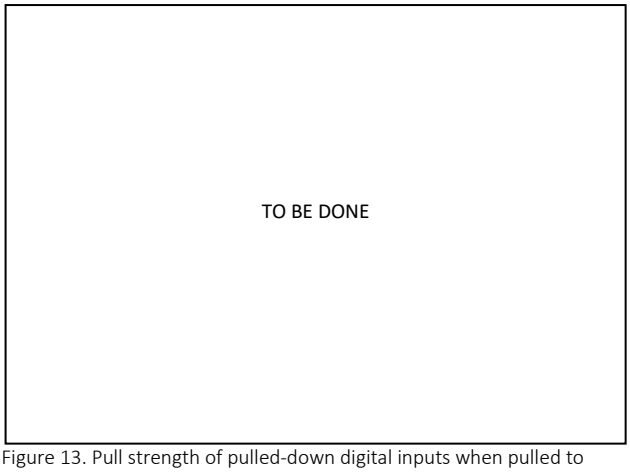


Figure 13. Pull strength of pulled-down digital inputs when pulled to VDD vs temperature. V_{IN}=6V and 35V, V_{DD}=5V.

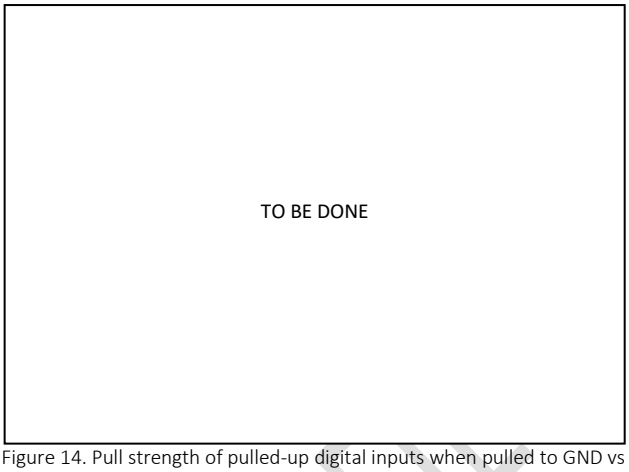


Figure 14. Pull strength of pulled-up digital inputs when pulled to GND vs temperature. V_{IN}=6V and 35V, V_{DD}=5V.

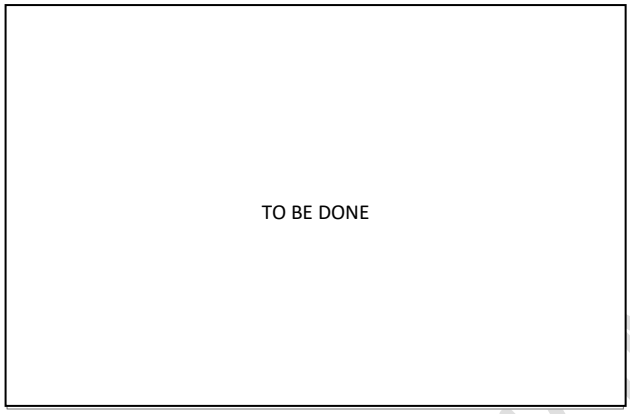


Figure 15. High-state on-resistance of output drivers vs input voltage (V_{IN}) for different case temperatures. Device sourcing 10mA, V_{DD}=4V (/LPMODE=0).

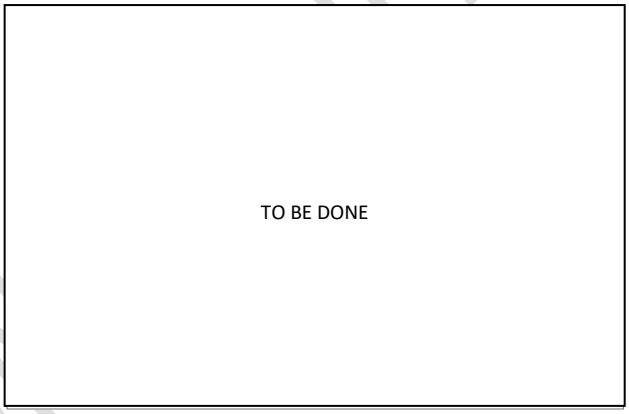


Figure 16. High-state on-resistance of output drivers vs input voltage (V_{IN}) for different case temperatures. Device sourcing 10mA, V_{DD}=5V (/LPMODE=1).

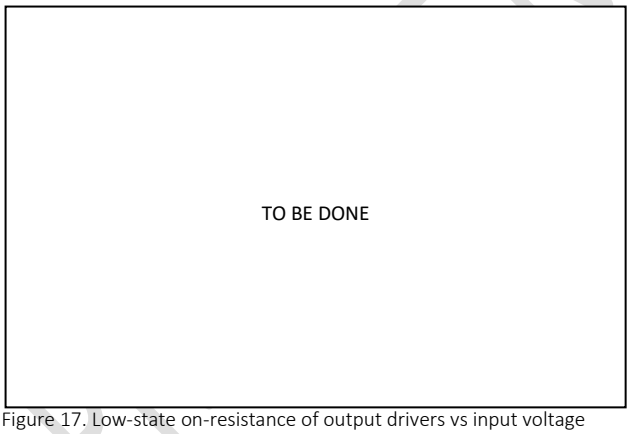


Figure 17. Low-state on-resistance of output drivers vs input voltage (V_{IN}) for different case temperatures. Device sinking 10mA, V_{DD}=4V (/LPMODE=0).

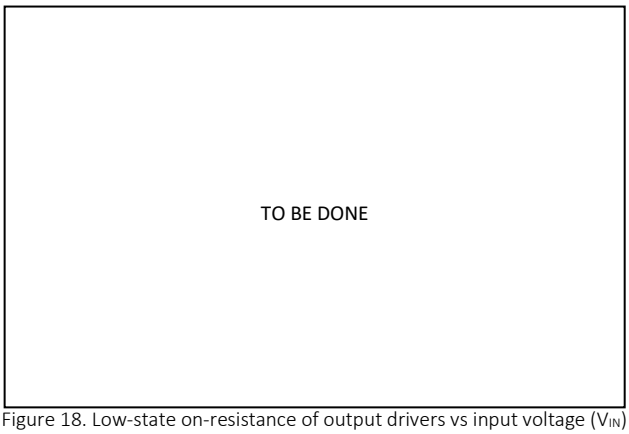


Figure 18. Low-state on-resistance of output drivers vs input voltage (V_{IN}) for different case temperatures. Device sinking 10mA, V_{DD}=5V (/LPMODE=1).

TO BE DONE

Figure 19. Peak sinking current capability of output drivers vs input voltage (V_{IN}) for different case temperatures. V_{DD}=4V (/LPMODE=0).

TO BE DONE

Figure 20. Peak sinking current capability of output drivers vs input voltage (V_{IN}) for different case temperatures. V_{DD}=5V (/LPMODE=1).

TO BE DONE

Figure 21. Peak sourcing current capability of output drivers vs input voltage (V_{IN}) for different case temperatures. V_{DD}=4V (/LPMODE=0).

TO BE DONE

Figure 22. Peak sourcing current capability of output drivers vs input voltage (V_{IN}) for different case temperatures. V_{DD}=5V (/LPMODE=1).

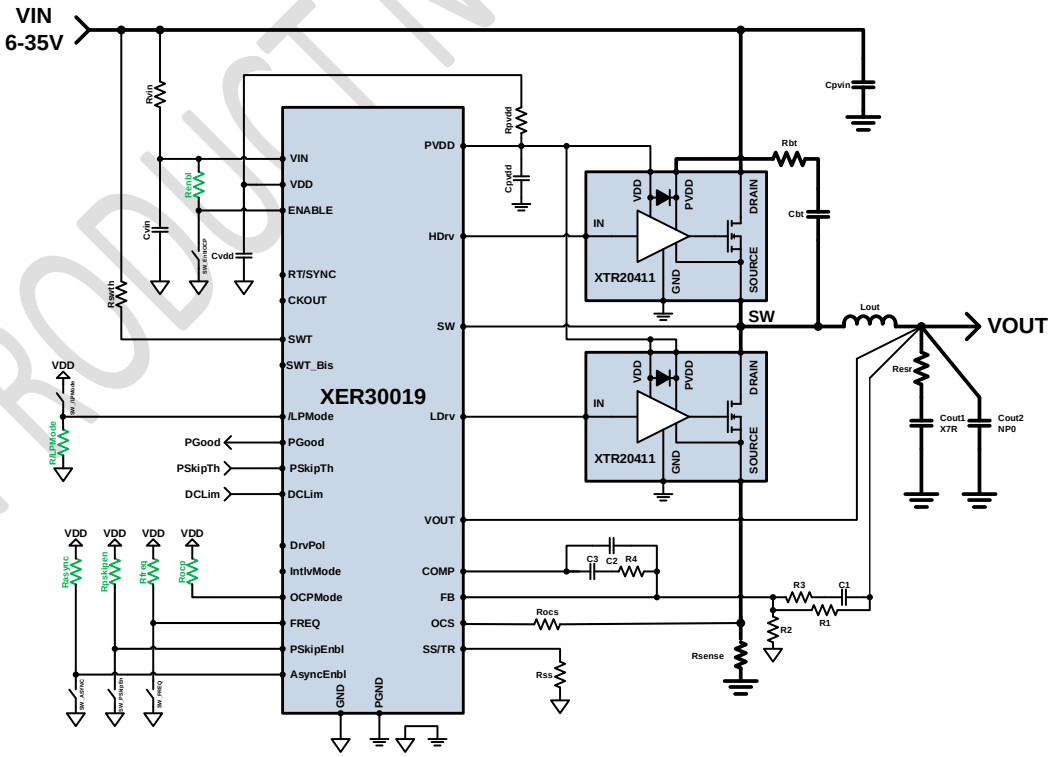


Figure 23. Buck (step-down) test configuration

TYPICAL PERFORMANCE (CONTINUED)

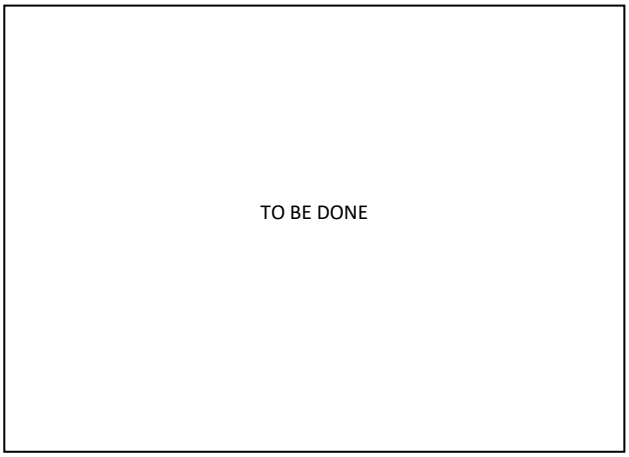


Figure 24. Comparison of full synchronous (dashed lines) and optimized mode with asynchronous mode and pulse-skipping mode enabled (plain lines) for several ambient temperatures. V_{IN}=7V. See Figure 23.

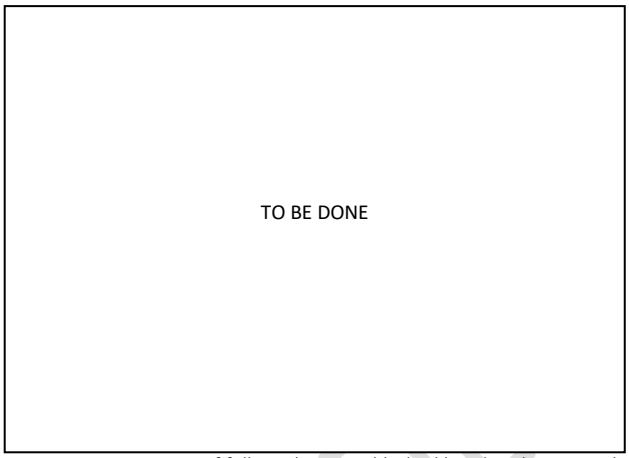


Figure 25. Comparison of full synchronous (dashed lines) and optimized mode with asynchronous mode and pulse-skipping mode enabled (plain lines) for several ambient temperatures. V_{IN}=30V. See Figure 23.

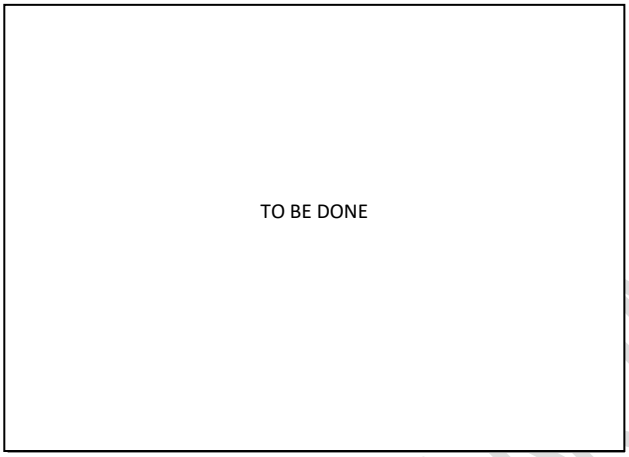


Figure 26. Efficiency vs load current for input voltages for T_{amb}=-50°C. Buck (step-down) configuration with operation in asynchronous mode and pulse-skipping mode enabled. See Figure 23.

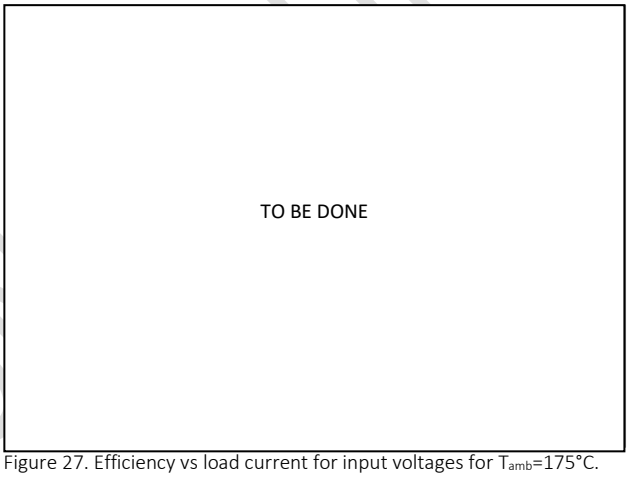


Figure 27. Efficiency vs load current for input voltages for T_{amb}=175°C. Buck (step-down) configuration with operation in asynchronous mode and pulse-skipping mode enabled. See Figure 23.

Introduction

The XER30019 is a voltage-mode PWM controllers able to operate from -50°C to +175°C, with supply voltages from 6V to 35V.

Integrated features include internal voltage reference and linear regulator, under-voltage lockout, synchronizing and externally tunable on-chip oscillator, programmable soft-start period with tracking capabilities, level and polarity programmable hiccup-mode over-current protection, anti-shoot-through, selection of the operating polarity of output drivers, programmable duty cycle limitation, possible interleave mode, low-power mode, asynchronous mode and pulse skipping mode with adjustable threshold.

Operation Modes

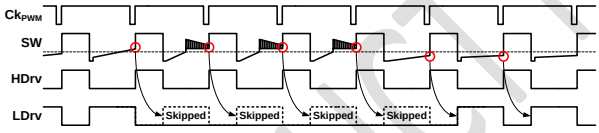
Low-power mode

Low-power mode operation (/LPMODE=0) allows a 5V output voltage from the DC-DC converter to be supplied to the PWM controller through the VOUT terminal. This voltage bypasses the internal linear regulator greatly reducing the current drawn from VIN and hence improving efficiency. Even without an external 5V, the low power mode can be forced. In this case, the PWM will operate under a 4V supply voltage generated by the internal LDO after the startup period. During the startup period, the internal LDO provides a 5V supply to the PWM. Once the PGood flag of the circuit is asserted, the LDO provides a 4V level.

Automatic transition to asynchronous mode

This mode is only available for Buck like converters. This mode is defined when OCPMode=1 (default mode thanks to the internal pull-up). For buck-like converters, automatic transition to asynchronous mode is allowed by setting AsyncEnbl=1 (or floating) or PSkipEnbl=1. In such a case, inversion of the inductor current in buck mode is detected by sensing the voltage on the switching node SW.

When the inductor current inverts during one cycle, conduction of the synchronous rectifier is disabled on the next cycle. When it is detected that the rectifier current does not inverts during one cycle, conduction of the synchronous rectifier is allowed in the next cycle. The controller toggles then automatically between synchronous and asynchronous modes depending on output current. This feature allows improving the DCDC efficiency at moderate and low current load.



When OCPMode=0 (i.e. not a Buck-like converter), the AsyncEnbl input, when grounded, turns-off the LDrv output, except in the interleaved mode (IntrlvMode=1) where AsyncEnbl has no effect on the ADrv output.

Pulse-skipping mode (case OCPMode=1)

When pulse-skipping mode is enabled (PSkipEnbl=1), automatic transition from synchronous to asynchronous modes is also forced, even if AsyncEnbl=0. Once the PWM duty-cycle becomes too low (threshold defined by the voltage on PSkipTh), the PWM controller will skip some clock periods. This occurs only at light load currents, where the load capacitance is able to supply the load during several clock periods without receiving energy. As long as the load current is low enough, the PWM will only provide some pulses with a fixed on-time as to keep the average output current. Output pulses are anyway synchronous with the internal clock. Once the load current starts increasing again, the system will skip less and less pulses before going back to asynchronous mode. If the load current further increases, the system will automatically switch to synchronous mode, depending on the voltage polarity on the SW node at the end of each clock period.

With OCPMode=1, the controller is always forced to go in asynchronous mode (i.e. LDrv output off) before entering into pulse skipping mode (i.e. LDrv still off and HDrv off for some clock periods).

In all cases, as long as the FB voltage is below 90% of the internal 1.2V reference, the LDrv output is off and the pulse skipping mode is authorized, whatever the PSkipEnbl level.

Pulse-skipping mode (case OCPMode=0)

With OCPMode=0, there is no asynchronous mode detector. The SW input is no longer monitored. If SW is available at the package level, it is recommended to leave SW floating (do not connect SW to VDD or VIN). In this mode HDrv and LDrv outputs work in complementary way (unless interleave mode is enabled) and the pulse skipping functionality still exists. As long as FB is below 90% of the internal 1.2V reference, the pulse skipping mode is forced, whatever the state of PSkipEnbl. Above this threshold, if PSkipEnbl=1, the LDrv is always the complementary of the HDrv as there is no asynchronous detector for this mode of operation. When OCPMode=0, it is possible to block the LDrv output by setting the AsyncEnbl input to ground. This reduces the dynamic consumption of the controller if the LDrv output is not required.

HDrv and LDrv operating mode

Outputs HDrv and LDrv behave differently depending on the programmable features used. In all cases, both outputs are never ON at the same time.

When in interleaved mode, the internal PWM signal is dispatched alternatively through the ADrv (LDrv) and BDrv (HDrv) outputs at every clock period[1]. This feature can be used in push-pull converters. In this case, OCPMode should be LOW.

When not in interleaved mode:

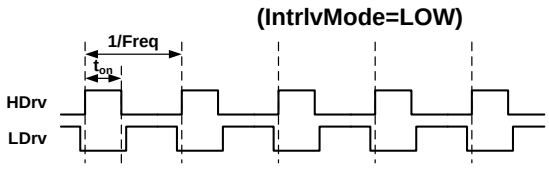
- Whenever ENABLE goes low or an under voltage occurs on VDD, both HDrv and LDrv outputs are OFF.
- During start-up or under any loss of regulation, the activity of HDrv and LDrv depends upon the status of control signals.
- In synchronous mode, both HDrv and LDrv are complementary (non-overlapped outputs).
- In asynchronous mode, LDrv is allowed to be OFF depending on the switching span of SW terminal, while only the HDrv is a copy of the internal PWM[2].
- It is also possible in some cases to turn off permanently the LDrv output in order to reduce the dynamic power consumption if LDrv not needed.[3]

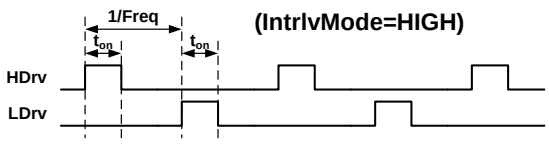
[1] At turn on, once VDD goes above the UVLO threshold, the first active output of the interleave mode is ADrv (LDrv).

[2] Depending on the DrvPOL pad status, HDrv can be active by HIGH state (default) or by a LOW state.

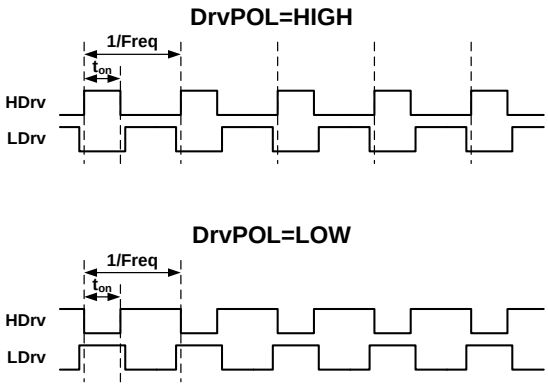
[3] OCPMode=0, AsyncEnbl=0

Condition	HDrv / BDrv	LDrv / ADrv
ENABLE=0	Off	Off
FB < 90% of V_{REF} (start-up, loss of regulation) IntrlvMode=0 IntrlvMode=1	Active	Off Active
FB > 120% of V_{REF} (loss of regulation) IntrlvMode=0 IntrlvMode=1	Off	Active Off
Synchronous mode (AsyncEnbl=0, PSkipEnbl=0)	Active	Active
OCPMode=0 and AsyncEnbl=0	Active	Off





Input DrvPOL changes the polarity of HDrv and LDrv. DrvPOL HIGH means that HDrv and LDrv are active when in HIGH state. Conversely, DrvPOL LOW makes HDrv and LDrv to be active when LOW. This feature allows parts of the XER30019 to be used with non-inverting or inverting drivers as well as N-type or P-type transistors. This feature is only available at die level or in a custom packaging configuration.



Internal Blocks and Functional Features

Supply voltage generation

The power supply block is composed by a voltage reference, a linear voltage regulator and a supply monitoring block.

An auxiliary input VOUT is used in case where the user de-sires to feed back the DC-DC output voltage to supply the controller. In such a case the DC-DC output voltage must be set to 5V (±10%)[4] only. This operating mode must be enabled by setting /LPMODE=0.

The low-power mode can also be used without feeding back a voltage on VOUT. Indeed, in this case when /PGood is asserted, the internal regulator supplies all blocks (including external power drivers if desired) with a lower voltage (4V).

[4] WARNING: if the voltage applied on VOUT is higher than 5.5V, the part may be permanently damaged. See "Recommended Operating Conditions "section.

Voltage reference

The voltage reference is of type band-gap and has a fixed output of 1.2V. This reference is used within the internal linear regulator as well as in the control loop as input of the error amplifier.

Linear voltage regulator

The linear voltage regulator supplies the internal circuitry as well as any external block connected to node VDD. The nominal output voltage is 5V, but it provides 4V when in low-power mode (/LPMODE=0) after PGood flag is asserted. The internal regulator is able to source up to 25mA for both output voltages. When ENABLE is pulled LOW, the internal LDO shuts down its output to GND.

The linear regulator output VDD must be externally connected to PVDD (eventually through some low-pass filtering) in order to supply the controller output buffers of HDrv & LDrv. A total load capacitance (on VDD & PVDD) between 300nF and 10uF is recommended for stability reasons. For proper operation, an input capacitor on VIN is also required (100nF or more).

Enable

When the ENABLE input goes under V_{ENOFF} threshold, XER30019 parts enter into shutdown mode, with the internal linear regulator and drivers outputs turned off. Output VDD is internally pulled down with a strength of about 1mA to prevent any unwanted behavior. The VDD terminal of the XER30019 cannot be forced to any voltage while ENABLE is LOW, otherwise malfunction or damage may occur. In case one of the outputs of the DC-DC converter (5V only) is connected to the VOUT terminal, this output voltage will discharge with a current of 1 mA. Additionally, PGood terminal is pulled down. When ENABLE is pulled above V_{ENON}, the PWM controller initiates a soft-start cycle.

ENABLE must not be connected to VDD (or PVDD) as this would prevent the internal regulator to start up. If not used, connect ENABLE to VIN.

Under-voltage lockout (UVLO)

The UVLO block monitors the supply voltage on VDD, ensuring that the internal oscillator and output drivers remain in the off state and by resetting the internal voltage of the SS/TR input to GND whenever VDD is below an internally set threshold. Notice that SS/TR can still be forced to a positive voltage, in case a voltage source is connected to implement the tracking functionality. Normal operation is achieved whenever VDD voltage goes above 4V. The UVLO block activates again whenever VDD drops below 3.5V. When VDD goes above 4V, the XER30019 initiates a soft-start sequence.

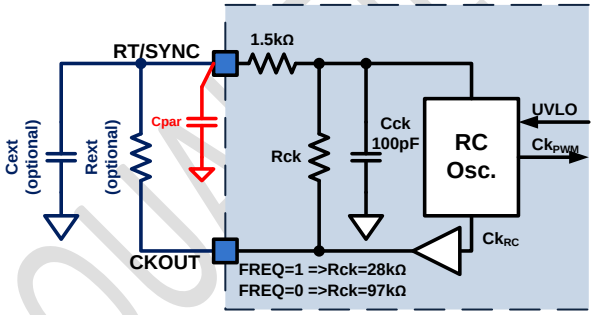
Oscillator

The internal oscillator generates a square clock signal (duty-cycle=50%) CkRC based on internal R_{ck} and C_{ck}. External resistor (decrease) and capacitor (increase) can be used in parallel with the internal ones through node RT/SYNC and CKOUT in order to change the oscillating frequency.

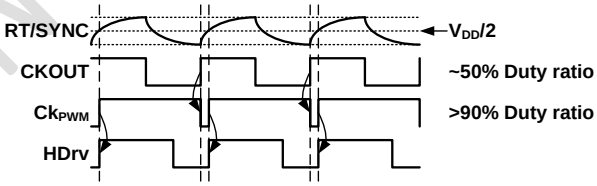
The oscillation frequency is given by the following relation (not taken into account the 1.5kΩ ESD resistor):

$$Freq = \frac{1}{T_{CK}} = \frac{1}{0.45 \cdot R_{Eff} \cdot C_{Eff} + 350ns}$$

$R_{Eff}=R_{Ext}//R_{ck}$ and $C_{Eff}=C_{Ext}+C_{par}+C_{ck}$.



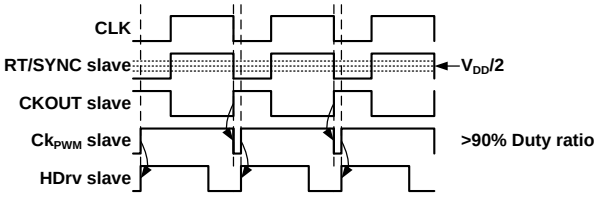
The following figure shows the evolution of signals on RT/SYNC, CKOUT, the internal PWM clock Ck_{PWM} and HDrv.



The signal on RT/SYNC is the charge and discharge of series resistor and capacitor between two thresholds equally spaced from $V_{DD}/2$. This leads to a CKOUT signal with a duty ratio close to 50%. When CKOUT goes up, an internal monostable is triggered ensuring a minimum off-time of the signal on HDrv. This minimum off-time of about 100ns sets the limit of the maximum possible output duty ratio. The internal PWM (HDrv) signal is triggered ON at the rising edge of the internal CK_{PWM} signal.

Synchronization of a PWM controller to an external clock, provided by another PWM controller or independent clock, is possible by directly driving the RT/SYNC terminal of the slave controller by the desired clock signal. The source providing the synchronizing clock must have an output impedance smaller than 6k.

The following figure shows a CLK signal fed to the RT/SYNC terminal of a slave controller. Notice that there is a phase inversion between the voltage on RT/SYNC and CKOUT of the slave device.

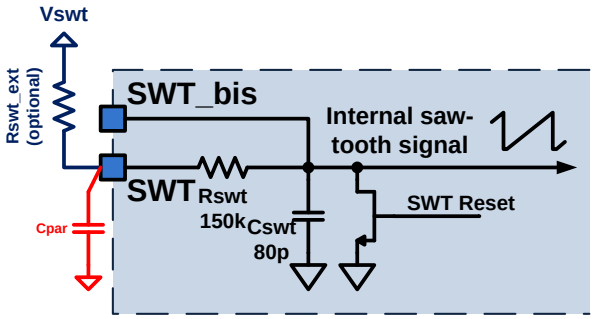


Saw-tooth signal generation

The saw-tooth signal is generated by the charge of an internal capacitor C_{SWT} (80pF) through an internal resistor R_{SWT} (150k). The XER30019 allows the addition of an optional external resistor in series with the internal R_{SWT} (150k), placed between node SWT and a positive supply

voltage. The parasitic capacitance on pin SWT must be minimized (10pF or lower if possible).
In Buck-like converters, using VIN as positive supply for the external saw-tooth resistor allows implementing the voltage feed-forward in order to have a loop gain independent of the supply voltage.

In a more general case, an external resistor R_{SWT_Ext} can be added to the internal R_{SWT} and a voltage different from V_{IN} can be used for saw-tooth signal generation. In such a case the total effective resistance R_{SWT_Tot}= R_{SWT}+ R_{SWT_Ext} must be considered.



The slope of the internal saw-tooth signal used for PWM generation is given by

$$Slope_{SWT} = \frac{V_{SWT}}{R_{SWT\_Tot} \cdot C_{SWT}}$$

The minimum allowed V_{SWT} voltage is 4V.

If V_{IN} and only the internal R-C components are used for saw-tooth generation, the slope value is

$$Slope_{SWT} = \frac{V_{IN}}{R_{SWT} \cdot C_{SWT}} = \frac{V_{IN}}{150k\Omega \cdot 80pF} = \frac{V_{IN}}{12\mu sec}$$

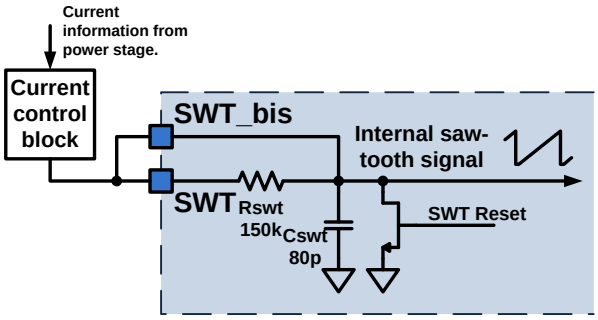
For loop gain determination, what matters is the "theoretical" peak saw-tooth voltage obtained from the following equation

$$V_{Peak} = \frac{V_{SWT}}{R_{SWT\_Tot} \cdot C_{SWT} \cdot Freq} = \frac{V_{SWT}}{R_{SWT\_Tot} \cdot C_{SWT}} \cdot T_{CK}$$

Freq=1/T_{CK} is the oscillation frequency of the PWM clock.

Note that V_{Peak} is the theoretical value that the internal saw-tooth signal would reach at the end of the clock period. Even if the theoretical V_{Peak} can be of several volts, what is really relevant is that the intersection between the saw-tooth signal and COMP happens under 2V. Otherwise said, the value of COMP in steady state should be 2V maximum. The intersection between the saw-tooth signal and COMP determines the maximum duty cycle that the PWM controller can reach in the target application.

The SWT_Bis node allows bypassing the internal saw-tooth generation resistor R_{SWT}, directly accessing to the internal capacitor terminal. The SWT_Bis terminal can be used to implement current-mode control by adding some external components. To ensure a correct reset of the saw-tooth signal, the injected current through SWT_Bis should not be higher than 200µA.



Soft-start and tracking functionality

The soft-start feature of the XER30019 controls the output voltage rise speed, limiting the inrush current during start-up. External resistor and capacitor can be added from the SS/TR node to GND in order to increase the soft-start period. The soft-start period is determined by the equation (Freq is the clock frequency):

$$t_{SS} = \frac{1.2V \cdot 2^{14}}{Freq \cdot V_{DD}} \cdot \frac{R_{SSExt} + 127k}{R_{SSExt}}$$ with R_{SSExt} > 40kΩ

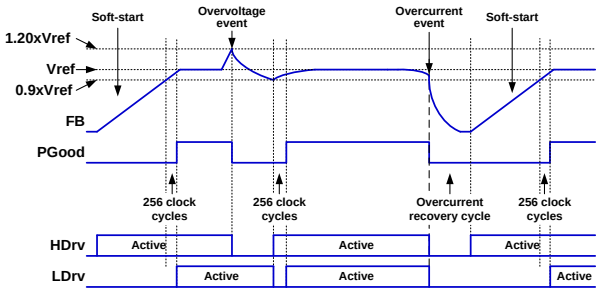
If no external resistor is used:

$$t_{SS} = \frac{1.2V \cdot 2^{14}}{Freq \cdot V_{DD}}$$

When the SS/TR input is driven by an external source below Vref, the output voltage tracks the voltage applied on SS/TR. Notice that there is a systematic offset between SS/TR and FB during operation (see Electrical Specifications section). For any mode other than the Interleaves mode of operation, output LDrv/ADrv is inactive whenever the voltage on SS/TR is below 90% of Vref.

Power-good flag

PGood is an active-HIGH output flag indicating that the DC-DC output is within a given range of values and that no overcurrent event is present. Output voltage sensing is performed on node FB. Whenever FB goes outside the range 90-120% of Vref (1.2V), PGood is immediately pulled down. In case of an overvoltage on FB (>120%Vref), the high-side output driver (HDrv) is turned off until FB reaches 90% of Vref, in which case the controller enters again into normal operation. Once that FB goes back above 90% of Vref, the PGood flag remains low for a period of about 256 clock cycles. When the HDrv driver is active again the output of the error amplifier COMP may be at an elevated value, depending on the loop filter speed. If COMP remains below DCLim, the value of COMP will determine the output duty-cycle. If COMP is slightly above DCLim, the output duty-cycle is determined by DCLim. If COMP goes above DCLim + 1.5V, the controller understands this situation as a critical error and self-resets, giving rise to a full soft-start cycle. If DCLim is externally forced above 2V, when the HDrv starts operating again, as COMP could be quite high, the output duty-cycle could be close to 100%. Depending on components used for the output LC filter and loop filter, this operation at high duty-cycle may give rise to an output overshoot, setting FB again above 120% and starting over a new recovery cycle. For this reason, it is strongly recommended to limit the duty-cycle by setting DCLim to an adequate value.
In an overcurrent (or short-circuit) event, PGood is immediately set LOW and an overcurrent recovery cycle starts followed by a soft-start cycle.
PGood is also pulled down in case of UVLO conditions and whenever ENABLE is LOW.
PGood output is softly pulled up to VDD through an internal 600kΩ resistor. Pull-up strength can be reinforced by connecting an external resistor between PGood and VDD. It is not allowed to pull PGood higher than VDD.



Error amplifier

The XER30019 error amplifier is of Miller-type OTA. The amplifier is capable of using Type II or Type III compensation filters, though in all cases the filter feedback must not have any DC path (capacitive feedback only) in order to keep a large DC gain.

In open loop, the error amplifier presents a GBW above 1.1MHz and a phase margin better than 40° for load capacitances up to 90pF. At PCB level, the FB and COMP nodes should be protected from any noisy signal.

PWM signal generation

XER30019 parts can operate in standard or pulse-skipping PWM generation modes.

In standard PWM mode, the internal saw-tooth signal is compared against the minimum of COMP (output of the error amplifier) or DCLim (duty-cycle limitation).

The DCLim analog input allows clamping of the maximum PWM duty-cycle (volt-second clamping). When the saw-tooth reaches Min[COMP, DCLim], a reset is asserted to the PWM logic, which in turn resets HDrv to the off state.

In a buck architecture, this duty-cycle limitation allows limiting the inductor current increase during the high side turn-on period (where the short-circuit protection is not active) in case of short-circuit. As soon, as the ON period finishes, the short-circuit protection senses the inductor current and immediately turns the PWM off if required.

In a flyback, forward or push-pull architecture, the volt-second clamping functionality provided by DCLim can be used to prevent transformer saturation.

The DCLim voltage is set by default to 40% of the VDD voltage (i.e. 2V for VDD=5V) with an internal 120kΩ resistor. The DCLim threshold can be lowered if needed using an external resistor to ground (R_{DCLim}) or an external voltage source. It is not recommended to set DCLim above 2V. However, if the DCLim functionality is not desired, DCLim can be directly connected to VDD, but in this case there is no volt-second clamping.

The volt-second clamping is given by

$$V_{SWT} \cdot t_{ON} = V_{DCLimit} \cdot R_{SWT\_Tot} \cdot C_{SWT}$$

The default volt-second clamping value is 24V.µsec (V_{DCLim}=2V, R_{SWT}=150k⍰, C_{SWT}=80pF).

From the equation above, the maximum ON time that can be achieved with the internal R_{SWT} and C_{SWT} for given V_{IN} and V_{DCLim} is

$$t_{ON\_Max} = \frac{V_{DCLimit}}{Slope_{SWT}} = \frac{V_{DCLimit} \cdot R_{SWT\_Tot} \cdot C_{SWT}}{V_{IN}}$$

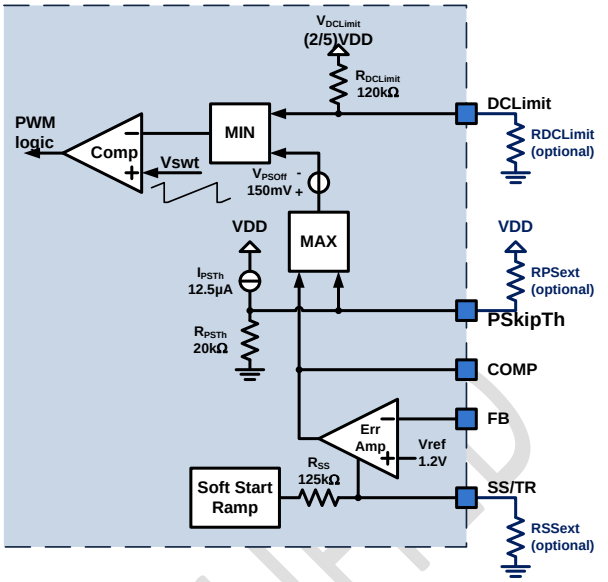
Knowing t_{ON_Max}, the maximum achievable duty-cycle is

$$D_{Max} = t_{ON\_Max} \cdot Freq = \frac{t_{ON\_Max}}{T_{CK}}$$

This gives a maximum ON time determined by V_{IN} as follows

$$t_{ON\_Max} = \frac{2V \cdot 150k\Omega \cdot 80pF}{V_{IN}} = \frac{24V \cdot \mu sec}{V_{IN}}$$

If COMP goes above DCLim + 1.5V, the PWM controller interprets this as an "unusual" event (rapid overload or lost of control loop) and it enters into a short-circuit recovery cycle. See section "**Over-current protection**" below.



For improved efficiency at low load currents, pulse-skipping mode can be used by ensuring PSkipEnbl=1. When pulse-skipping is enabled, the equivalent circuit of the PWM generator can be depicted as in the figure below.

During start-up, pulse-skipping mode is forced to ensure that settling to the final output voltage is achieved smoothly even for operation under very low duty ratios. An analog input PSkipTh is used to set minimum allowed on-time which must be adapted for given Vin-Vout-Freq parameters. For Buck converters (OCPMode=1), pulse-skipping mode takes place when operating in asynchronous mode only. In pulse-skipping mode, the output of the error amplifier is also compared against the saw-tooth signal, but in this case if COMP is under a given threshold, the controller keeps a minimum t_{ON} given by:

$$t_{ON} = \frac{V_{PSTh} - V_{PSOff}}{S_{SWT}}$$

$$V_{PSTh} = \left(\frac{V_{DD}}{R_{PSExt}} + I_{PSTh}\right) \cdot (R_{PSExt} // 20k)$$

V_{PSOff}=150mV, S_{SWT}=V_{IN}/($R_{SWTEff}C_{SWT}$), I_{PSTh}=12µA

In the previous equation it is supposed that an external R_{PSExt} is used between VDD and PSKipTh. If no R_{PSExt} is used, V_{PSTh}=250mV. When COMP is below PSkipTh, a dedicated block masks the clock setting pulses. The system enters into fixed t_{ON} mode which leads to a variable effective output frequency, but still synchronized by the internal clock which runs at a fixed frequency.

In a general case for a Buck converter where a voltage V_{SWT} is used to generate the saw-tooth signal, the output current at which pulse-skipping starts can be approximately determined by

$$I_{OutPS} = \frac{Freq \cdot \left[R_{SWT\_Tot} \cdot C_{SWT} \cdot \left(V_{PSTh} - V_{PSOff}\right)\right]^2}{2 \cdot L} \cdot \frac{V_{IN} - V_{OUT}}{V_{SWT}^2 \cdot V_{OUT}} \cdot V_{IN}$$

In case input voltage feed forward is used (V_{SWT}=V_{IN}) the equation for I_{OutPS} becomes

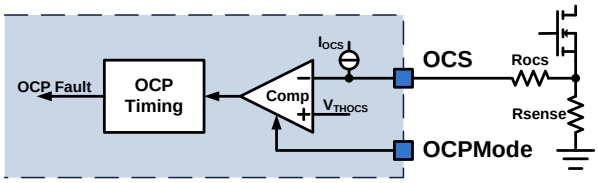
$$I_{OutPS} = \frac{Freq \cdot \left[R_{SWT\_Tot} \cdot C_{SWT} \cdot \left(V_{PSTh} - V_{PSOff}\right)\right]^2}{2 \cdot L} \cdot \frac{V_{IN} - V_{OUT}}{V_{IN} \cdot V_{OUT}}$$

If R_{SWT_Tot}=150kΩ, C_{SWT}=80pF, L=10µH, V_{IN}=30V, V_{OUT}=5V and V_{PSTh}=0.5V, Freq=520kHz, then I_{OutPS}=76mA.

Over-current protection

Over-current protection is achieved by sensing the voltage on a resistor in series with the source of the low-side transistor or directly on the

switching node SW (assuming that the R_{ON} of the synchronous rectifier transistor is known).



Control input OCPMode sets the sensing polarity on OCS node. For a Buck converter, the voltage sensed is negative (OCPMode=1). For boost, flyback or push-pull converters, the voltage sensed is positive (OCPMode=0).
An external resistor together with an internal current source I_{OCS} are used to set the over-current detection threshold. When an overcurrent state is detected, a recovery cycle starts immediately turning off the output drivers for a period of about 16100 clock cycles. After this period a new soft-start sequence is reinitiated. In this mode, hiccup current limiting is achieved.
The overcurrent threshold is determined by:

$$I_{OCP} = \frac{R_{OCS}}{R_{sense}} \cdot I_{OCS} \qquad \text{for OCPMode=1}$$

$$I_{OCP} = \frac{V_{THOCS} - I_{OCS} \cdot R_{OCS}}{R_{sense}} \qquad \text{for OCPMode=0}$$

For the second case (OCPMode=0), R_{OCS} should preferably be smaller than 3-4kΩ, as larger values would give a poor precision on the short circuit protection threshold. Due to the fast-transient response of the node used for current sensing, any parasitic capacitance on node OCS makes a low-pass filter with R_{OCS} resistor. To compensate for this effect, an external capacitor can be placed in parallel with R_{OCS}. This capacitor should be at least one order of magnitude larger than the expected parasitic capacitance on the OCS pin.
As mentioned in the previous PWM section, the short-circuit protection through the OCS sensing operates just after PWM signal goes low if OCPMode=1 and just before the end of the ON time of the PWM if OCPMode=0.
With OCPMode=1, terminal SW is used as a trigger to enable the OCS detection. This means that SW shall go below 0V to enable OCS detection on the current conduction cycle. This triggering mechanism is not present, nor needed, when OCPMode=0.
If the current increase through the inductor during the ON time of the PWM can be larger than the expected short-circuit current protection threshold, it is highly recommended to limit the maximum duty cycle using the DCLim analog input pin.
Indeed, a second short circuit protection is also integrated by means of the DCLim pin. This protection triggers a short-circuit recovery cycle whenever the error amplifier goes outside its linear regime (COMP above DCLim + 1.5V). For a strong short-circuit event (i.e. very low load impedances), COMP can rise quickly towards VDD (speed depends on the external RC filter of the error amplifier). In such a case, the XER30019 will consider a short-circuit event happened, even if the current sense is still in the blind period. On the other side, in case of an overcurrent (i.e. not strong short circuit), the COMP output rising can be much slower, so that the overcurrent event could be detected quite late. In such case, the over current will be first detected by the short circuit protection through the OCS terminal.
It is important to notice that second short circuit protection based on DCLim is always active, even if the OCS pin is not used. Nevertheless, it is possible to inhibit this second protection by connecting DCLim to VDD in the packages that have available DCLim. In such a case it is no longer possible to limit the maximum duty cycle of the PWM controller.

Output drivers & drivers control

The output drivers are able to source and sink at least 50mA at 175°C. By default, the HDrv and LDrv outputs are considered ON when they are at HIGH level. However, at die level, there is a pad DrvPOL which, when grounded, allows to reverse the logic (ON at LOW level). Both the LDrv and HDrv outputs are referenced to PGND and are able to provide a signal up to 5V (PVDD) of amplitude.
The drivers control block has anti-shoot through capabilities. Prevention of cross conduction is achieved by feeding back HDrv and LDrv nodes to the drivers control block for whatever the DrvPOL state. However, it is important that the used external drivers (high side and low side) present a delay mismatch smaller than the non-overlap period of the XER30019 controller defined earlier in the electrical specification.
System start-up is carried out in pulse-skipping mode forced internally until FB goes above 90% of the internal 1.2V reference.
In case an overcurrent event is detected, both the HDrv and LDrv outputs are set OFF for an internally timed recovery period. After this recovery period, a soft-start cycle is initiated.
When an overvoltage event is detected (FB going above 120% of 1.2V), the HDrv is set off, while and LDrv remains active, until FB recovers to 90% of Vref (1.2V).
For Buck converters only (OCPMode=1), a special feature, called "**Forced bootstrap capacitor pre-charge**" has been introduced in order to force the switching node SW to ground at some moments thus making sure the bootstrap capacitor charges. This is critical for the external high-side driver in order to guarantee a minimum charging of the associated bootstrap capacitor when the driver has no integrated charge pump circuitry. In normal operation (except pulse skipping), the SW node of a Buck converter is supposed to go to a slightly negative voltage at each clock period. At that moment, the bootstrap capacitor can be pre-charged. The high side driver will then operate as expected. If for any reason, the bootstrap capacitor is not pre-charged enough, the high side switching device cannot be turned on correctly anymore. The result is that the SW node will not be pulled down any more below ground by the output inductor. This can be an incorrect stable state from which the DC-DC cannot recover from itself. In order to avoid such condition, the XER30019 controller (when OCPMode=1) continuously checks if the SW node goes bellow about +1V at each clock period. If during 16 consecutive clock periods, the SW node never goes below this threshold, the PWM logic will force the LDrv output ON the next clock period as soon as the HDrv output is OFF. In practice, the duration of the LDrv pulse is very short (100ns range). As soon as SW goes below +1V, the LDrv turns OFF. Even during this short pulse, the system guarantees that HDrv and LDrv are never ON together.
In normal operation, the short LDrv pulse that occurs whenever SW remains positive over 16 clock periods can be observed at very low load current condition, when the system goes in deep pulse skipping (i.e. the PWM remains OFF for more than 16 clock periods) due to low load currents. The effect of this brief pulse on the output voltage ripple is nearly not visible. Without this short pulse, the bootstrap capacitor could discharge during asynchronous or pulse skipping operation and block the system. In case this "Forced bootstrap capacitor pre-charge" feature is not desired; it is possible to deactivate it by setting AsyncEnbl=0 and PSkipEnbl=1. This feature is not available for non-Buck converters (OCPMode=0).

System design guidelines

- FB, COMP and OCS terminals are sensitive to system noise. Layout these terminals with minimum parasitic capacitance and avoid any possible coupling with SW, HDrv, LDrv, CKOUT and PGOOD signals.
- Noise on RT/SYNC could cause erratic behavior of the internal clock generator. Avoid any possible coupling with SW, HDrv, LDrv, CKOUT and PGOOD signals. In case a capacitor is connected to RT/SYNC to slow down the clock, connect the capacitor to a noiseless GND. Do not connect this capacitor to PGND under any condition.
- Notice that terminal OCS is relative to PGND (not GND).
- Connect a capacitor of at least 1nF on terminals determining operational thresholds (PSKipTh and DCLim) to avoid any possible noise. For PSkipTh connect this capacitor to GND and for DCLim connect the capacitor to VDD.
- When using "input voltage feedforward", connect SWT to VIN through a resistor of at least 100Ω.

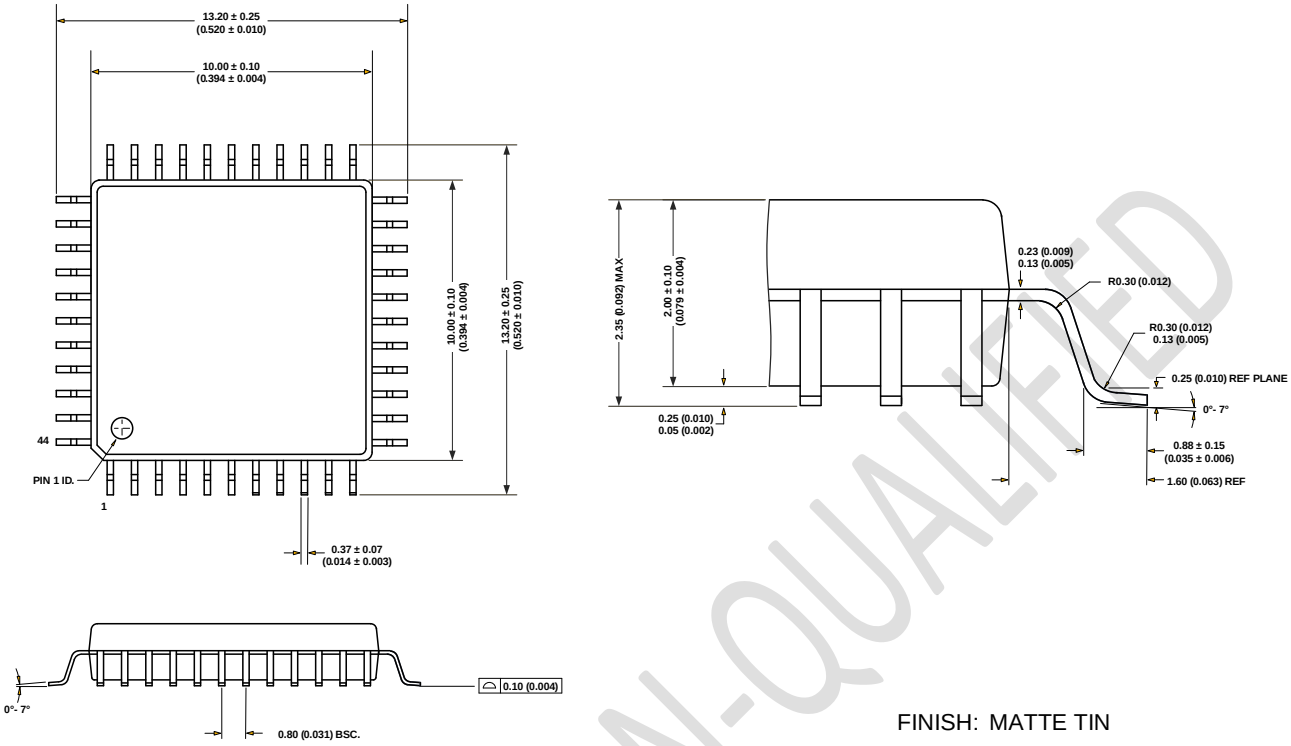
Summary of Operating Modes

Desired Functionality	OCPMode	PSkipEnbl	AsyncEnbl	IntlvMode
Buck mode with asynchronous and pulse skipping enabled. “Forced bootstrap capacitor pre-charge” active.	1	1	1	0
Buck mode with asynchronous and pulse skipping enabled. “Forced bootstrap capacitor pre-charge” inactive.	1	1	0	0
Buck mode with asynchronous enabled and pulse skipping disabled. “Forced bootstrap capacitor pre-charge” active.	1	0	1	0
Buck mode with fixed synchronous mode (after startup). “Forced bootstrap capacitor pre-charge” active.	1	0	0	0
Boost, flyback modes (complementary non-overlapped outputs). Pulse skipping mode enabled.	0	1	1	0
Boost, flyback modes with LDrv permanently off. Pulse skipping mode enabled.	0	1	0	0
Boost, flyback modes (complementary non-overlapped outputs). Pulse skipping mode disabled.	0	0	1	0
Boost, flyback modes with LDrv permanently off. Pulse skipping mode disabled.	0	0	0	0
Interleaved mode only. Pulse skipping mode enabled.	0	1	X	1
Interleaved mode only. Pulse skipping mode disabled.	0	0	X	1

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise stated.

Plastic QFP44



Part Marking Convention	
Part Reference: XERPPPPPP	
XER	X-REL Semiconductor, high-reliability product.
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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