ESD Protection Diodes with Ultra−Low Capacitance

The XESD2LV is designed to protect voltage sensitive components that require ultra− low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

DFN0603-D

Specification Features:

- Ultra Low Capacitance 1.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
  (0.61 mm x 0.31 mm)
- Low Body Height: 0.28 mm
- Stand−off Voltage: 10 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- This is a Pb−Free Device

Device	Marking	Shipping
XESD2LV12M	M	15000/Tape&Reel

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V−0

LEAD FINISH: 100% Matte Sn (Tin)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	200	mW
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature Range	T_J	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

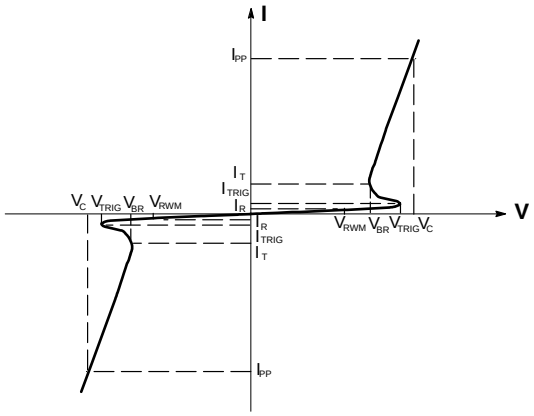
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.62 in.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse standoff voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{TRIG}	Reverse trigger voltage
I_{TRIG}	Reverse trigger current



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF)	V_C (V) @ I_{PP} = 1.65 A (Note 3)	V_C
		Max	Max	Min	mA	Max	Max	Per IEC61000−4−2 (Note 4)
XESD2LV12M	M	10	1.0	12	1.0	1.8	24.5	Figures 1 and 2 See Below

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Surge current waveform per Figure 4.
4. For test procedure see Figures 3.

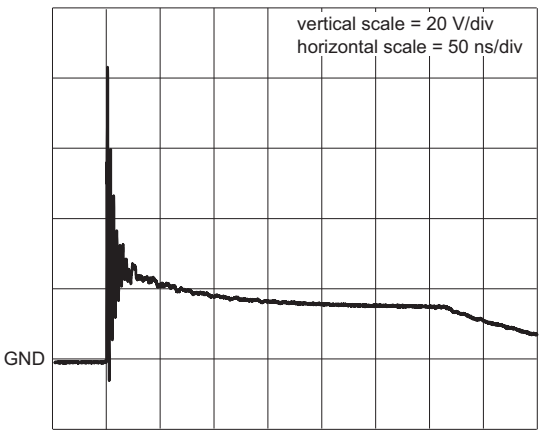


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

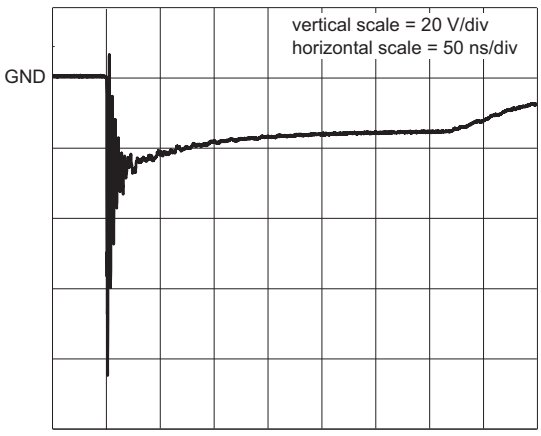


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000–4–2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

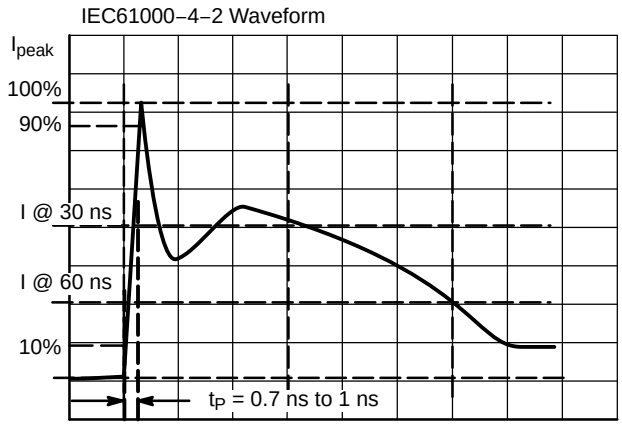


Figure 3. IEC61000–4–2 Spec

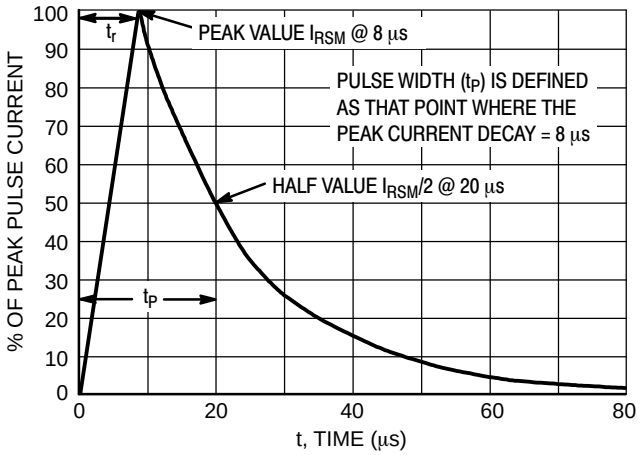


Figure 4. 8 X 20 µs Pulse Waveform

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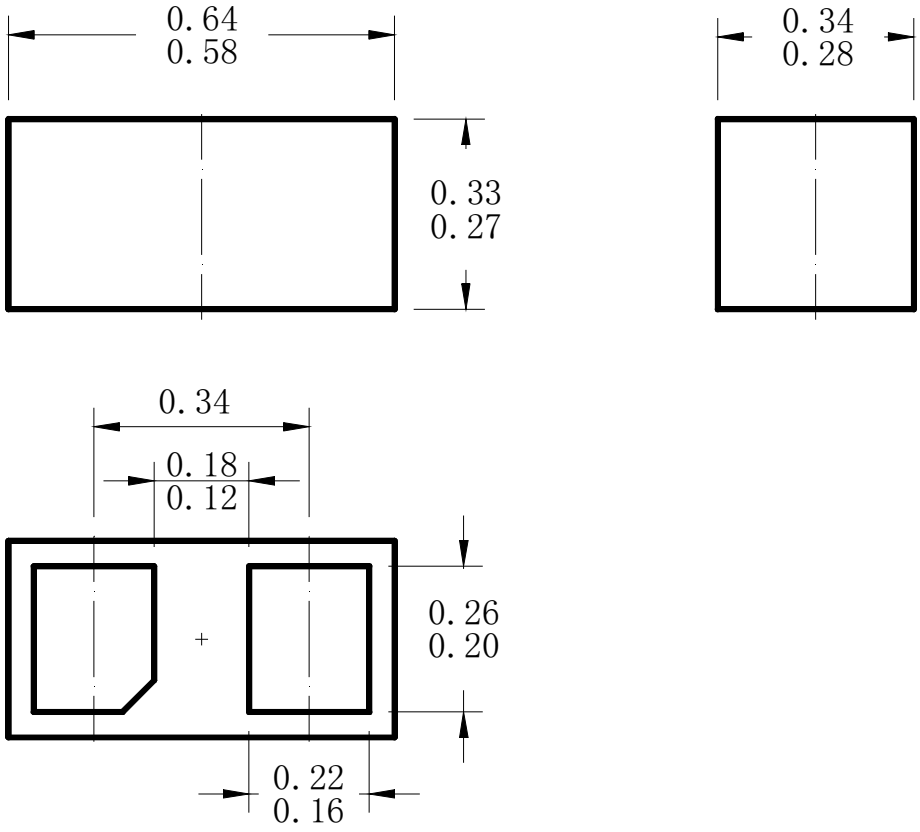
DIMENSION OUTLINE:

Unit:mm



Soldering Footprint