XL2864A

8K X 8 Electrically Erasable PROM

FEATURES

- **Fast Read Access Times**
  — 250ns, 300ns, 350ns, 450ns
- **5 Volt-only Operation Including Write**
- **Industrial Temperature Range Available (XLE2864A)**
- **Fast Nonvolatile Write Cycle**
  — Internally Latched Data and Address
  — 200ns Byte-load Cycle
  — 10ms (max.) Nonvolatile Write Cycle
  — Automatic Erase Before Write
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{DATA}$ Polling To Minimize Write Cycle Times**
- **Automatic Page Write**
  — 1 to 32 bytes in 10ms (max.)
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**

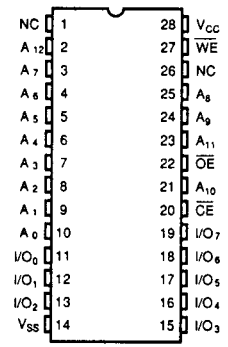
OVERVIEW

The XL2864A is a full-featured, 8K x 8 bit E^2PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E^2PROM devices. Read access times are as low as 250ns; standby current, less than 50mA. The device is fully functional with a single 5V power supply, and the XL2864A is manufactured with EXEL's 2.0µ NMOS E^2PROM process.

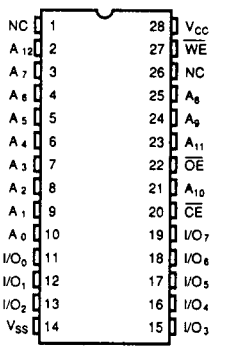
The device is exceptionally system friendly, incorporating a device status indicator and a fully automatic 32-byte page write feature. $\overline{DATA}$ polling is provided to maximize device versatility and allow the host system to exploit the actual nonvolatile write cycle time. This is a software technique which is used to observe nonvolatile write cycle completion without requiring external hardware.

PIN CONFIGURATION

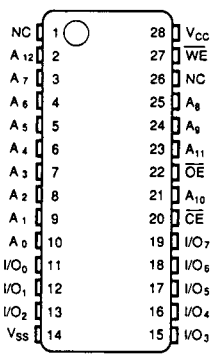
28 Pin PDIP
Type "P" Package



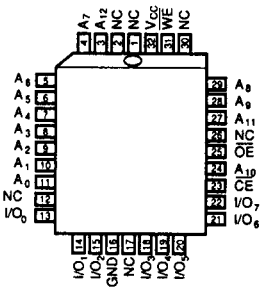
28 Pin CERDIP
Type "C" Package



Small Outline
Type "J" Package



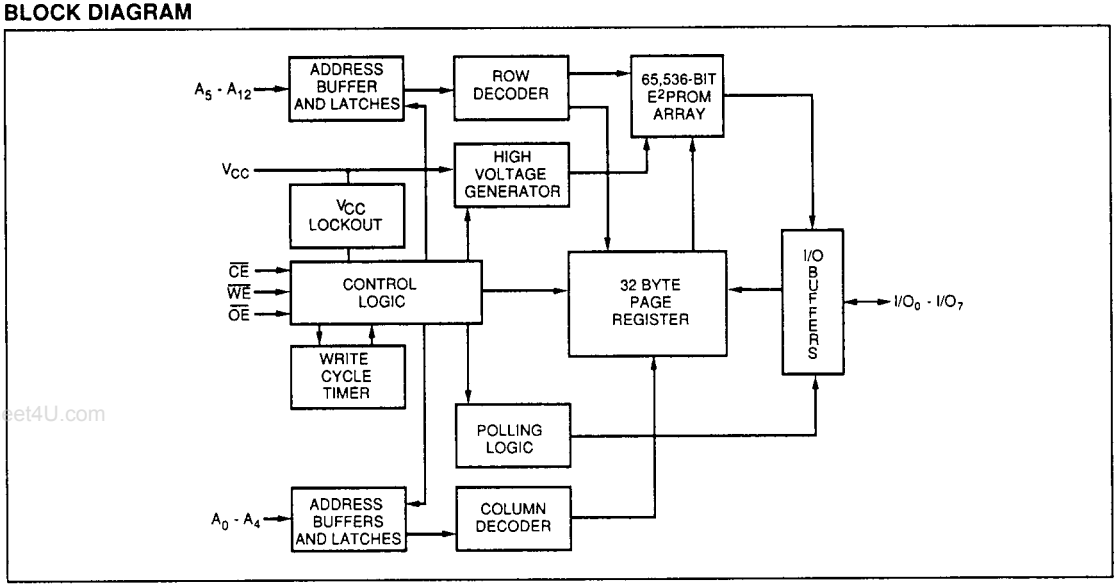
32 Pin PLCC
Type "D" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The automatic page write feature allows the system to program up to 32 bytes during a single nonvolatile write cycle, providing an effective write speed of at most 312ms/byte. The entire 8K byte memory may be programmed in a maximum of 2.6 seconds when the page write mode is employed.

The XL2864A features $\overline{OE}$ write inhibit logic and noise protected $\overline{WE}$ to inhibit inadvertent writes.

The XL2864A is compatible with industrial standard 8K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL2864A provides secure and reliable data storage thoughout your systems lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2864A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2864A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2864A is designed for applications requiring up to 10,000 data writes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

The latches in the automatic page write buffer include corresponding flag bits which are set when a given page location is written. In the event that a nonvolatile write cycle occurs with less than 32-bytes of data, only those bytes in the E^2PROM array corresponding to the locations in the buffer which were actually written will be reprogrammed. This feature eliminates unnecessary cycling and ensures maximum endurance. This is in contrast to some competing E^2PROM devices which reprogram the full page of nonvolatile locations independent of the number of page latches actually written to. This wastes cell cycles and may substantially reduce device endurance and, consequently, system reliability.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2864A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2864A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Write Mode

In the XL2864A, the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both address and data are latched in a brief 150ns interval using a 5V supply and TTL write signals.

Once the data is latched, the XL2864A will automatically erase the selected byte and write the new data in less than 10ms. The host system is therefore freed to proceed with other operations while the XL2864A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress with the exception of I/O_7 if a read command is asserted. (See Monitoring Device Status in the next column of this page.) (See Figures 3 and 4.)

Standby Mode

Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 50mA. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode

The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O pins high. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL2864A, a status indicator has been incorporated to provide for the host system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL2864A until it determines a simple logical condition.

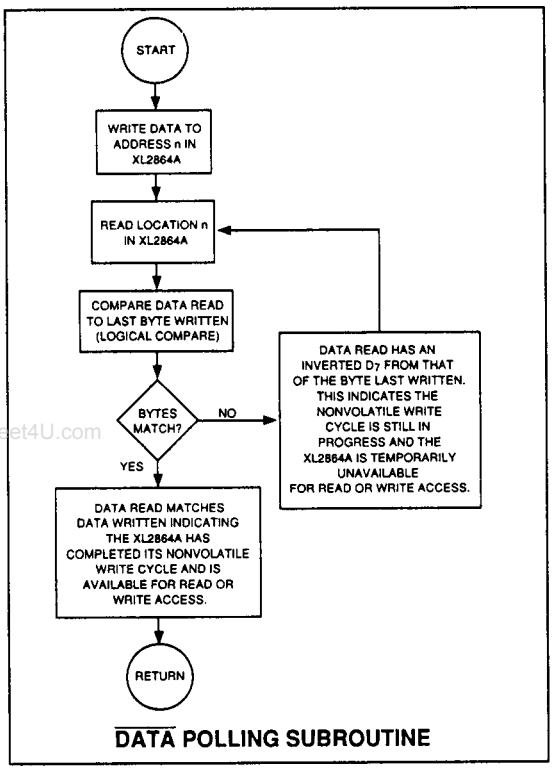
$\overline{DATA}$ Polling

The XL2864A provides a feature named $\overline{DATA}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL2864A is busy executing its nonvolatile write cycle will be interpreted as a $\overline{DATA}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{DATA}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile write cycle timing.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓_⊓	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊓_⊓	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	⊓_⊓	Chip Erase*	$D_{IN} = V_{IH}$	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL Microelectronics for details on the Chip Erase Mode.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL2864A. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL2864A. During the 10ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O7. I/O7 is set to output the **complement** of the value of the MSB of the last byte written to the XL2864A when a read command is asserted. (See Figure 5.)

The READY/$\overline{\text{BUSY}}$ test procedure is quite simple. The system simply reads the location last written to in the XL2864A and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL2864A is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to wait the 10ms (max.) period specified and enabling accelerated device loading operations.

Automatic Page Write

The XL2864A contains a 32-byte temporary (volatile) buffer which allows the user to simultaneously program from one to 32 bytes in a page during a single 10ms (max.) nonvolatile write cycle without any special setup or software procedures. This can effectively reduce the byte write time by a factor of 32. The device will begin its nonvolatile write cycle from 300 to 600µs (t_{PL}) after the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). At this point, the device commences a nonvolatile write cycle and copies data from each of the latches which were updated into the designated E^2PROM locations (see Endurance and Data Retention section). Thus, all bytes to be programmed during an automatic page write cycle must be written into the page buffer within t_{PL} minimum to guarantee that they are transferred into the E^2PROM array. (See Figure 6.)

The 32-byte page into which the data will be written is specified by the most significant bits of the address (A_5-A_{12}) presented during the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). The byte within the specified page is identified by the five least significant bits of the address (A_0-A_4) presented during the first and subsequent system write cycles. Bytes may be written into the page in any order. If data is written more than once to the same byte in the temporary buffer during a single page load operation, then the most recently written data will be valid.

If a read operation is attempted during loading of the page buffer, the buffer load cycle is not affected. However, that read cycle will be interpreted as a $\overline{\text{DATA}}$ polling cycle.

WRITE PROTECT MECHANISMS

The XL2864A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{\text{OE}}$ Write Inhibit

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will be inhibited. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 20ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin (except $\overline{OE}$)* ..... -1.0V to +6.5V
Voltage on $\overline{OE}$ Pin* ..... -1.0V to +22.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		110	mA
I_{SB}	V_{CC} Current-Standby	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.25V	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.25V	-10	10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH}= -400µA	2.4		V
V_H	High Voltage for Chip Erase		15	18	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	XL2864A-250 Limits		XL2864A-300 Limits		XL2864A-350 Limits		XL2864A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		80		80		120		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	125		ns
t_{CS}	Chip Enable or Write Enable Setup Time	0		ns
t_{CH}	Chip Enable or Write Enable Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}*	Write Enable Pulse Width	150		ns
t_{WPH}	Write Recovery Time	50		ns
t_{DV}	Data Valid Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{PL}	Page Load Time	300	600	µs
t_{BLC}	Byte Load Cycle	0.2	25	µs

* NOTE: A write pulse of less than 20ns will not initiate a write cycle.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

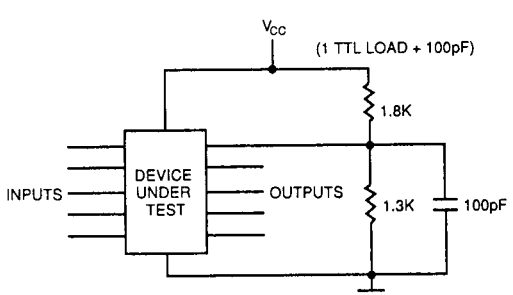


FIGURE 1. AC TEST CONDITIONS

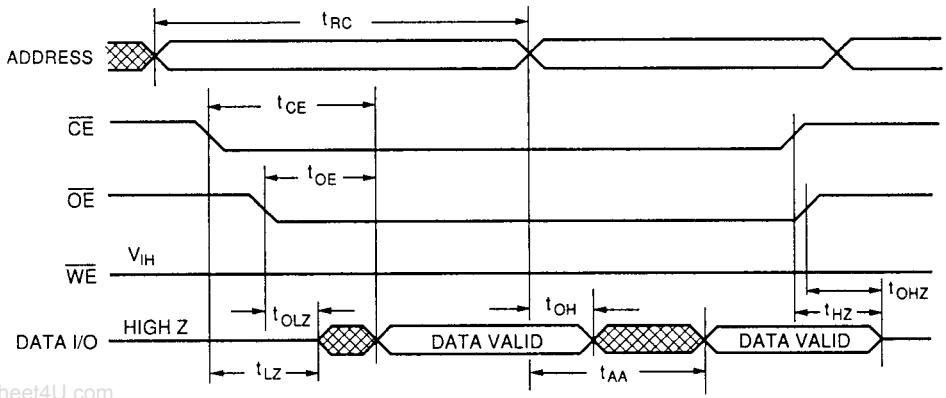


FIGURE 2. READ CYCLE TIMING

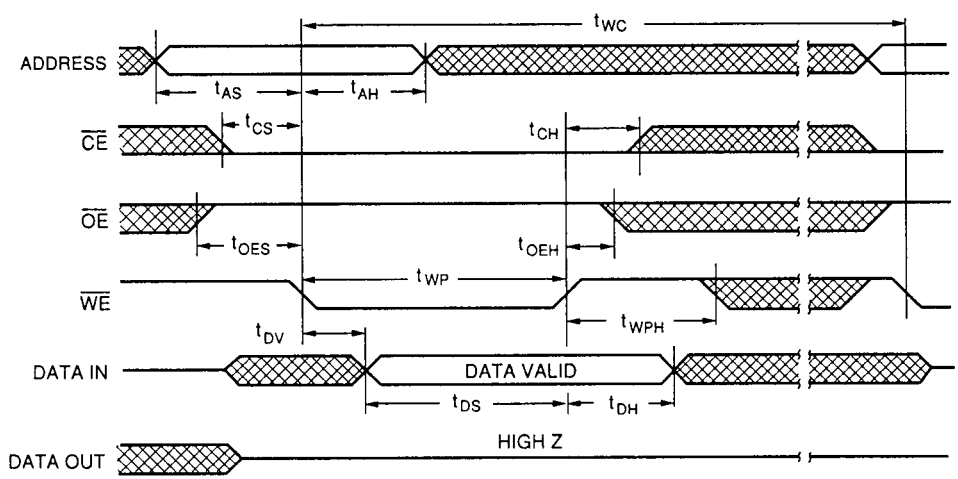


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

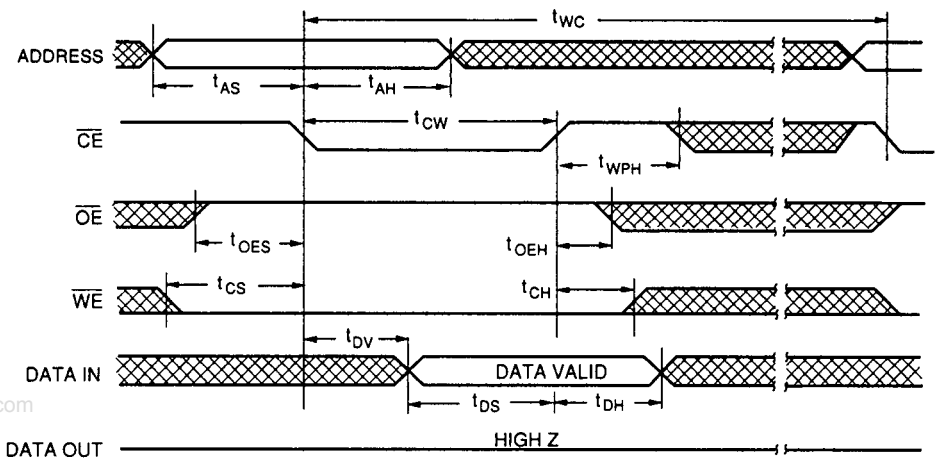
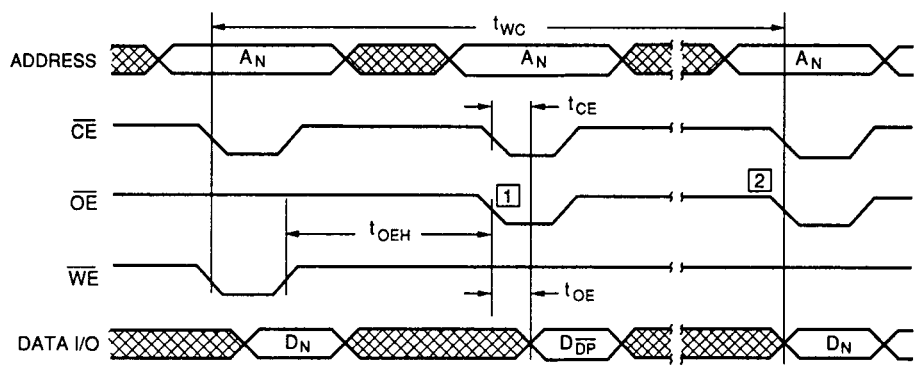


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL2864A indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

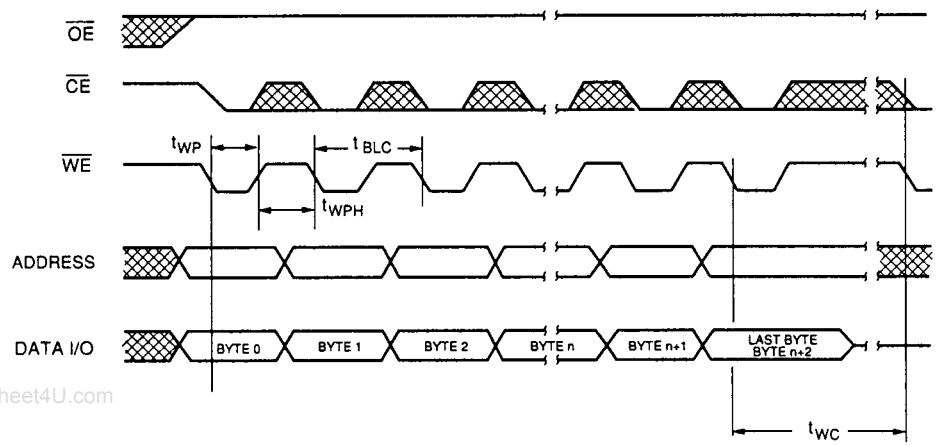


FIGURE 6. PAGE MODE WRITE CYCLE TIMING