EXEL MICROELECTRONICS
Excellence in E²

XL93C66

4,096-Bit Serial Electrically Erasable PROM **with 2V Read Capability**

FEATURES

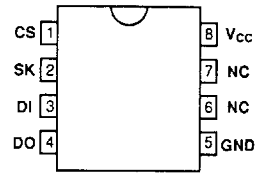
- State-of-the-Art Architecture
  - — Nonvolatile data storage
  - — Single supply - 5V operation
  - — Fully TTL compatible inputs and outputs
  - — 1MHz operation
- Hardware and Software Write Protection
  - — Defaults to write-disabled state at power up
  - — Software instructions for write-enable/disable
- Low Power Consumption
  - — 1mA active (typical)
  - — 1μA standby (typical)
- Low Voltage Read Operations
  - — Reliable read operations down to 2.0 volts
- Advanced Low Voltage CMOS E^2PROM Technology
- Versatile, Easy-to-Use Interface
  - — Self-timed programming cycle
  - — Automatic erase-before-write
  - — Programming Status Indicator
  - — Word and chip erasable
- Durable and Reliable
  - — 10-year data retention after 100K write cycles
  - — Minimum of 100,000 write cycles per word
  - — Unlimited read cycles
  - — ESD protection

OVERVIEW

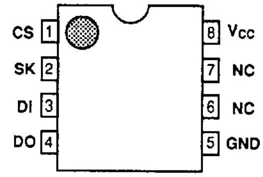
The XL93C66 is a low cost 4,096-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93C66 provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



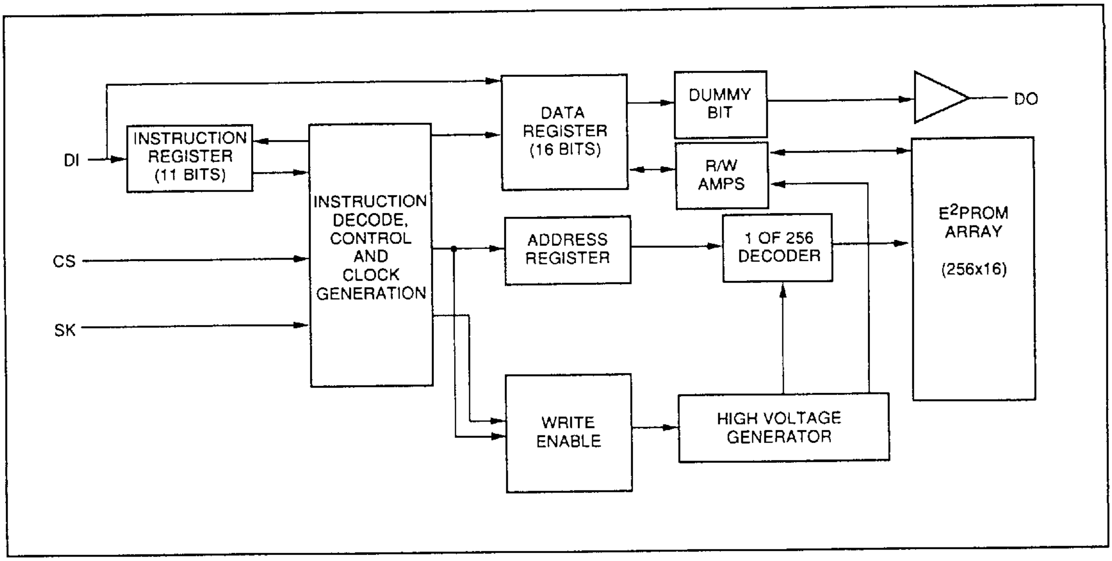
EIAJ Small Outline "JR" Package



PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

BLOCK DIAGRAM



APPLICATIONS

The XL93C66 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93C66 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93C66 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93C66 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93C66 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93C66 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/BUSY status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.(See Figure 6.) The ERAL operation is required before WRAL operation. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/BUSY status of the chip. (See Figure 6.)

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

SERIAL 2 P'DCTS

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address	Input Data
READ	01	10	(A_7-A_0)	
WEN (Write Enable)	01	00	11XXXXXX	
WRITE	01	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	01	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	01	00	00XXXXXX	
ERASE	01	11	(A_7-A_0)	
ERAL (Erase All Registers)	01	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93C66 .... 0°C to +70°C
XLE93C66 .... -40°C to +85°C
Storage Temperature. .... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) .... 300°C
Supply Voltage .... 0 to 6.5V
Voltage on Any Pin .... -0.3 to Vcc +0.3V
ESD Rating 2000V
NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C66 or -40°C to +85°C for the XLE93C66

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current (CMOS)	CS = DI = SK =0V		4		2	μA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	μA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	μA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400μA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10μA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10μA CMOS	Vcc-0.2		Vcc - 0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C66 or -40°C to +85°C for the XLE93C66

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time		250		2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ↑	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ↑	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ↓	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ↑	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		n/a	ms

CAPACITANCE

$T_A = 25°C$, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

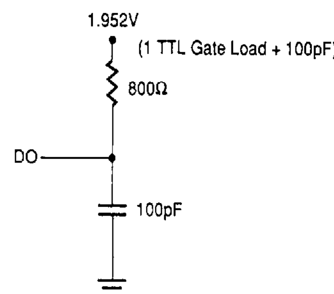
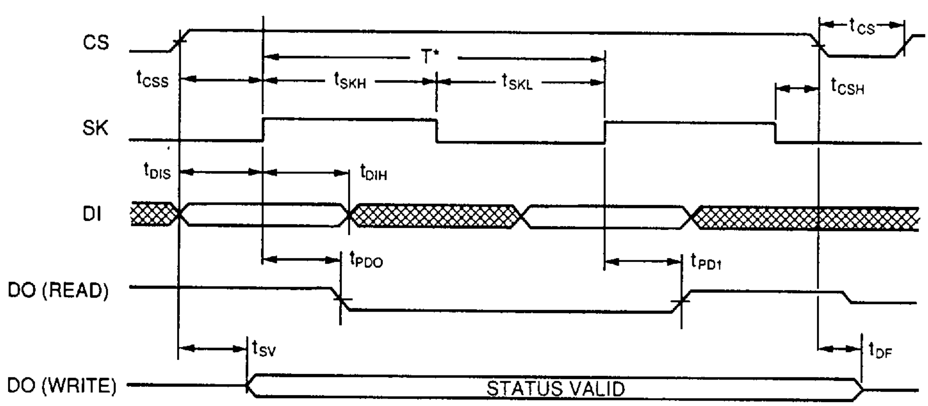


FIGURE 1. AC TEST CONDITIONS



*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING

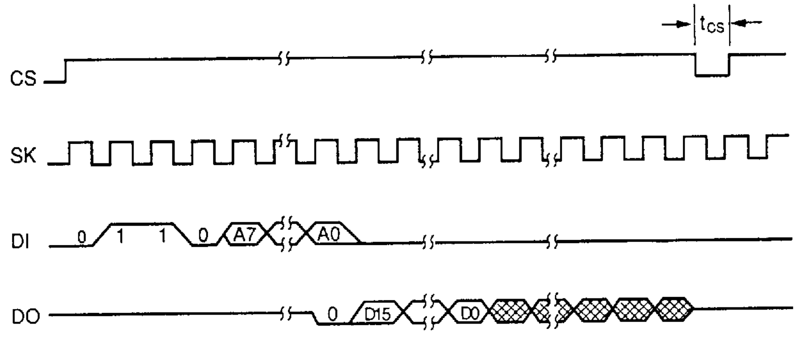


FIGURE 3. READ CYCLE TIMING

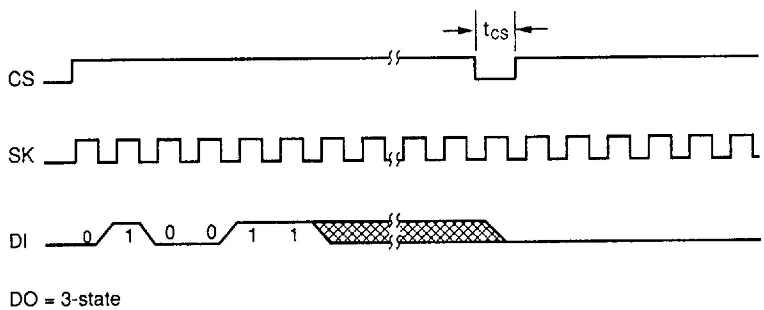


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

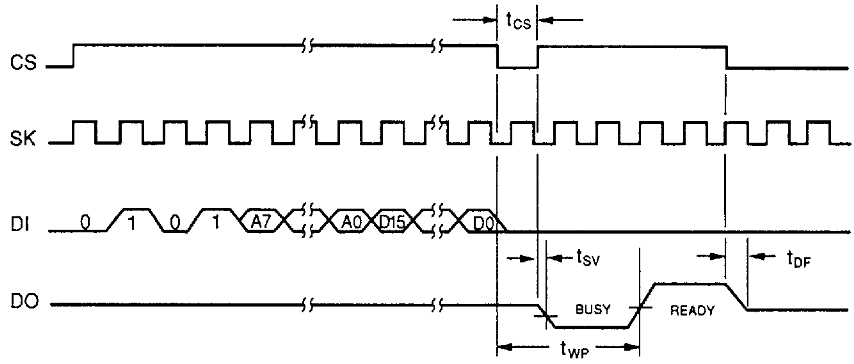


FIGURE 5. WRITE CYCLE TIMING

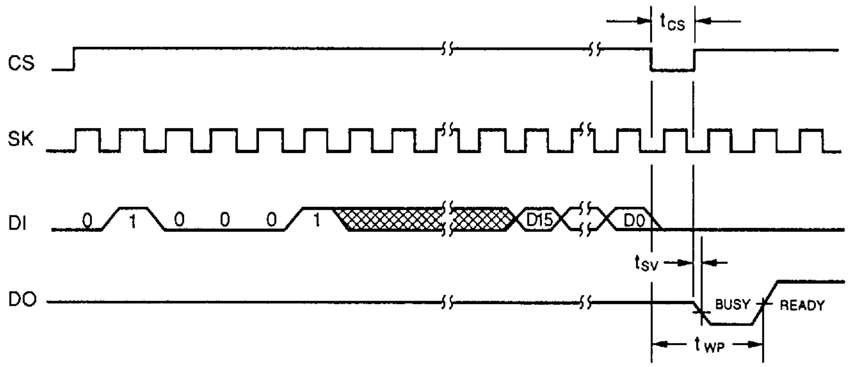


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

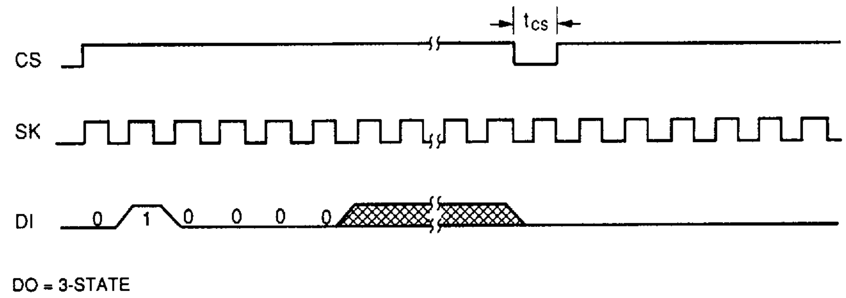


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

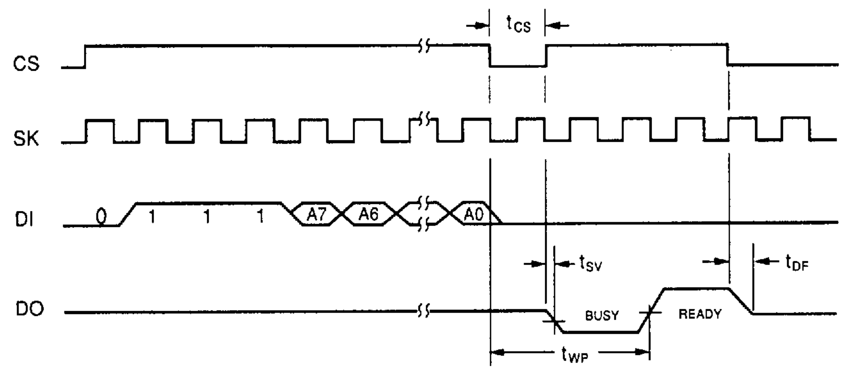


FIGURE 8. ERASE (REGISTER) CYCLE TIMING

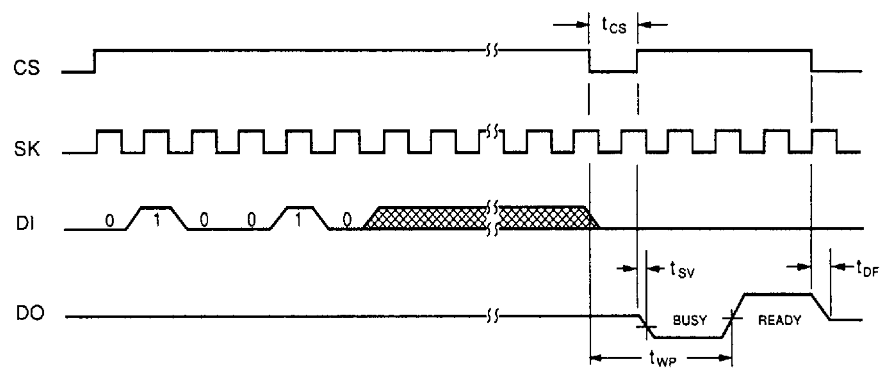


FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING