XM91080A

Datasheet

FHD TFT Display Driver
16M Color, 1080RGB x 1920 (MAX. 2400), Gateless Panel

Table of Contents

1 Reversion History

Version	Date	Page	Description
V0.01		ALL	New Created

2 General Description

2.1 Purpose of this Document

This document has been created to provide complete reference specifications for the XM91080. IC designers, testing engineers and application engineers should refer to these specifications for circuits design, quality/performance control, and IC applications for customer.

2.2 General Description

The XM91080 device is single chips RAM less solution for LTPS TFT LCD that incorporates gate drivers, a timing controller with glass interface level shifters, a VCOM driver and a glass power supply circuit.

The XM91080 can support MIPI interface. The source resolution support 1080RGB, and the gate resolution also can be set from 1920 lines to 2400 lines.

The XM91080 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC includes internal boosters that generate the LCD driving voltage, breeder resistance and voltage follower circuit for the LCD driver.

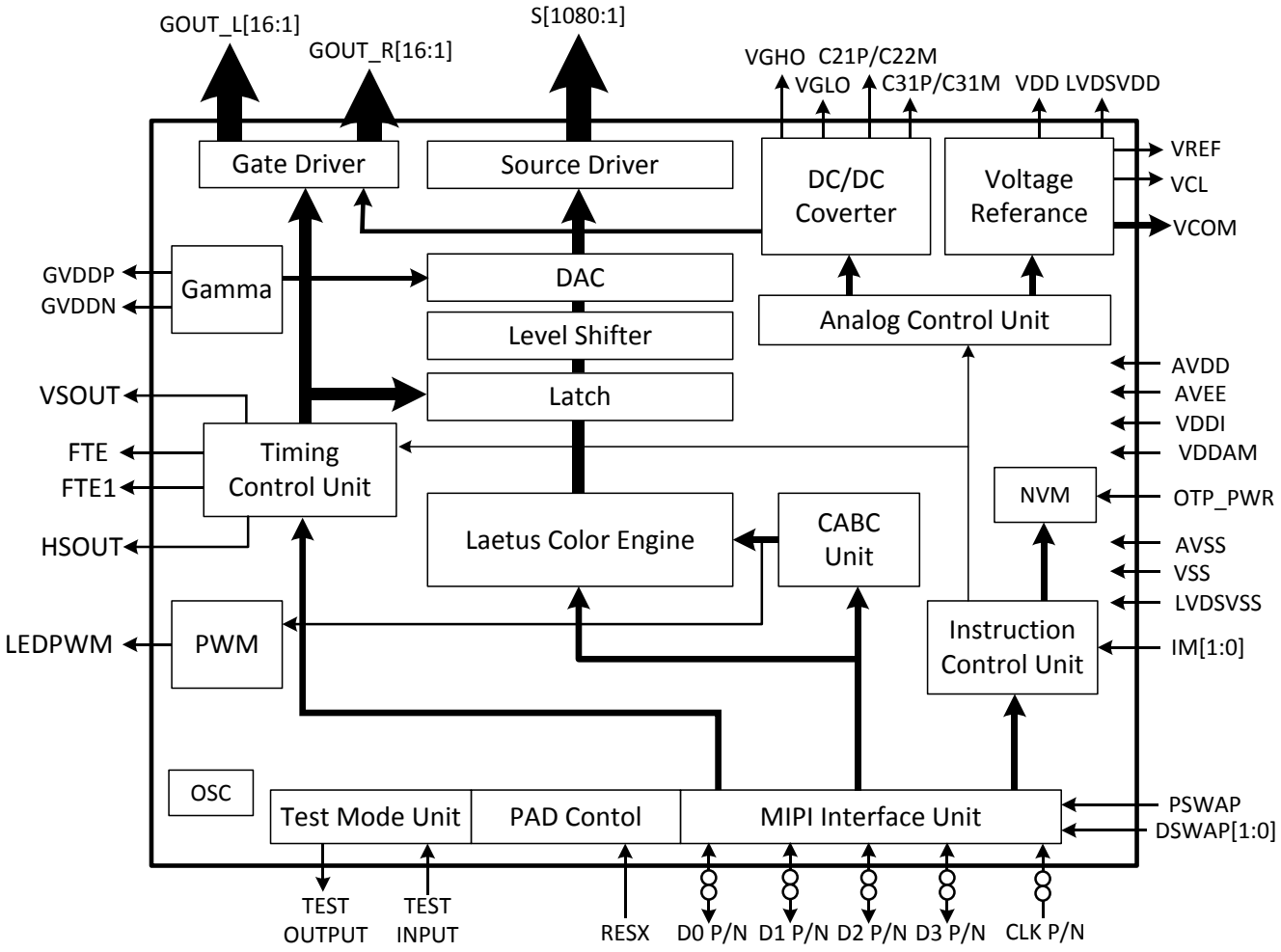
The XM91080 also supports CABC function for the backlight control. It's able to reduce the total power consumption of display module significantly.

This LSI is suitable for small or medium sized portable mobile solutions requiring long term driving capabilities, including bidirectional pagers, smartphone, digital audio players, cellular phones and handheld PDA.

3 Features

- **Single chip FHD LTPS Controller / Driver.**
- **Display Resolution**
  - 1080RGBx1920
- **Display Modes**
  - Full Color Mode: 16.77M colors (24bit data, R: 8bit, G: 8bit, B: 8bit)
  - Reduced Color Mode: 8 colors (3bit data, R: 1bit, G: 1bit, B: 1bit)
- **Interface**
  - MIPI DSI Interface
    - Support DPHY: V1.0
    - Support DSI: 1.01
    - Support DCS: 1.01.
    - MIPI I/F Supported 2, 3 or 4 data lanes
- **Display Features**
  - Individual gamma correction setting for RGB dots
  - Support 1080 source channels output
  - Support gate control signals GOUT_L[1:16], GOUT_R[1:16] for gate driver
  - Support 1dot / column / zigzag inversion
- **On Chip Function**
  - DC/DC converter
  - VCOM voltage generator
  - Provide OTP (1 time) to store related Power, LTPS setting, and DDB calibration
  - Provide MTP (4 times) to store VCOM, ID1, ID2, ID3, and gamma setting
  - Oscillator for display clock generation
  - On module checksum checking
  - Image enhancement technology
- **Content Adaptive Brightness Control (CABC) Function**
  - Histogram analysis & data process
  - Dimming control
  - Only supported in full display mode

4 Block Diagram



5 Pin Description

Signal	I/O	Pad Type	Function
Power Supply Pad			
AVDD	I	Analog Power	4.5V~6.0V. Connect a capacitor for stabilization
AVEE	I	Analog Power	-4.5V~-6.0V. Connect a capacitor for stabilization
VDDI	I	Digital Power	Power Supply for IO, 1.65V~1.95V.
VDDAM	I	Digital Power	Power Supply for MIPI LDO, 1.65V~1.95V.
AVSS	I	Analog Ground	Ground for source.
VSS	I	Digital Ground	Ground for Digital Circuits.
LVDSVSS	I	Digital Ground	Ground for Analog Circuits.
OTP_PWR	I	I/O Power	Used for external power input for OTP program
DC-DC Converter Pad			
VGH	O	Internal Power	Positive Charge Pump Power. Connect a capacitor for stabilization.
VGL	O	Internal Power	Negative Charge Pump Power. Connect a capacitor for stabilization.
C21P/C21M	O	Internal Power	Flying cap for VGH charge Pump. Connect a capacitor for stabilization.
C31P/C31M	O	Internal Power	Flying cap for VGL charge Pump. Connect a capacitor for stabilization.
EXTP	O	Analog	Please keep it open.
EXTN	O	Analog	Please keep it open.
Regulator Pad			
VCL	O	Internal Power	Regulator output voltage
VDD	O	Internal Power	Regulator output voltage. Connect a capacitor for stabilization.
LVDSVDD	O	Internal Power	Regulator output voltage generate. Connect a capacitor for stabilization.
VCI1	O	Internal Power	Reference voltage.
GVDDP	O	Internal Power	Regulator output voltage (for positive gamma high voltage generator).
GVDDN	O	Internal Power	Regulator output voltage (for negative gamma high voltage generator).
VGHO	O	Internal Power	Regulator output for panel control circuits.
VGLO	O	Internal Power	Regulator output for panel control circuits.
LCD Interface Logic Pad			
RESX	I	Digital (VDDI)	Global Reset Signal. Active Low.

<table>
<tr><td>PSWAP</td><td>I</td><td>Digital (VDDI)</td><td>MIPI lane polarity swap pin.
<table>
<tr><td rowspan="2">PSWAP</td><td rowspan="2">Polarity</td><td colspan="5">Lane Mapping</td></tr>
<tr><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>Reverse</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>Obverse</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
</table></td></tr>
<tr><td>DSWAP[1:0]</td><td>I</td><td>Digital (VDDI)</td><td>MIPI data lane swap pin.
<table>
<tr><td colspan="3">External HW pin</td><td colspan="5">MIPI Lane Configuration</td></tr>
<tr><td>PSWAP</td><td colspan="2">DSWAP[1:0]</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
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<tr><td>0</td><td>1</td><td>0</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
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<tr><td>1</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
</table></td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Digital (VDDI)</td><td>Interface selection pin.
<table>
<tr><td colspan="3">IM[2:0]</td><td>Interface status</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI 4 Lane</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>BOOSTM[1:0]</td><td>I</td><td>Digital (VDDI)</td><td>External power mode selection pin.
<table>
<tr><td colspan="2">BOOSTM[1:0]</td><td>Power mode status</td></tr>
<tr><td>0</td><td>0</td><td>External AVDD & External AVEE</td></tr>
<tr><td colspan="2">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>FTE</td><td>O</td><td>Digital (VDDI)</td><td>Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command.
When this pin is not activated (FTE function OFF), this pin is VSS level.</td></tr>
<tr><td>FTE1</td><td>O</td><td>Digital (VDDI)</td><td>Output pin for scan line signal, activated by S/W command.
When this pin is not activated (FTE1 function OFF), this pin is VSS level.</td></tr>
<tr><td>VSOUT</td><td>O</td><td>Digital (VDDI)</td><td>Internal Vsync signal.
When this pin is not activated (VSOUT function OFF), this pin is VSS level.</td></tr>
<tr><td>HSOUT</td><td>O</td><td>Digital (VDDI)</td><td>Internal Hsync signal.
When this pin is not activated (HSOUT function OFF), this pin is VSS level.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>Digital (VDDI)</td><td>LCD backlight PWM control.</td></tr>
<tr><td colspan="4">MIPI-DSI Interface Input Signals</td></tr>
</table>

CLKP/N	I	MIPI (LVDSVDD)	MIPI-DSI CLOCK differential signal input pins. If not used, Please connect to LVDSVSS.
D0P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI Data differential signal input pins. If not used, Please connect to LVDSVSS.
D1P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI Data differential signal input pins. If not used, Please connect to LVDSVSS.
D2P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI Data differential signal input pins. If not used, Please connect to LVDSVSS.
D3P/N	I/O	MIPI (LVDSVDD)	MIPI-DSI Data differential signal input pins. If not used, Please connect to LVDSVSS.
Test Pad			
DBIST	I	Digital (VDDI)	Test Signal, not accessible to user. Fix to GND or leave it open. IC internal pull low
TESTIN[2:0]	I	Digital (VDDI)	Test Mode control signal, Test pins. Fix to GND or leave it open. IC internal pull low
TEST[19:0]	I/O	Digital (VDDI)	Test Signal, not accessible to user. Must be left open.
EN4PWR	I	Digital (VDDI)	Test Signal, not accessible to user. Please connected to GND.
DE	I	Digital (VDDI)	Data enable signal. For test only. Fix to GND or leave it open
VSYNC	I	Digital (VDDI)	Vertical synchronization signal. Fix to GND or leave it open.
HSYNC	I	Digital (VDDI)	Horizontal synchronization signal. Fix to GND or leave it open.
DCX	I	Digital (VDDI)	Display data / Command selection pin in parallel interface 0 : Command data 1 : Display data Fix to GND or leave it open
RDX	I	Digital (VDDI)	Display data / Command selection pin in parallel interface Fix to VDDI or leave it open
CSX	I	Digital (VDDI)	Chip select signal. For SPI mode test only Low: chip can be accessed (In SPI mode); High: chip cannot be accessed (In SPI mode). Fix to VDDI or leave it open
WRX_SCL	I	Digital (VDDI)	Clock input for SPI mode test only Fix to GND or leave it open
SDI	I	Digital (VDDI)	Input for SPI mode test only Fix to GND or leave it open

SDO	O	Digital (VDDI)	Output for SPI mode test only Leave it open if not used.
TESTDUM	I	Digital (VDDI)	Test Mode control signal, Test pins. Fix to GND or leave it open. IC internal pull low
TOUT[1:0]	O	Digital (VDDI)	Test Signal, not accessible to user. Must be left open.
VSSDUM	-	-	Dummy pin. Please keep it open.
VREFM	-	-	Dummy pin. Please keep it open.
COGTEST	-	-	Dummy pin. Please keep it open.
C41P/C41M	-	-	Dummy pin. Please keep it open.
DUMMY[4:1]	-	-	Dummy pin. Please connected to GND.
DUMMY	-	-	Dummy pin. Please keep it open.
CGDUM_R[2:1]	-	-	Dummy pin. Please keep it open.
CGDUM_L[2:1]	-	-	Dummy pin. Please keep it open.
Driving Pad			
S[1080:1]	O	Analog (AVDD)	Source output
SL1	O	Analog (AVDD)	Left dummy source pin.
SR1	O	Analog (AVDD)	Right dummy source pin.
CGOUT_L[16:1]	O	Analog (VGH/VGL)	GOA Output
CGOUT_R[16:1]	O	Analog (VGH/VGL)	GOA Output
VCOMDC	O	Analog (VCL)	VCOM output

6 MIPI-DSI Interface

6.1 General Description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface level : low level communication
- Packet level : High level communication

6.2 Interface level Communication

6.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both of clock lane and data lane 0 can be driven at Low Power (LP) or High Speed (HS) mode. Data lane 1/2/3 can be driven at High Speed mode only.

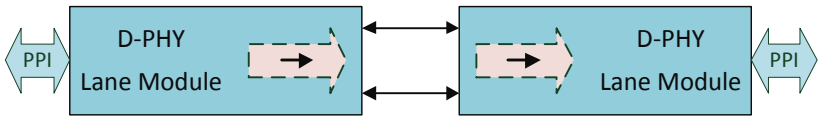
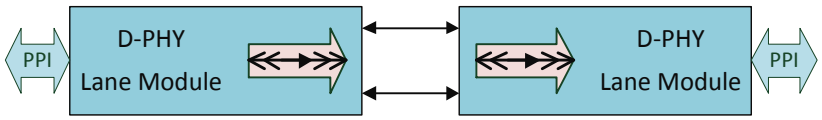
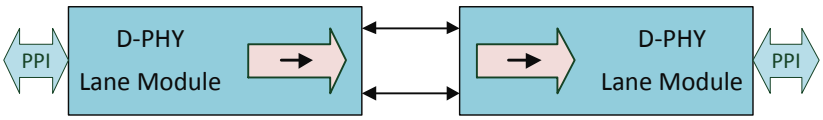
Lane type	Lane support mode	MPU(Host) XUA001 (Slave)
Clock Lane	Unidirectional lane ▪ High-speed clock only ▪ Simplified Escape Mode (ULPS Only)	
Data Lane 0	Bidirectional lane ▪ Forward high-speed only ▪ Bi-directional Escape Mode ▪ Bi-direction LPDT	
Data Lane 1/2/3	Unidirectional lane ▪ Forward high-speed only ▪ Simplified Escape Mode (ULPS Only)	

Figure 1. Lane Types and Support Mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High-Speed(HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Figure 2. High-speed and low-power lane pair state description

6.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences. The principal flow chart of the different clock lanes power modes is illustrated below.

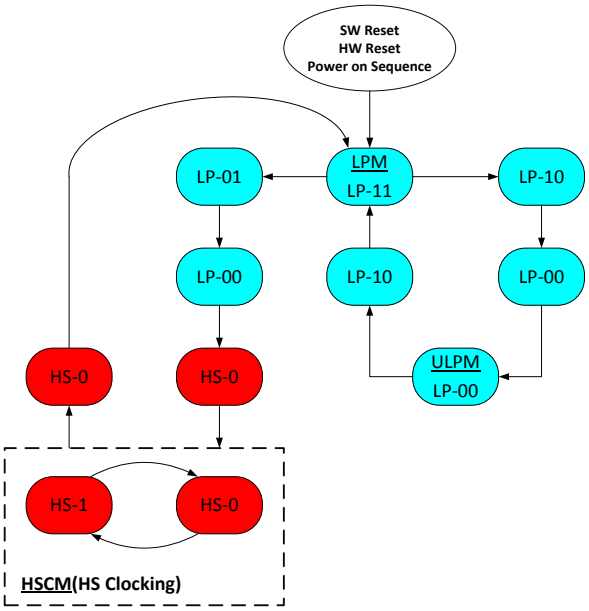


Figure 3. Clock lanes power mode

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

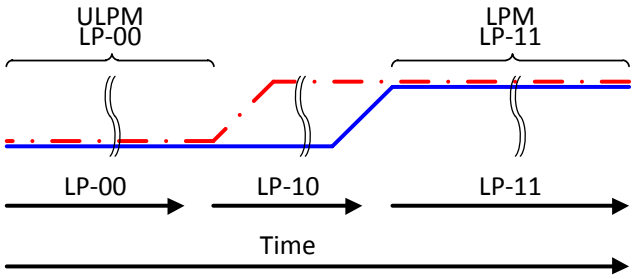


Figure 4. From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

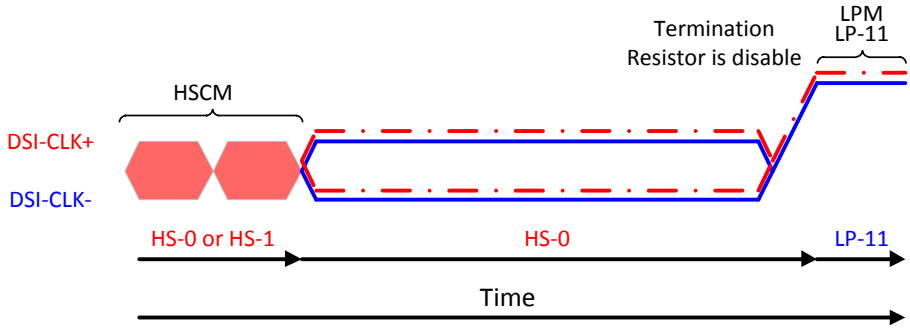


Figure 5. From HSCM to LPM

All three mode changes are illustrated a flow chart below.

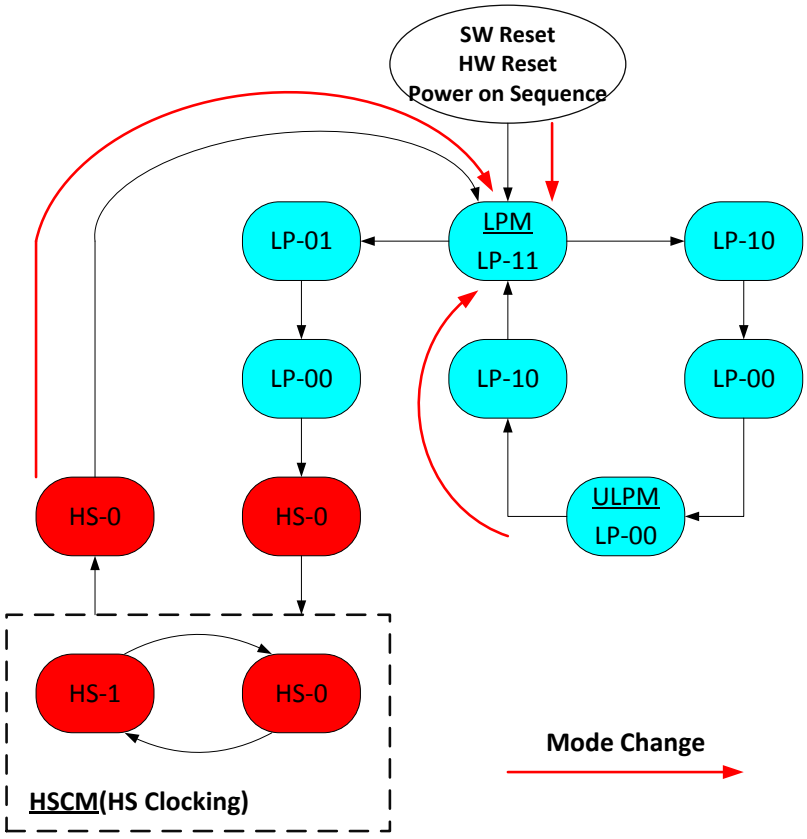


Figure 6. All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

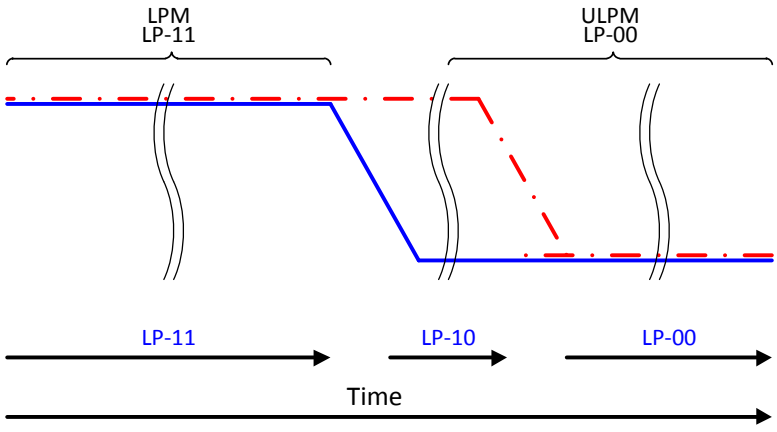


Figure 7. From LPM to ULPM

The mode change is also illustrated below:

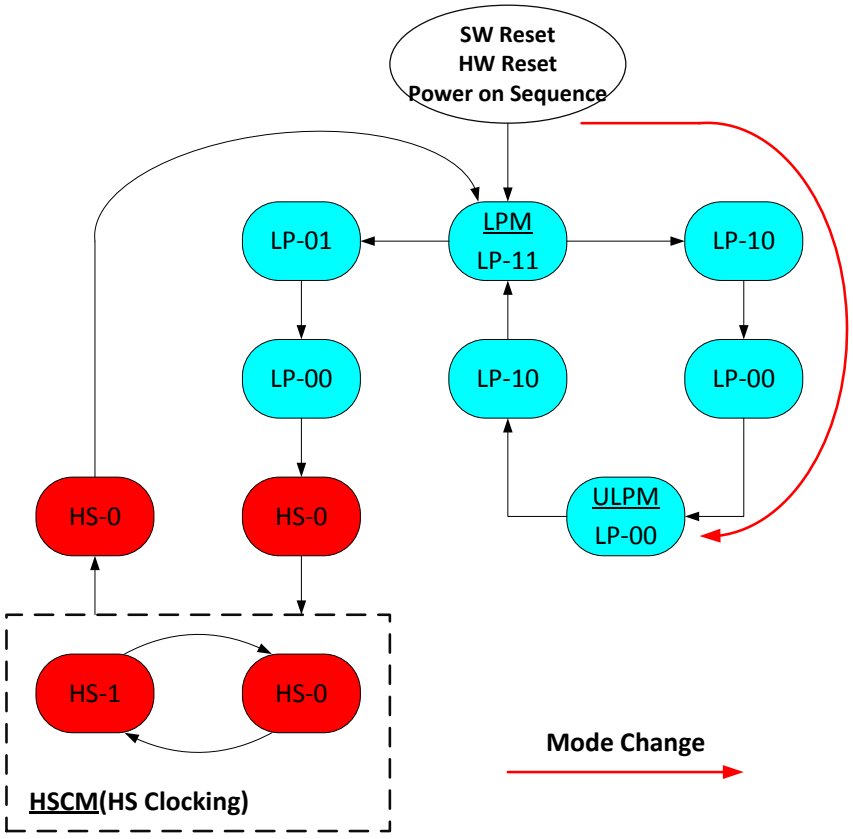


Figure 8. The mode change from LPM to ULPM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

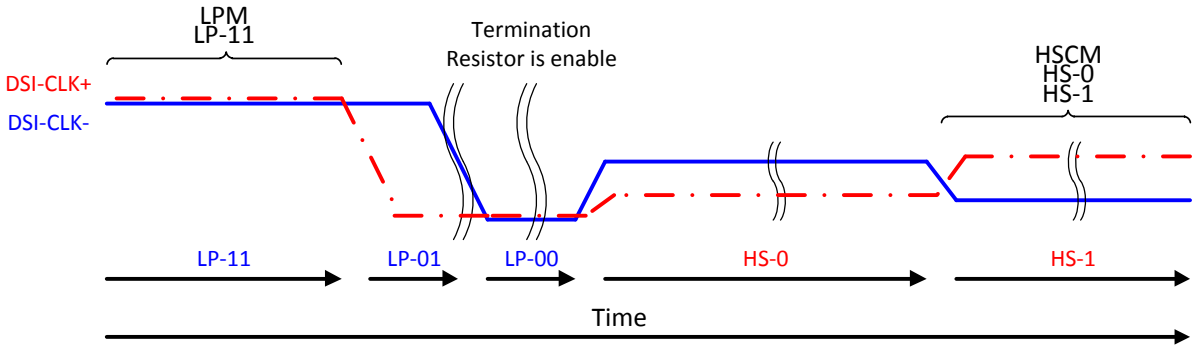


Figure 9. From LPM to HSCM

The mode change is also illustrated below:

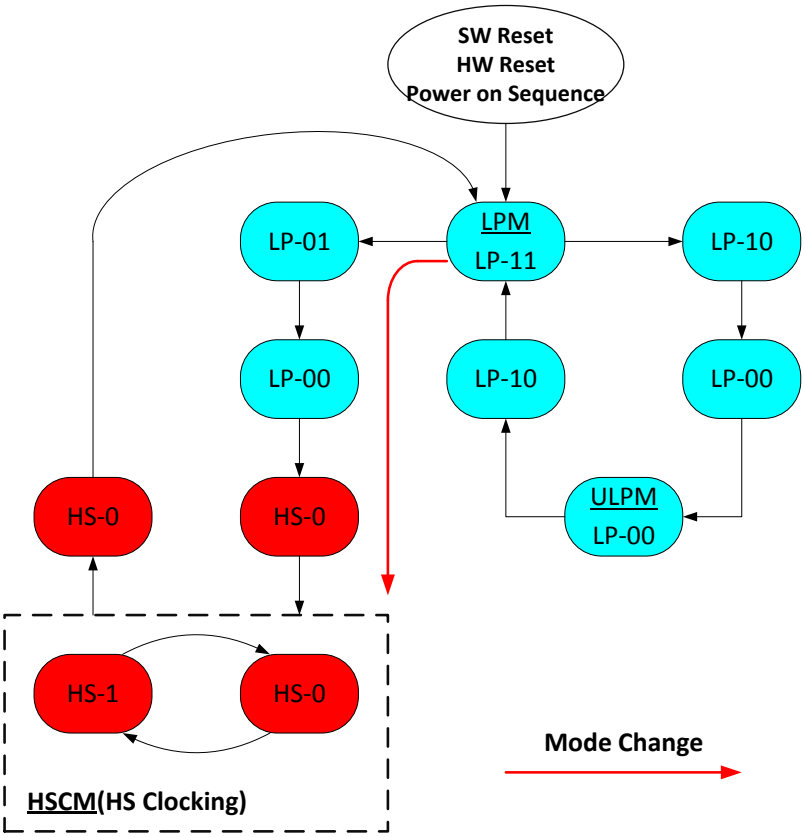
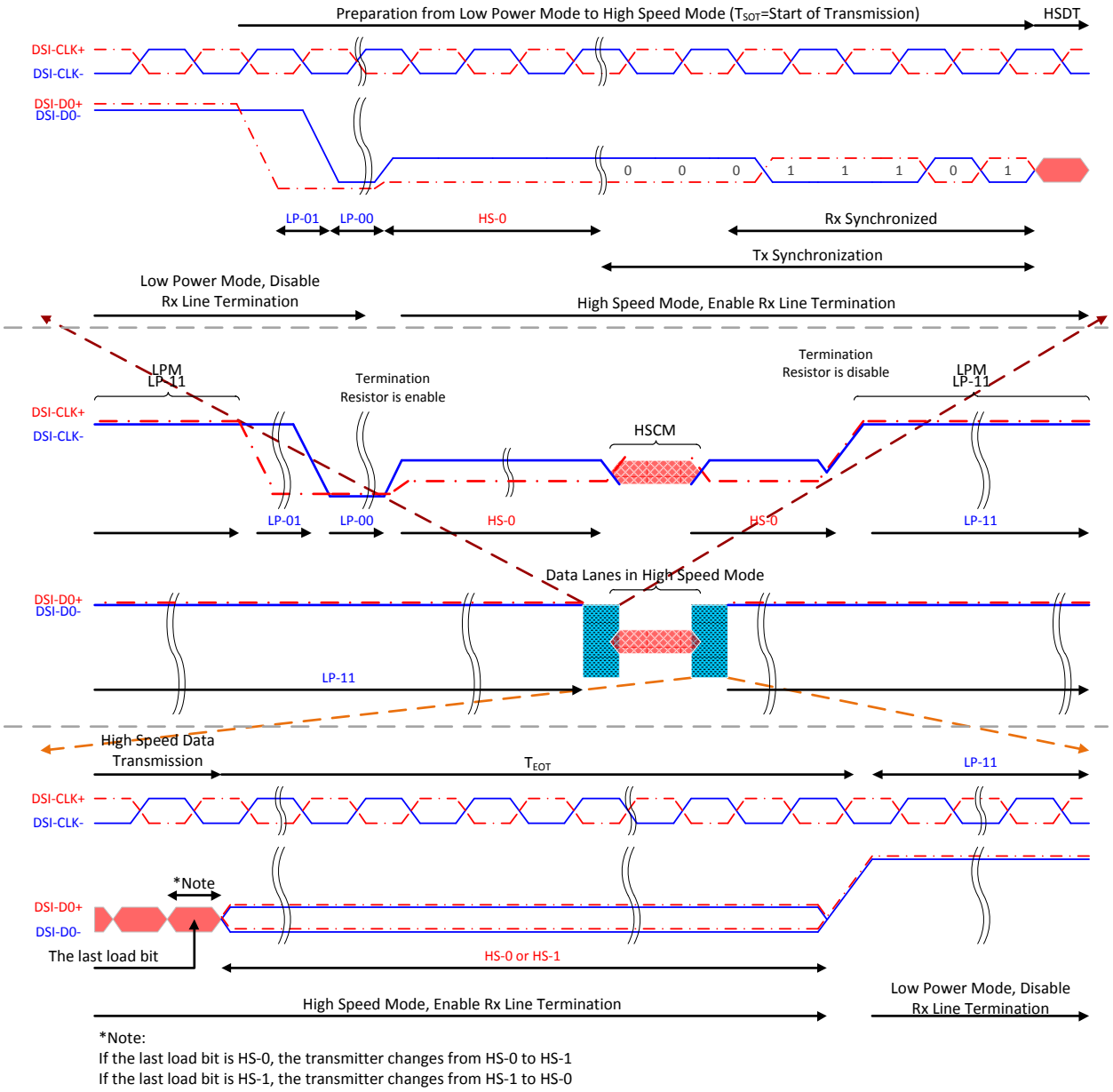


Figure 10. Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



*Note:
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

Figure 11. High speed clock burst

6.2.3 DSI data lanes

General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 => LP-10 => LP-00 => LP-01 => LP-00	LP-00 => LP-10 => LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 => LP-01 => LP-00 => HS-0	(HS-0 or HS-1) => LP-11
Bus Turnaround Request	LP-11 => LP-10 => LP-00 => LP-10 => LP-00	High-Z, Note

Figure 12. Entering and leaving sequences

Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction. The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. All currently available Escape mode commands and actions are list below.

- Send or receive “Low-Power Data Transmission” (LPDT)
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU.
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If

the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state. For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

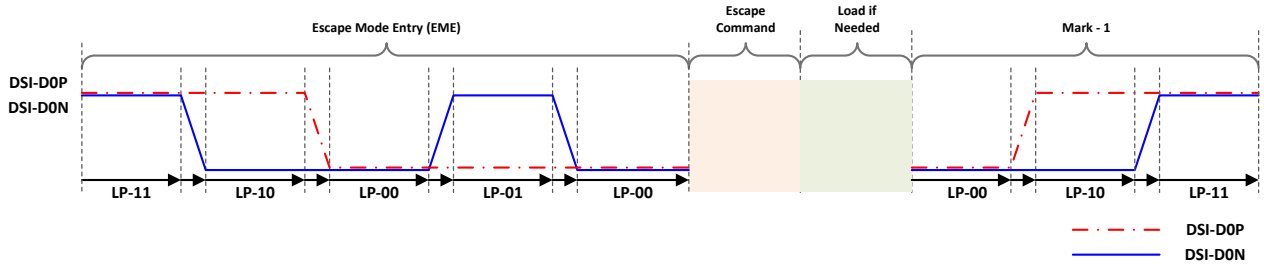


Figure 13. General Escape Mode Sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided in 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode / Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1100 0001 bin
Ultra-Low Power mode	Mode	0001 1110 bin
Remote Application Request	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Figure 14. Escape Commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape ode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU. The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
  - One or more bytes
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

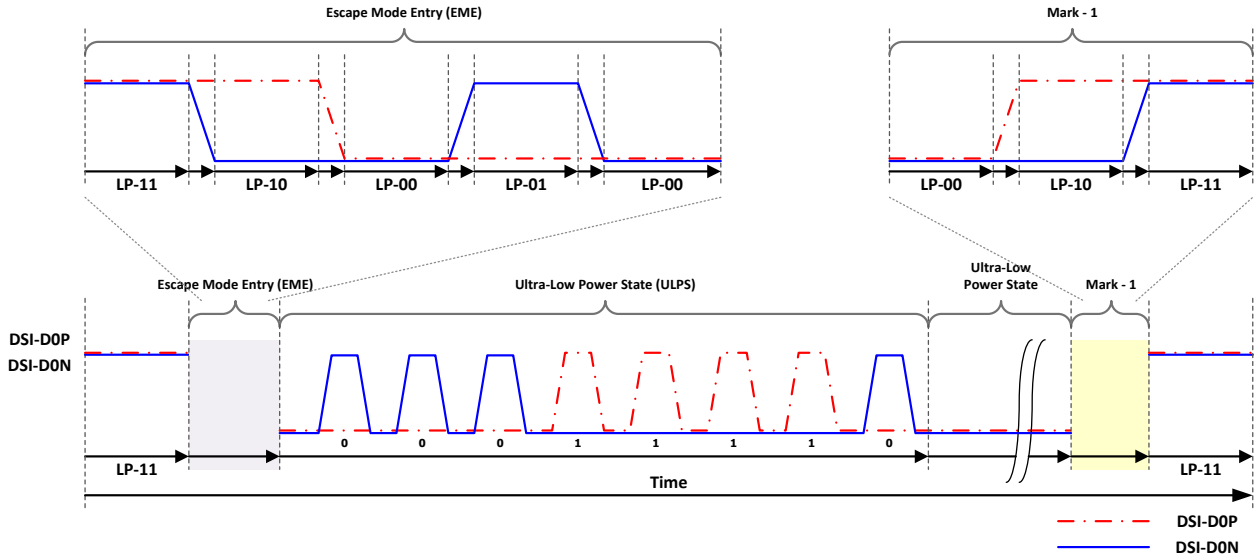


Figure 15. Low-Power Data Transmission

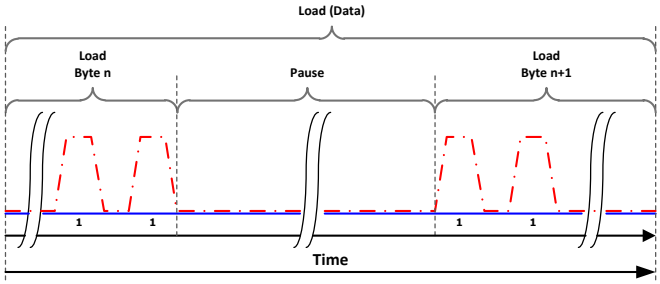


Figure 16. Pause (Example)

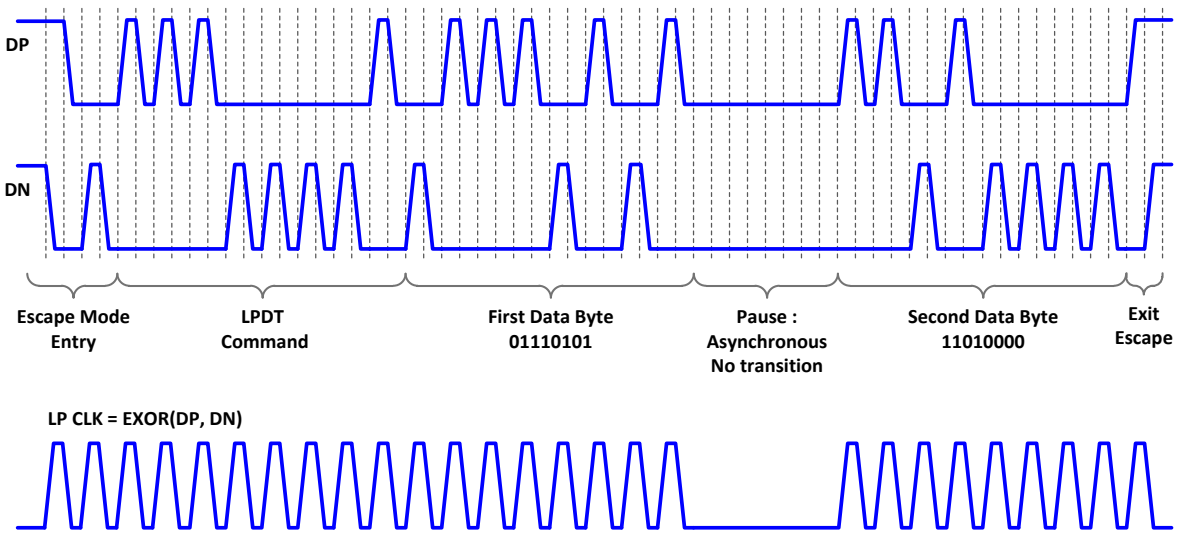


Figure 17. Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode. The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

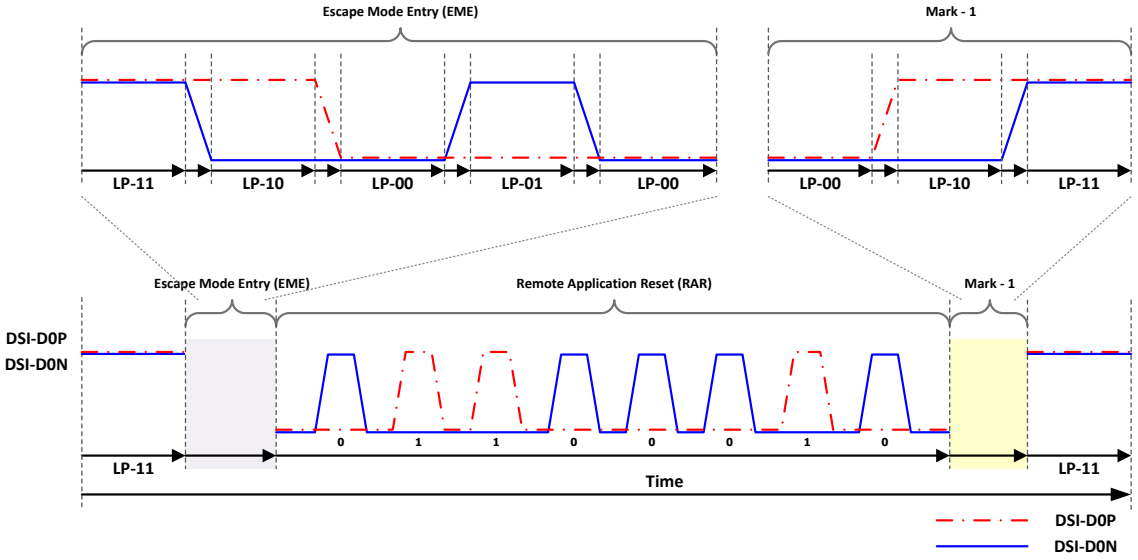


Figure 18. Ultra-Low Power State (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

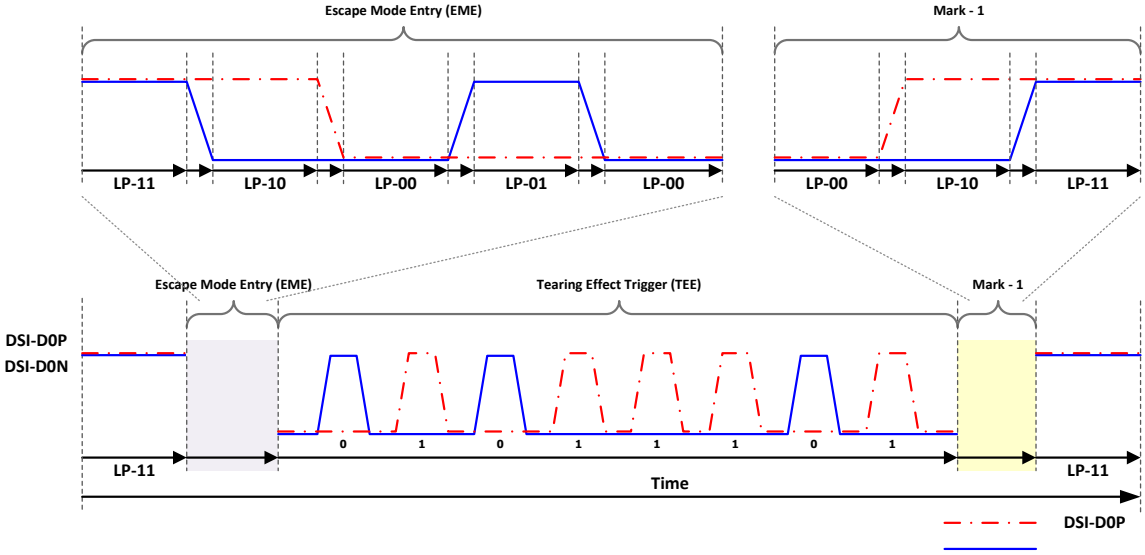


Figure 19. Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE). The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

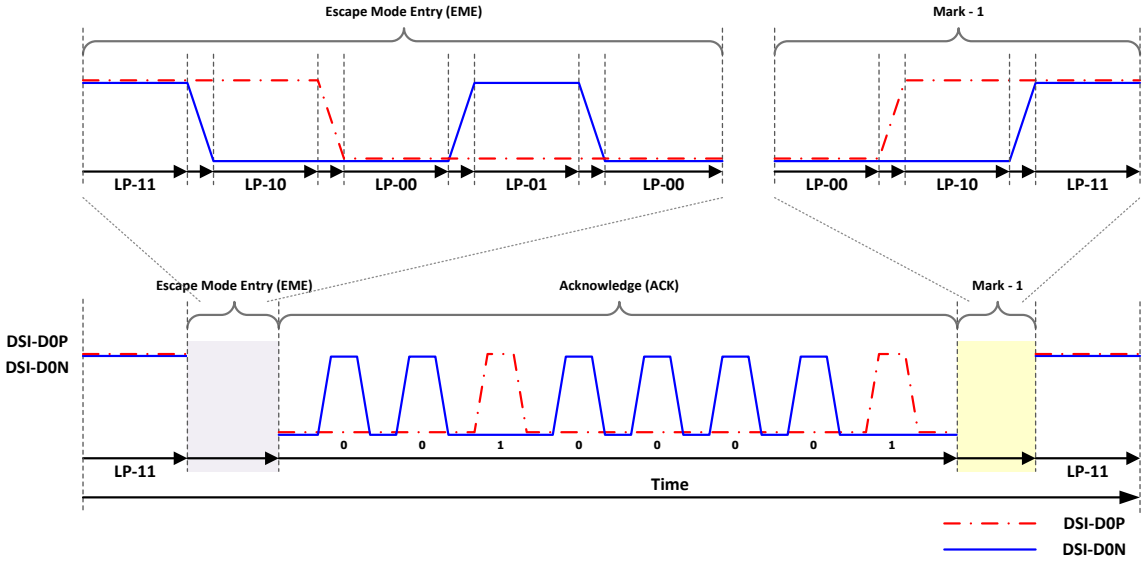


Figure 20. Tearing Effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

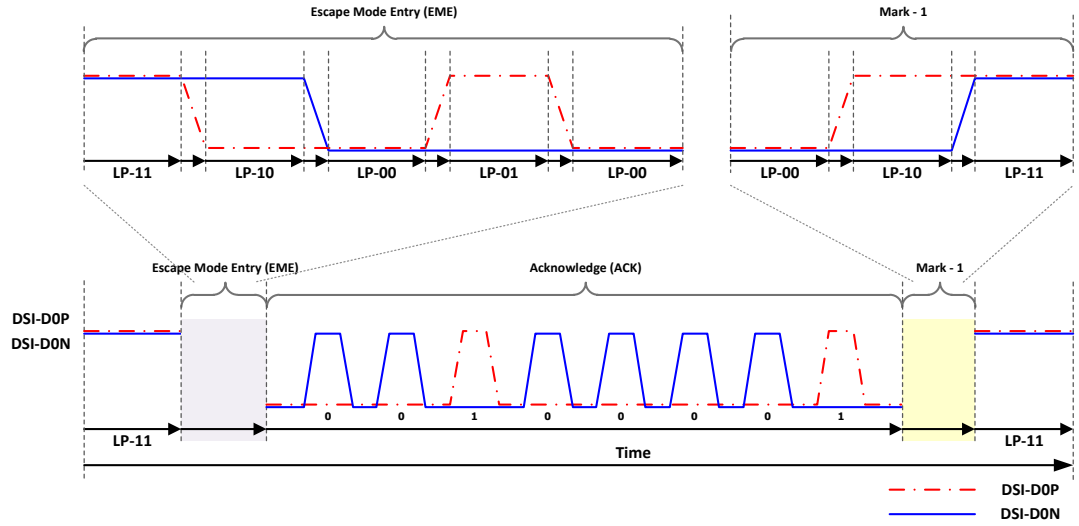


Figure 21. Acknowledgement (ACK)

High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (Tsot of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”. Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

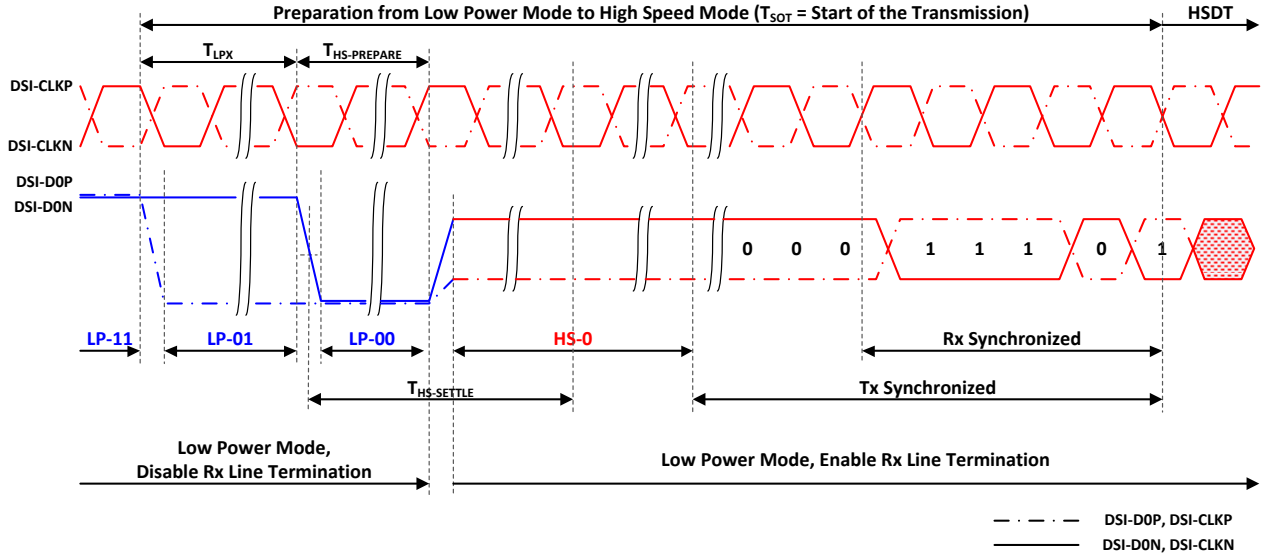


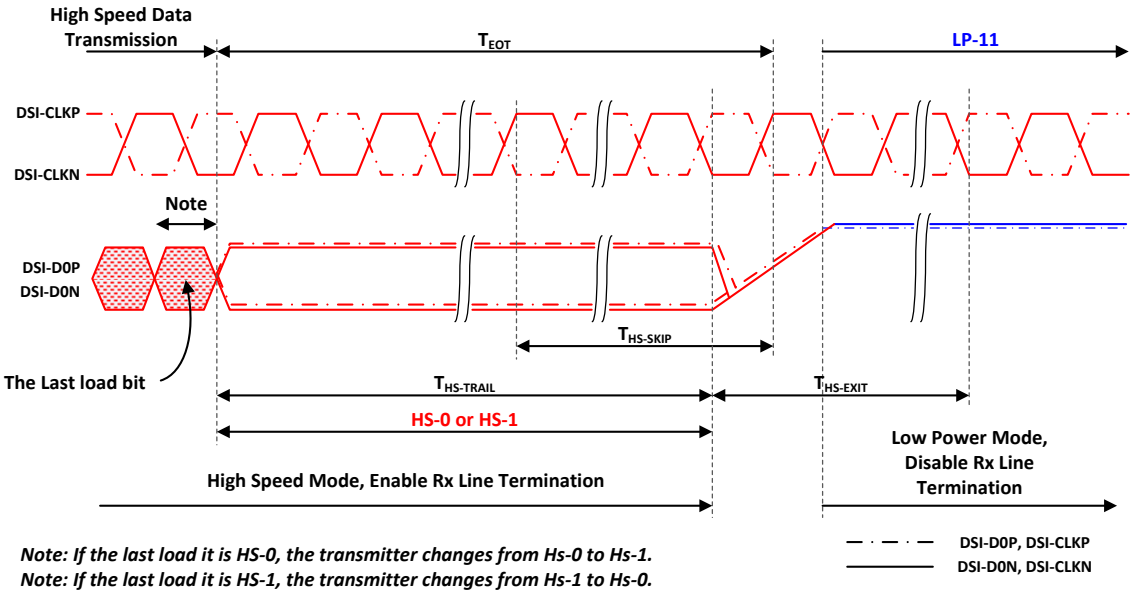
Figure 22. T_{SOT} of HSDT

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”. Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below:



Note: If the last load it is HS-0, the transmitter changes from Hs-0 to Hs-1.
Note: If the last load it is HS-1, the transmitter changes from Hs-1 to Hs-0.

Figure 23. T_{EoT} of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LgP) or Short (SP) packets. These packets are defined on chapter “Short Packet (SP) and Long Packet (LgP) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below:

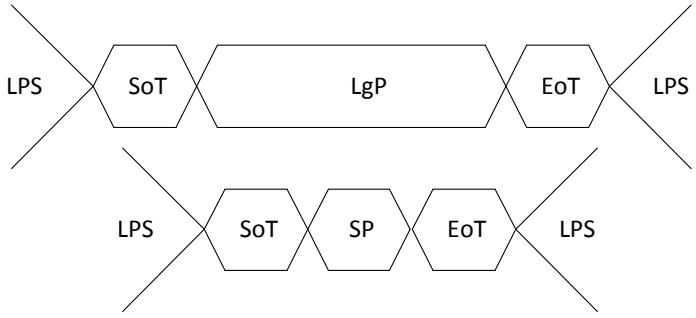


Figure 24 Single Packet in HSDT

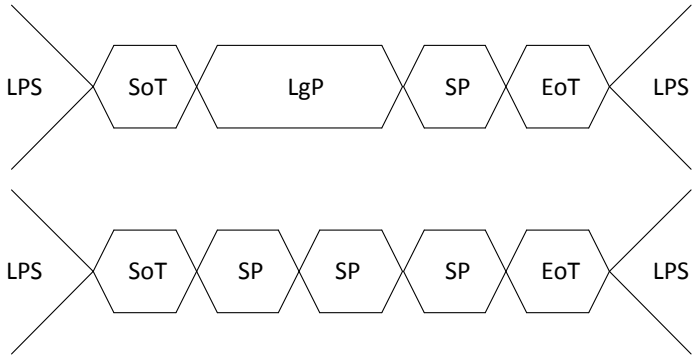


Figure 25. Multiple Packets in HSDT

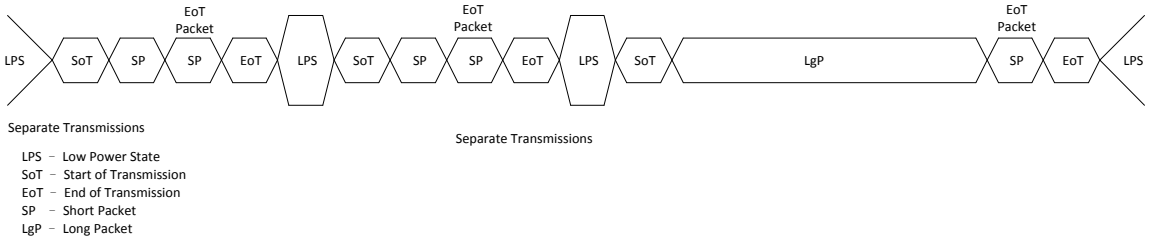


Figure 26. Packets with EoT Package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SoT	Start of the Transmission
LgP	Long Packet
SP	Short Packet
EoT	End of the Transmission

Figure 27. Abbreviation Table

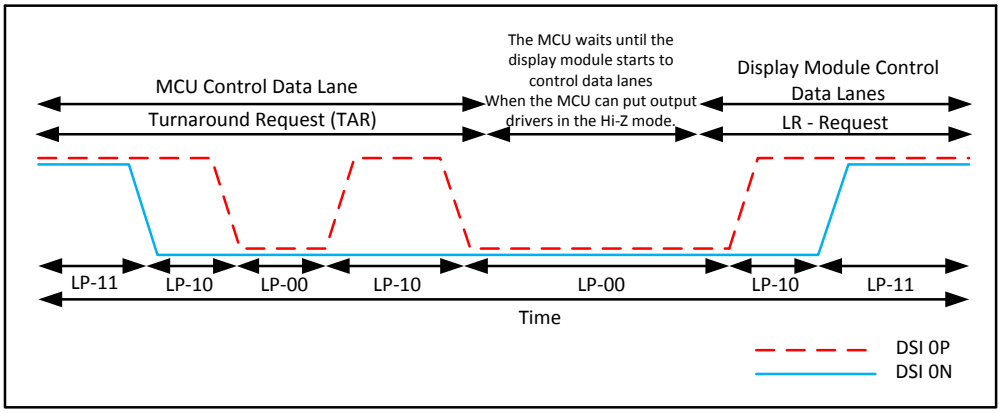
Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module. The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below:



Bus Turnaround (BTA)

Figure 28. Bus Turnaround Procedure

Two Data-lane High Speed Transmission

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, one lane may run out of data before the other. Therefore, the lane management layer, as it buffers up the final set of less-than-2 bytes, de-asserts its “valid data” signal into all lanes for which there’s no further data.

Although all lanes start simultaneously with parallel SoTs, each lane operates independently and may complete the HS transmission before the other lane, sending an EoT one cycle (byte) earlier.

The two PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission.

The figure as below shows the way a HS transmission can terminate for two data-lane HS transmission.

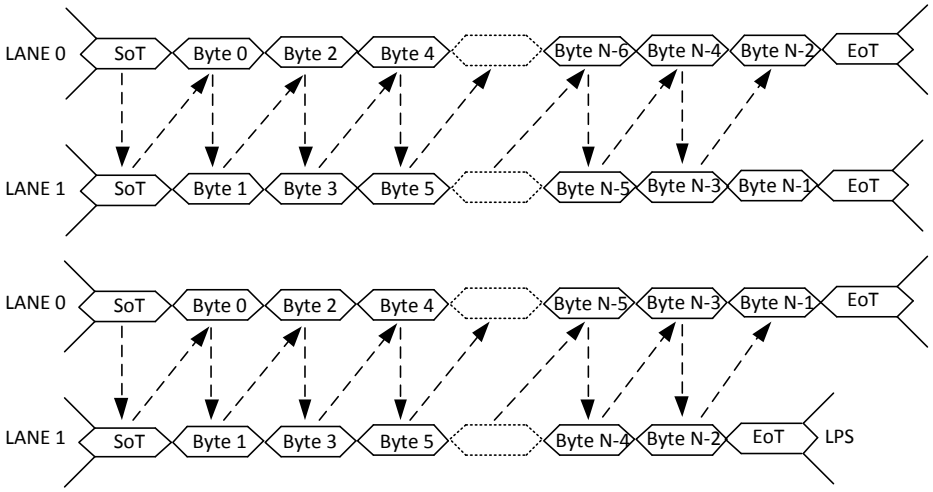


Figure 29. Two Data-Lane HS Transmission Example

Three Data-lane High Speed Transmission

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission.

Below Figure illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

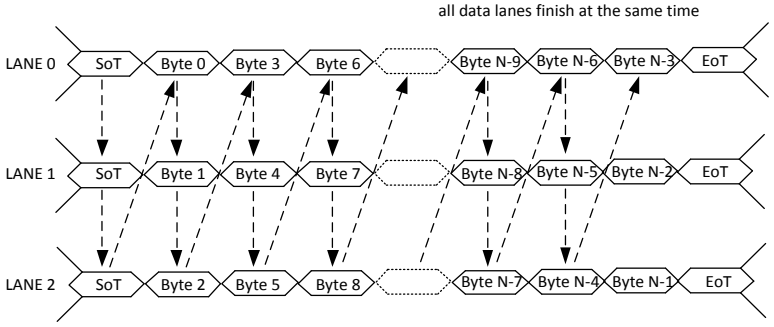


Figure 30. Number of Transmitted Bytes, N, an Integer Multiple of Number of Lanes

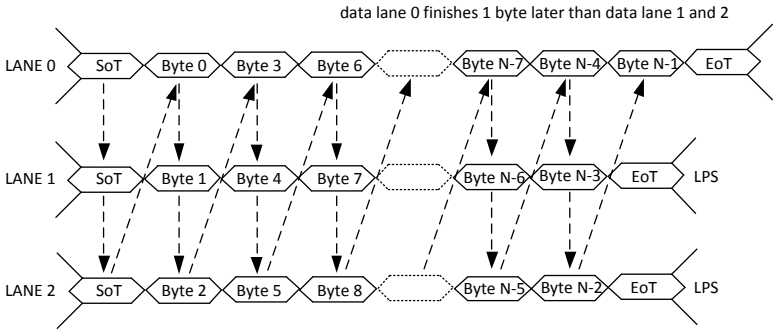


Figure 31. Number of Transmitted Bytes, N, NOT an Integer Multiple of Number of Lanes (Example 1)

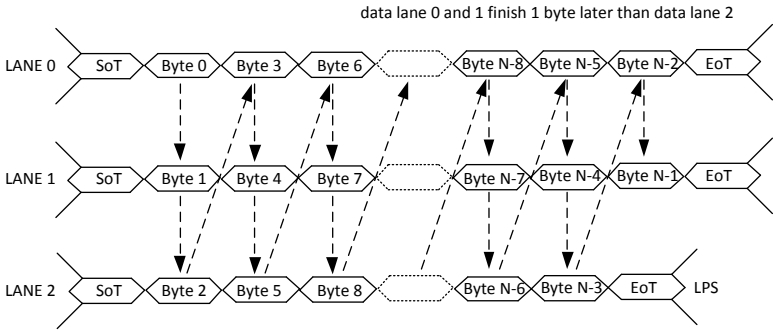


Figure 32. Number of Transmitted Bytes, N, NOT an Integer Multiple of Number of Lanes (Example 2)

6.2.4 Packet Level Communication

Short Packet (SP) and Long Packet (LgP) structures

Short Packet (SP) and Long Packet (LgP) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

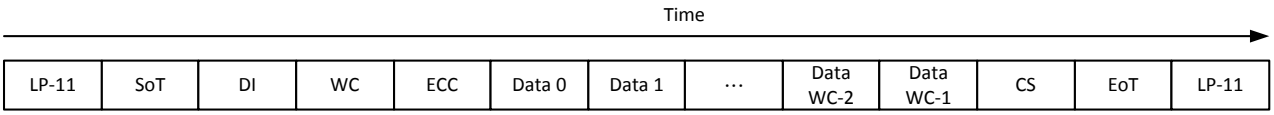
The lengths of the packets are

- Short Packet (SP): 4 bytes
- Long Packet (LgP): From 6 to 65,541 bytes

The type (SP or LgP) of the packet can be recognized from their package headers (PH).

LP-11 : low power stop state
SoT : Start of transmission
DI : Data Identification(8 bit)
Data 0 : Packet Data (8 bit)
Data 1 : Packet Data (8 bit)
Ecc : Error Correction Code (8bit)
EoT : End of Transmission

Figure 33. Short Packet Structure



LP-11 : low power stop state
SoT : Start of transmission
DI : Data Identification(8 bit)
WC : Word Count (16 bit)
Ecc : Error Correction Code (8bit)
Data 0 ~ Data WC-1 : Packet Data (0 ~ 65536 bytes)
CS : Checksum (16 bit) = Packet Footer (PF)
EoT : End of Transmission

Figure 34. Long packet structure

Note: Short Packet (SP) Structure" and Long Packet (LgP) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 => SoT => SP => LgP => SP => SP => EoT => LP-11
- LP-11 => SoT => SP => SP => SP => EoT => LP-11
- LP-11 => SoT => LgP => LgP => LgP => EoT => LP-11

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure 6.2.4.1.3 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

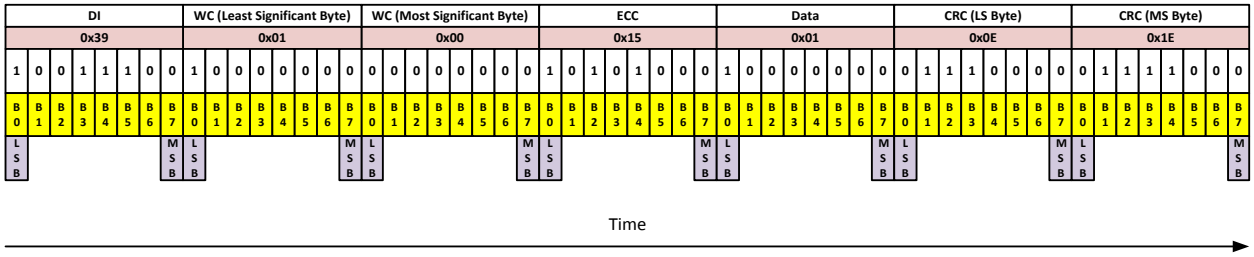


Figure 35. Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

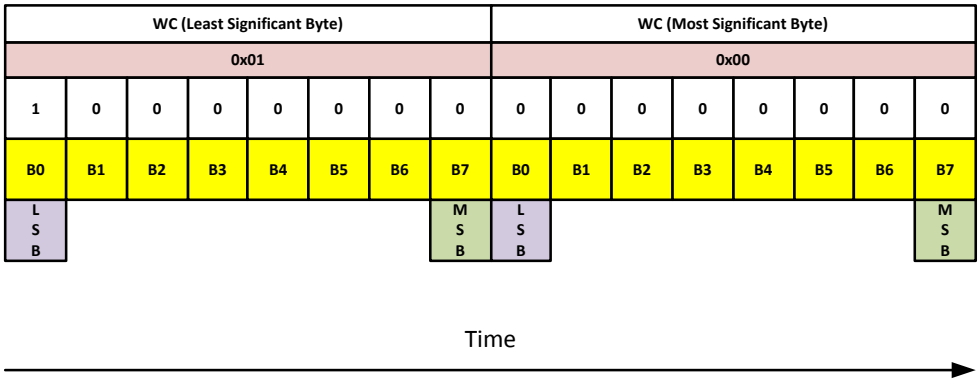


Figure 36. Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SP) or Long Packet (LgP).

Short Packet (SP):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SP)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

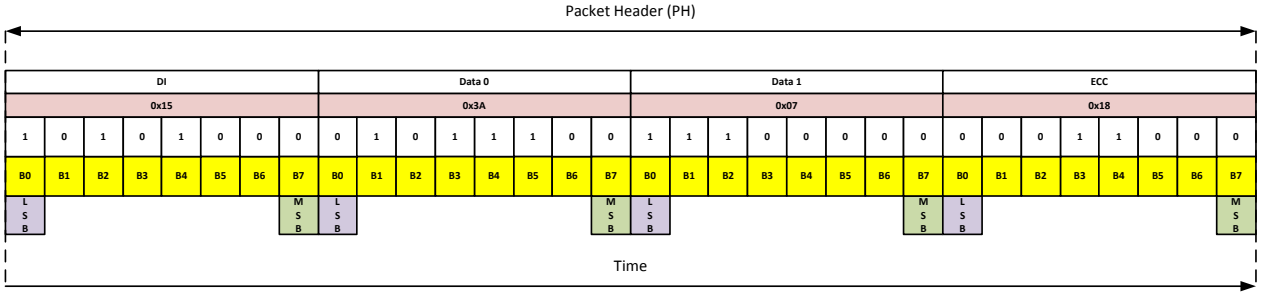


Figure 37. Packet head on short packet

Long Packet (LgP):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LgP)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

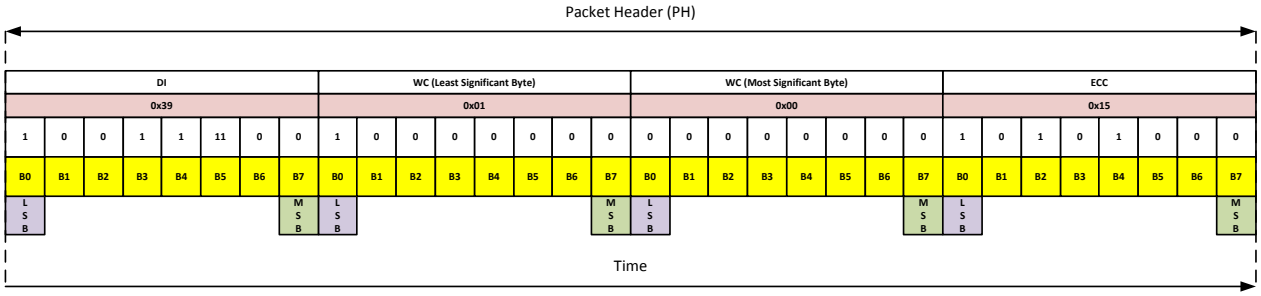


Figure 38. Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

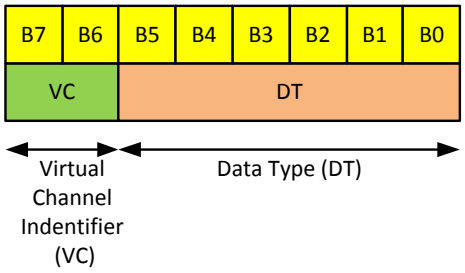


Figure 39. Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

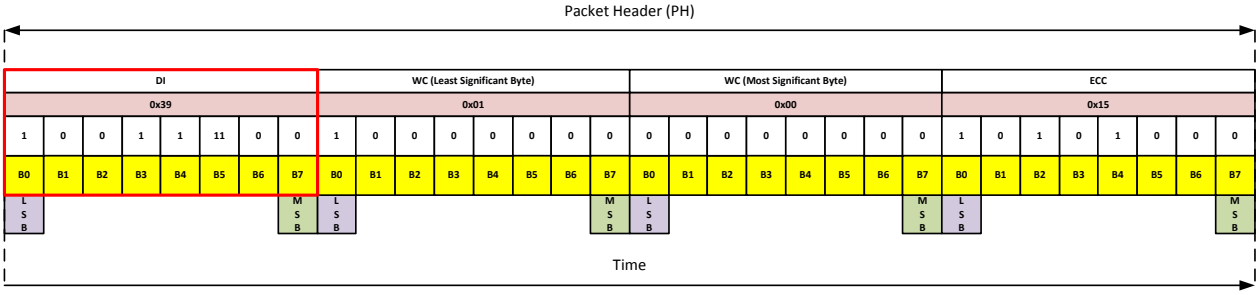


Figure 40. Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

XUA001 only support VC code=00, package with other VC code (01/10/11) will be filter out.

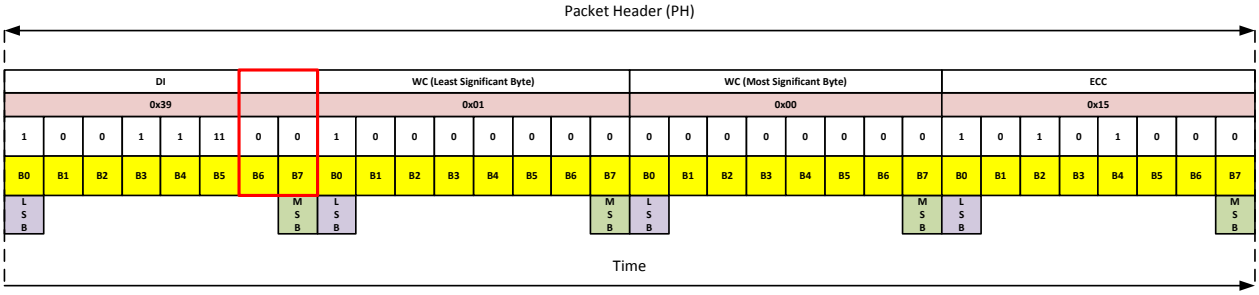


Figure 41. Virtual channel on the packet head

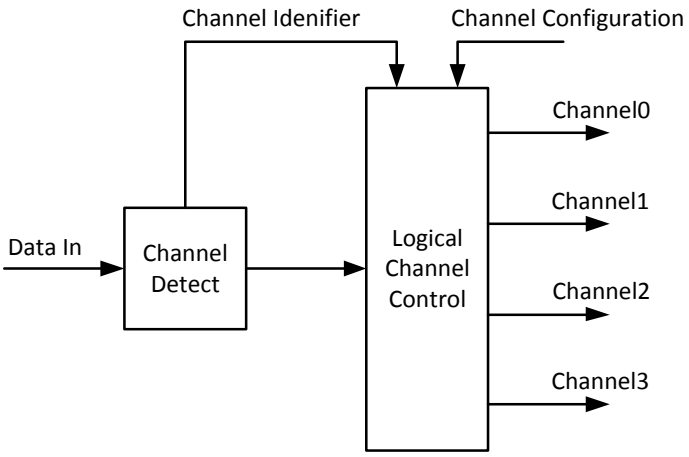


Figure 42. Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

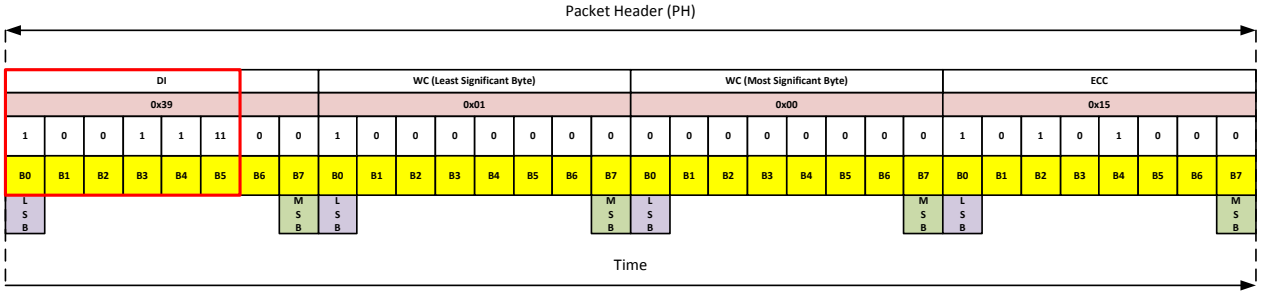


Figure 43. Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SP) or Long Packet (LgP). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display Module		
Data Type (HEX)	Data Type (Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Error, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT) packet
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	10 0010	Shut Down Peripheral Command

32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short Write, no parameters
13h	01 0011	Generic Short Write, 1 parameter
23h	10 0011	Generic Short Write, 2 parameters
04h	00 0100	Generic Short Read, no parameters
14h	01 0100	Generic Short Read, 1 parameter
24h	10 0100	Generic Short Read, 2 parameters
05h	00 0101	DCS Write, no parameters
15h	01 0101	DCS Write, 1 parameter
06h	00 0110	DCS Read, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write / Write LUT Command Packet
0Eh	00 1110	Packet Pixel Stream, 16-bit RGB, 5-6-5 Format
2Eh	10 1110	Loosely Packet Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format

Figure 44. Data type from the MCU to the display module

From the Display Module to the MCU		
Data Type (HEX)	Data Type (Binary)	Description
02h	00 0010	Acknowledge and Error Report
1Ch	01 1100	DCS Long Read Response
21h	10 0001	DCS Short Read Response, 1 byte returned
22h	10 0010	DCS Short Read Response, 2 bytes returned

Figure 45. Data type from the display module to the MCU

The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send "Generic Read" data type, XM91080A will return DCS Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SP) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SP) is wanted to send.

Packet Data (PD) of the Short Packet (SP) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SP), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

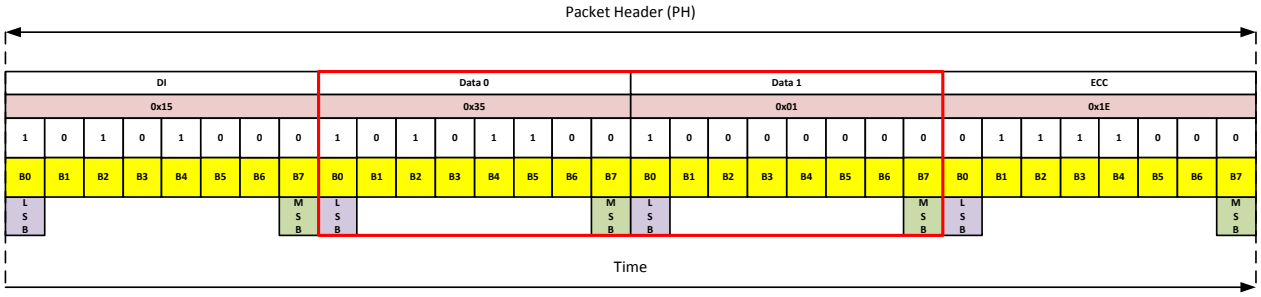


Figure 46. Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

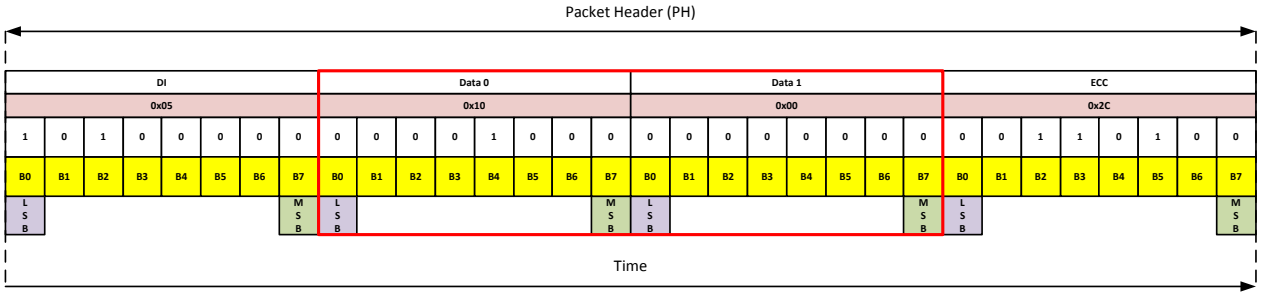


Figure 47. Packet data on the short packet, 1 byte information

Word count on the long packet

Word Count (WC) of the Long Packet (LgP) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LgP) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SP) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LgP) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

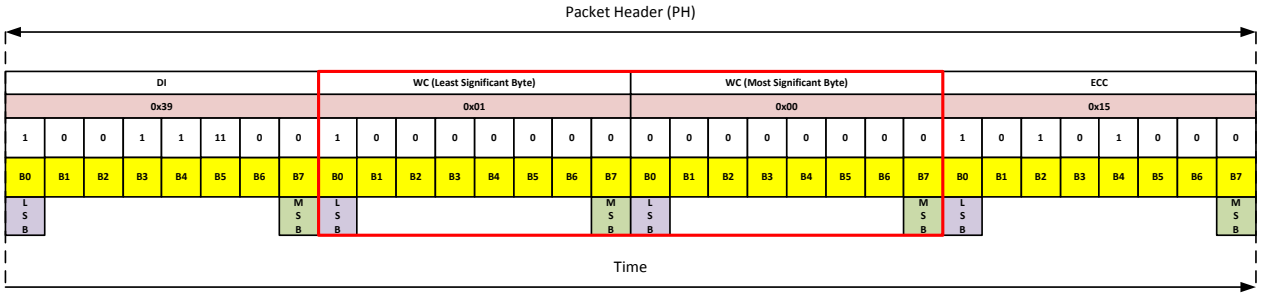


Figure 48. Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SP): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])
- Long Packet (LgP): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

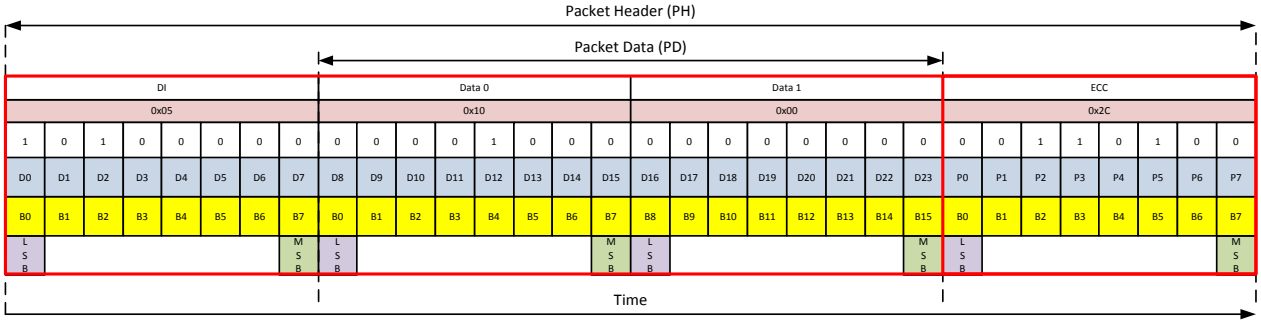


Figure 49. D[23:0] and P[7:0] on the short packet

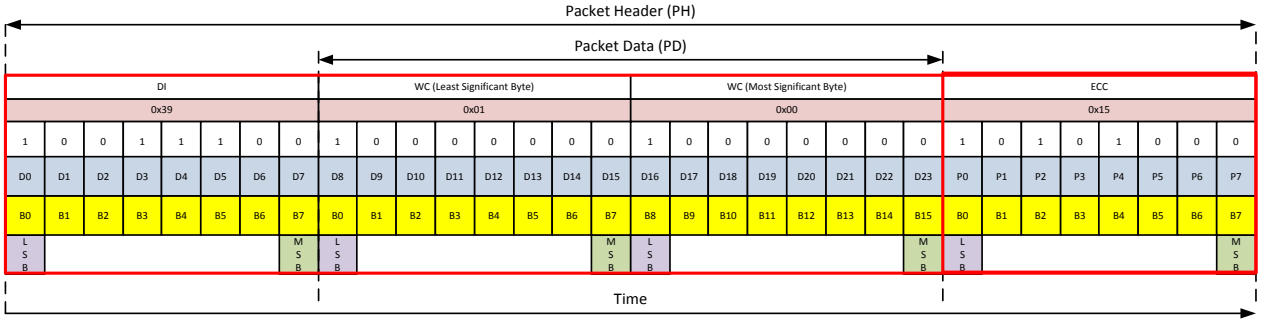


Figure 50. D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

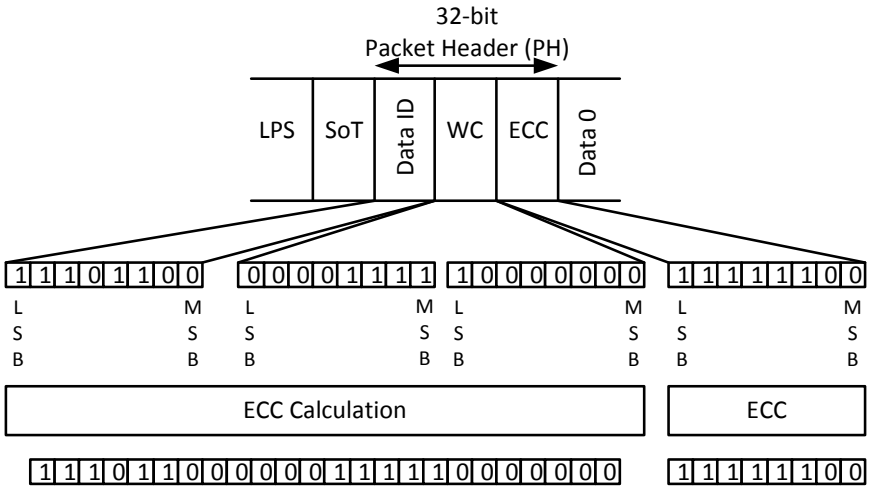


Figure 51. 24'bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LgP) is defined after the Packet Data (PD) of the Long Packet (LgP). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LgP).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

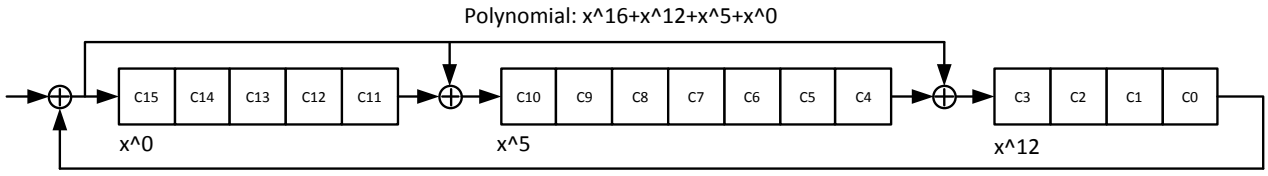


Figure 52. 16'bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

Packet Transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SP) and Long packet (LgP) as these are illustrated below.

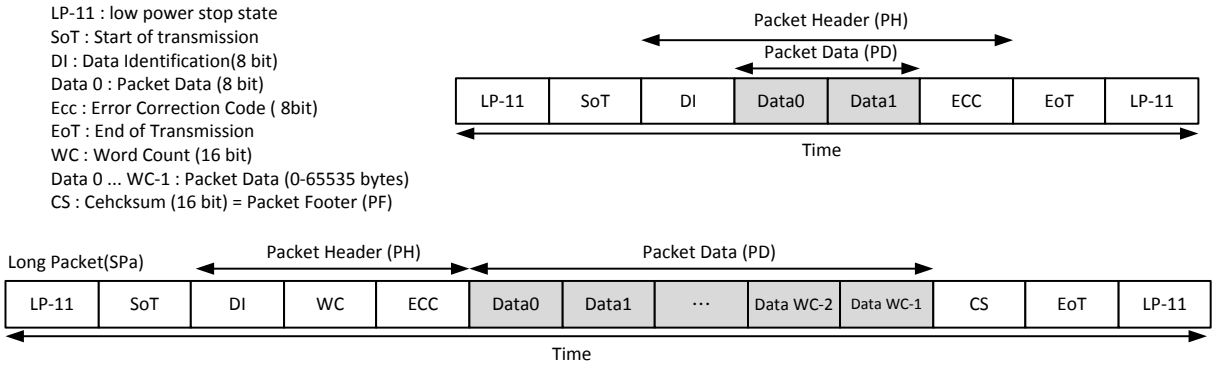


Figure 53. DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SP) or Long Packet (LgP), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

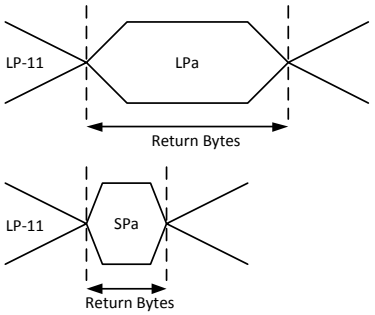


Figure 54. Return bytes on the single packet

Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SP), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1, as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected and corrected)
10	Checksum (CRC) Error (only for Long Packet (LgP))
11	DSI Date Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, set to 0 internally
15	DSI Protocol violation

Figure 55. Acknowledge with error report for long packet response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected and corrected)
10	Reserved, set to 0 internally
11	DSI Date Type (DT) Not Recognized

12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, set to 0 internally
15	DSI Protocol violation

Figure 56. Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SP) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

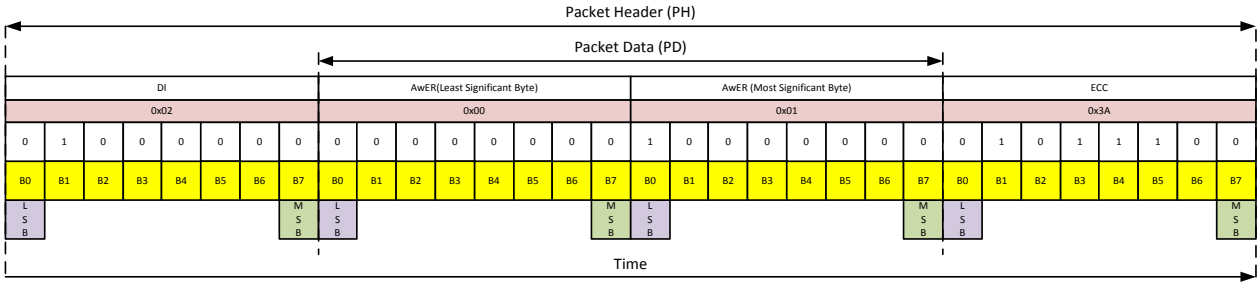


Figure 57. Acknowledge with error report – example

6.2.5 Customer-defined generic read data type format

The short packet of Data Type 24h (Generic READ, 2 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 24h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

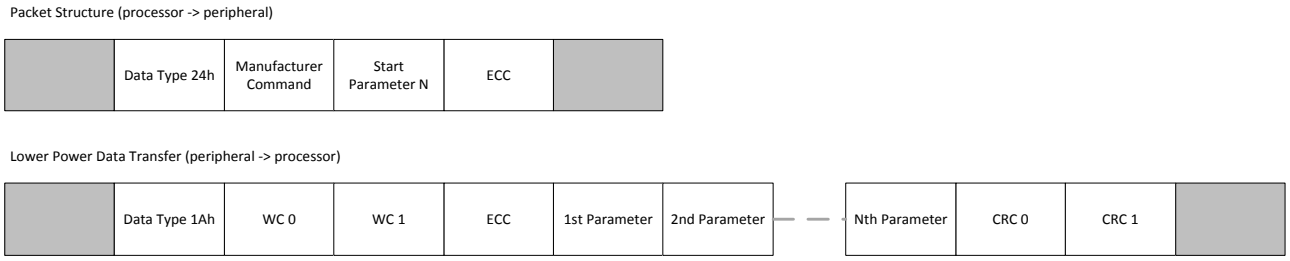
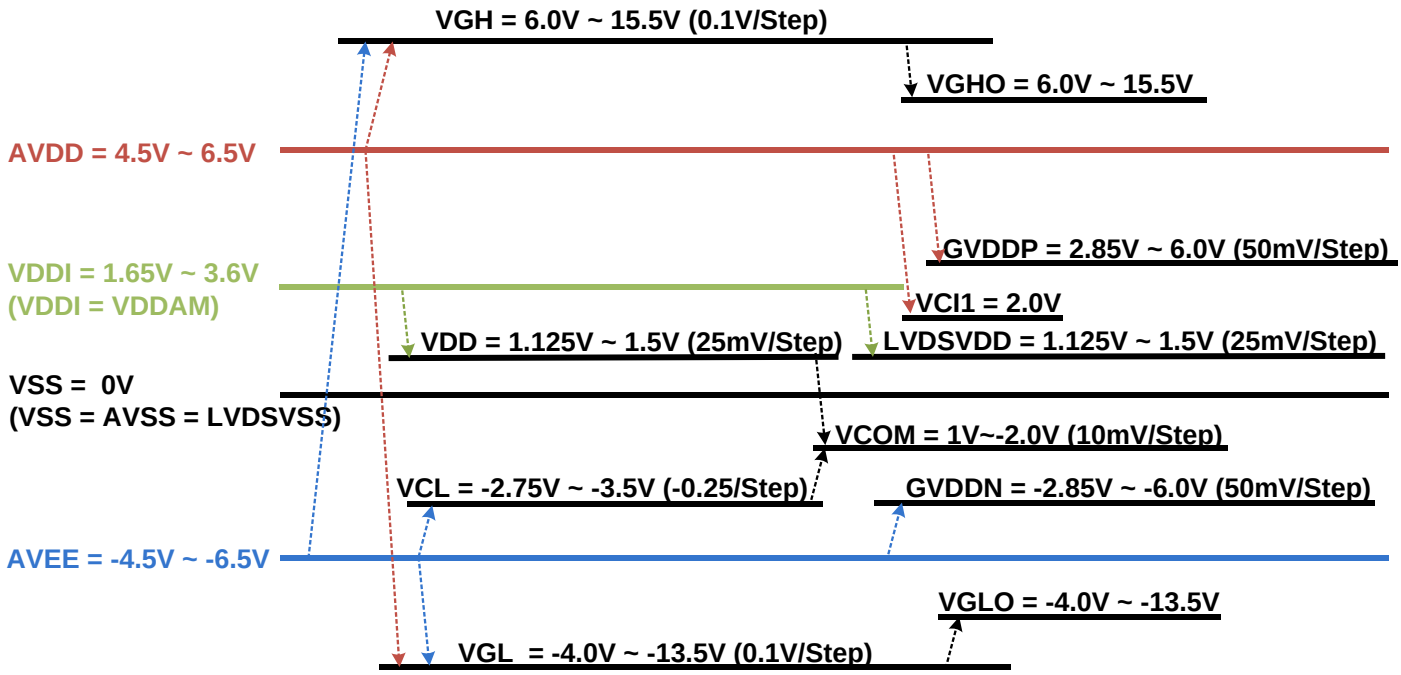


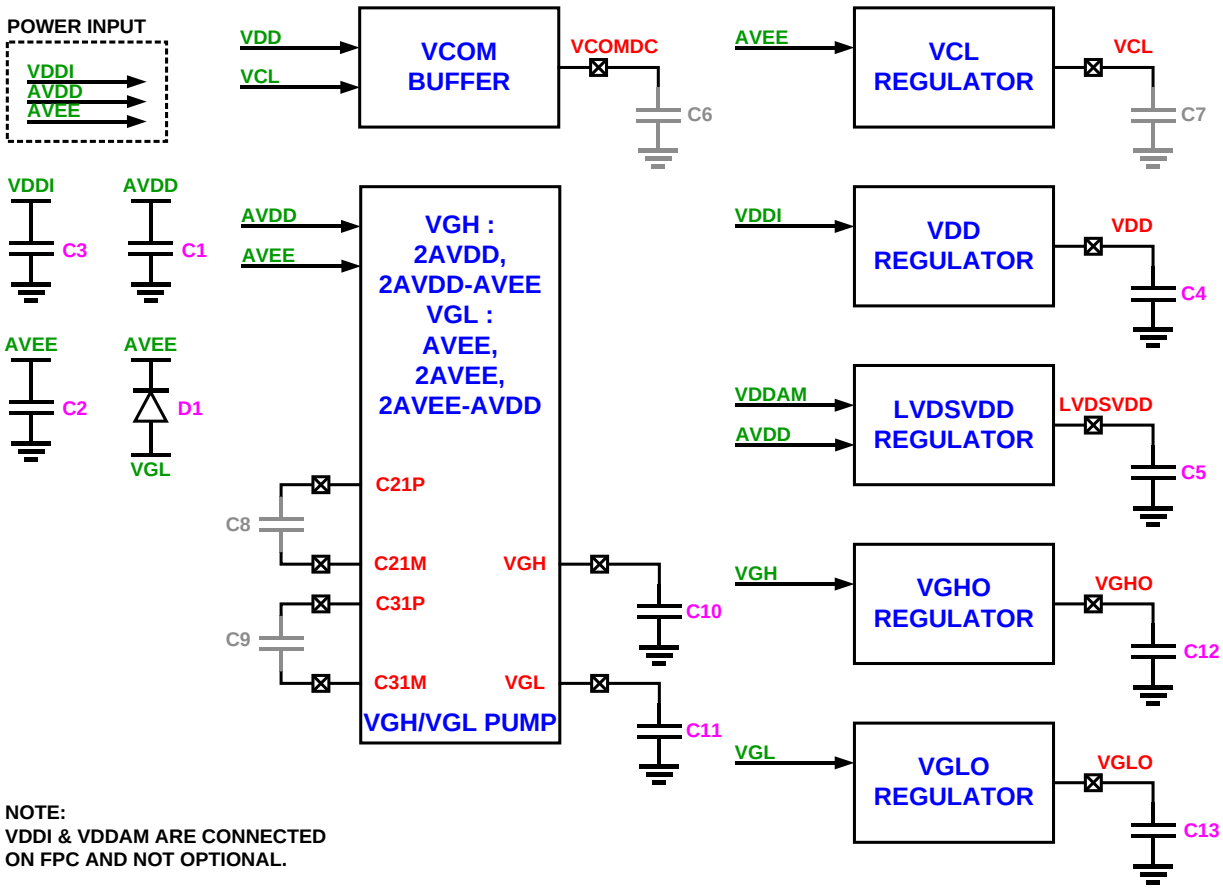
Figure 58. Generic read data type format

7 Power Supply Configuration

7.1 Power Block Diagram



7.2 Power Supply Configuration



NOTE:
VDDI & VDDAM ARE CONNECTED ON FPC AND NOT OPTIONAL.

7.3 BOM List

XM91080 BOM LISTS					
NO.	Signal Name	Components	Value	Max. Ability	Note
C1	AVDD	Capacitor	2.2 uF	10V	External AVDD Power
C2	AVEE	Capacitor	2.2 uF	10V	External AVEE Power
C3	VDDI	Capacitor	2.2 uF	4V	External I/O and Digital Power
C4	VDD	Capacitor	2.2 uF	4V	Internal Regulator Output for TCON
C5	LVDSVDD	Capacitor	2.2 uF	4V	Internal Regulator Output for HiSSi
C8	C21P/C21M	Capacitor	1 uF or 2.2 uF	16V	Flying cap. For VGH
C9	C31P/C31M	Capacitor	1 uF or 2.2 uF	16V	Flying cap. For VGL
C10	VGH	Capacitor	1 uF or 2.2 uF	16V	Charge Pump Output
C11	VGL	Capacitor	1 uF or 2.2 uF	16V	Charge Pump Output
D1	AVEE/VGL	Diode			Schottky Diode
Optional					
C6	VCOMDC	Capacitor	2.2 uF	4V	VCOMDC
C7	VCL	Capacitor	2.2 uF	6V	Internal Regulator Output
C12	VGHO	Capacitor	1 uF	16V	HV Regulator Output
C13	VGLO	Capacitor	1 uF	16V	HV Regulator Output

Note 1: If customer need use VGHO or VGLO, the C12/C13 must be existed.

8 Functions

8.1 CABC (Content Adaptive LCD Brightness Control)

8.1.1 Block Diagram

The CABC, a dynamic brightness control function, which can reduce the power consumption of luminance source. To reduce the power consumption, CABC will refer the gray level of display image to decrease the duty of LEDPWM pulse. Simultaneously, to keep the same brightness, the content of gray level will be increased.

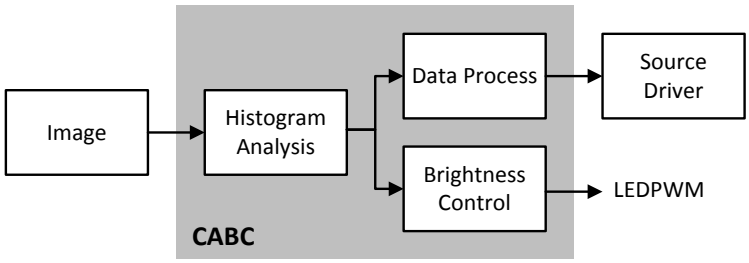


Figure 59. CABC Block Diagram

The XM91080 will calculate the backlight brightness level and output a LEDPWM pulse. The control pulse will via LEDPWM pin to the LED driver for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DUTY_PRECSION parameters, and the calculating equation is shown below:

$$\text{PWM\_FREQ} = \left(\frac{\text{System OSC (MHz)}}{\text{PWM\_DUTY\_PRECSION}}\right)$$

Note: reference to Dynamic Backlight Control 2

Below is the basic timing diagram which is applied by the XM91080 in order to control a LED driver

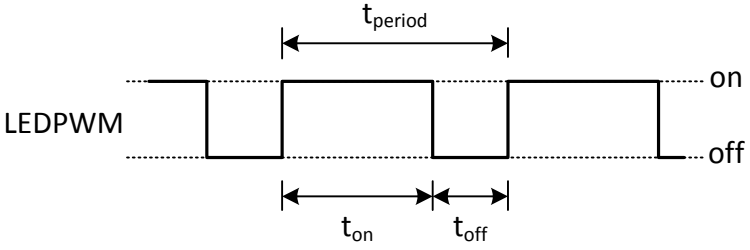


Figure 60. LEDPWM Basic Timing

8.1.2 CABC Mode Operation

The CABC function provides three operation modes, and these modes can be selected by the CMD1 register 55h. See command “Write Power Save (55h)” (CABC[1:0]) for more information. These three modes are described as below:

- **Off Mode**

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, the XM91080 will use the original Gamma registers setting for display.

- **UI Mode (User interface Image Mode)**

This mode is applied to optimize for UI image. It is keep image quality as much as possible. XM91080 provides flexible configuration for UI-Mode via setting the register to choose prefer quality and brightness.

- **Still Mode (Still Picture Mode)**

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. The XM91080 will automatically determine a better gamma setting and PWM duty based on different image contents.

- **Moving Mode (Moving Image Mode)**

User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. For this mode, user can flexibly configure a specified gamma algorithm to keep prefer image quality, and the brightness of backlight is dynamically varying with different image contents.

9 Operation Flowchart

9.1 DrIC State Diagram

The state diagram of XM91080 is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in the figure.

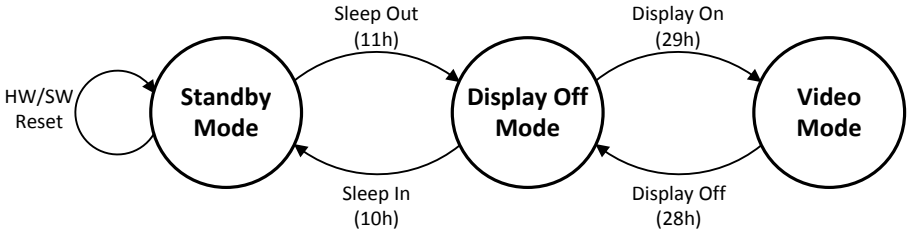


Figure 61. DrIC State Diagram

9.2 Instruction Setting Timing Chart

When setting instruction to the XM91080, the sequences shown in below figures must be followed to complete the instruction setting. If user wants to change the LTPS timing, frame rate, porch settings, it would be necessary to make sure the DrIC is in Standby Mode.

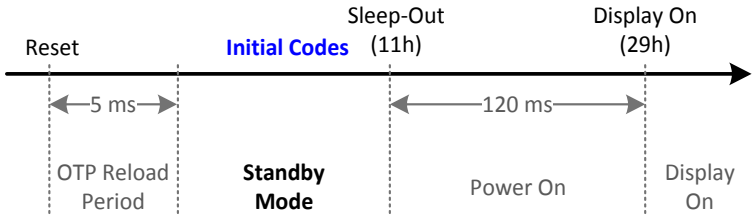
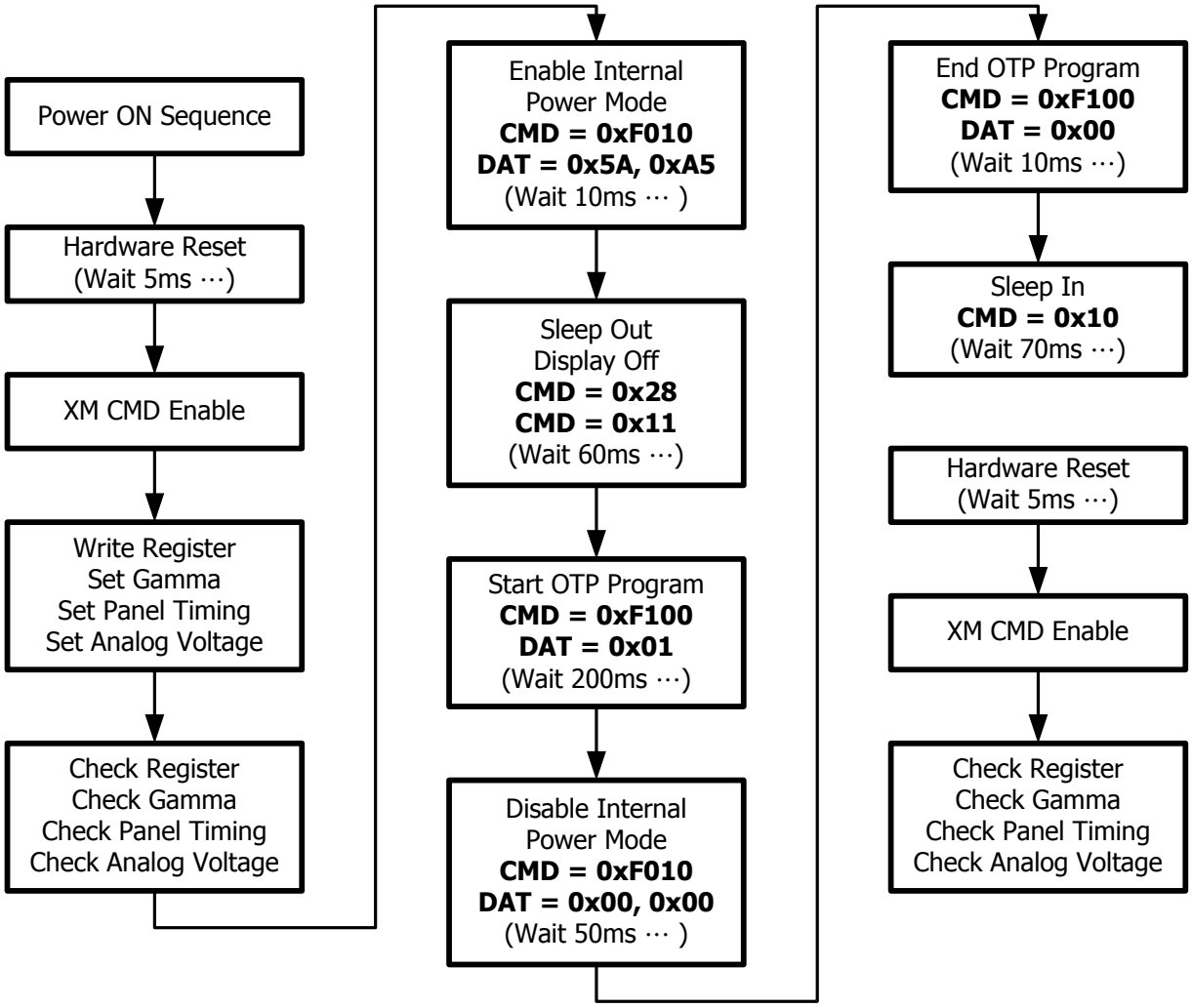


Figure 62. Initial Setting Timing Chart

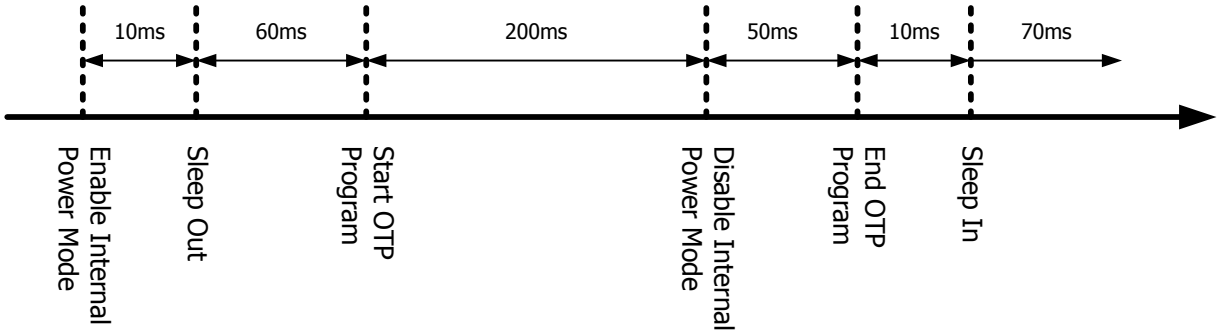
9.3 OTP Programming Procedure

9.3.1 OTP Programming Flow Chart



9.3.2 Programming Sequence

The following figure shows the sequence of OTP programming with internal write power. The first step is to make sure that the driver IC is in “Standby Mode” and then turn on the internal write power for NVM(CMD=0xF010, DAT=0x5A, 0xA5). After that, wait 10ms and write “Sleep Out”(CMD=0x11) command. Wait 60ms to ensure internal power is stable and write “OTP Program Start Command” (CMD=0xF100, DAT=0x01). Wait **200ms** to program data, and then turn off Internal power (CMD=0xF010, DAT=0x00, 0x00). After 50ms, write “OTP Program End Command” (CMD=0xF100, DAT=0x00). Finally, wait 10ms and write “Sleep In” (CMD=0x10) commend. After the sequence is over, Normal operation command is written to verify the OTP memory.



10 Command List

10.1 Command 1

10.1.1 NOP (00h): No Operation

Command Set		NOP (No Operation)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	00h								—
1st Parameter	—	No Parameter								—
Description	This command is empty command. It does not have effect on the display module.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

10.1.2 SWRESET (01h): Software Reset

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">SWRESET (Software Reset)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">01h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">When the Software Reset command is written, it causes a software reset.
It resets the commands and parameters to their S/W Reset default values and the display is blank immediately.</td></tr>
<tr><td>Restriction</td><td colspan="10">It will be necessary to wait 5msec before sending new command following software reset.

The display module loads all display suppliers’ factory default values to the registers during this 5msec.

If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.

Software Reset command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

10.1.3 RDNUMED (05h): Read Number of Errors on DSI

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDNUMED (Read Number of Errors on DSI)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">05h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>P[7]</td><td colspan="7">P[6:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">The first parameter is telling a number of the parity errors on DSI.
P[6:0] bits are telling a number of the parity errors.
P[7] is set to “1” if there is overflow with P[6:0] bits.

See also section “Acknowledge with Error Report (AwER)” and command RDDSM 0Eh.
This command is used for MIPI DSI only. It is no function for others interface operation.</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

10.1.4 RDDPM (0Ah): Read Display Power Mode

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDDPM (Read Display Power Mode)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">0Ah</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>P[7]</td><td>P[6]</td><td>P[5]</td><td>P[4]</td><td>P[3]</td><td>P[2]</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>P[7]</td><td>Booster Voltage Status</td><td>“1”=Booster On,
“0”=Booster Off</td></tr>
<tr><td>P[6]</td><td>Idle Mode On/Off</td><td>“1”=Idle Mode On,
“0”=Idle Mode Off</td></tr>
<tr><td>P[5]</td><td>Partial mode On/Off</td><td>“1”= Partial Mode On,
“0”= Partial Mode Off</td></tr>
<tr><td>P[4]</td><td>Sleep In/Out</td><td>“1” = Sleep Out Mode,
“0” = Sleep In Mode</td></tr>
<tr><td>P[3]</td><td>Display Normal Mode On/Off</td><td>“1” = Display Normal On,
“0” = Display Normal Off</td></tr>
<tr><td>P[2]</td><td>Display On/Off</td><td>“1” = Display is On,
“0” = Display is Off</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

10.1.5 RDDMADCTL (0Bh): Read Display MADCTL

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDDMADCTL (Read Display MADCTL)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">0Bh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P[3]</td><td>0</td><td>P[1]</td><td>P[0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>P[7]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[6]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[5]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[4]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[3]</td><td>RGB/BGR Order</td><td>“1” = BGR
“0” = RGB</td></tr>
<tr><td>P[2]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[1]</td><td>Source Scanning Order</td><td>“1” = Reverse
“0” = Normal</td></tr>
<tr><td>P[0]</td><td>Gate Scanning Order</td><td>“1” = Reverse
“0” = Normal</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

10.1.6 RDDIM (0Dh): Read Display Image Mode

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDDIM (Read Display Image Mode)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">0Dh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>P[5]</td><td>P[4]</td><td>P[3]</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>P[7]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[6]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[5]</td><td>Inversion On/Off</td><td>“1” = Inversion On
“0” = Inversion Off</td></tr>
<tr><td>P[4]</td><td>All Pixel On</td><td>“1” = White display
“0” = Normal display</td></tr>
<tr><td>P[3]</td><td>All Pixel Off</td><td>“1” = Black display
“0” = Normal display</td></tr>
<tr><td>P[2]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[1]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[0]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

10.1.7 RDDSM (0Eh): Read Display Signal Mode

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDDSM (Read Display Signal Mode)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">0Eh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>P[7]</td><td>P[6]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P[0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>P[7]</td><td>Tearing Effect Line On/Off</td><td>“1” = Tearing Effect Line On,
“0” = Tearing Effect Line Off</td></tr>
<tr><td>P[6]</td><td>Tearing Effect Line Mode</td><td>“1” = Mode 2,
“0” = Mode 1</td></tr>
<tr><td>P[5]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[4]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[3]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[2]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[1]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[0]</td><td>Error on DSI</td><td>“1” = Error,
“0” = No Error</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

10.1.8 RDDSDR (0Fh): Read Display Self-Diagnostic Result

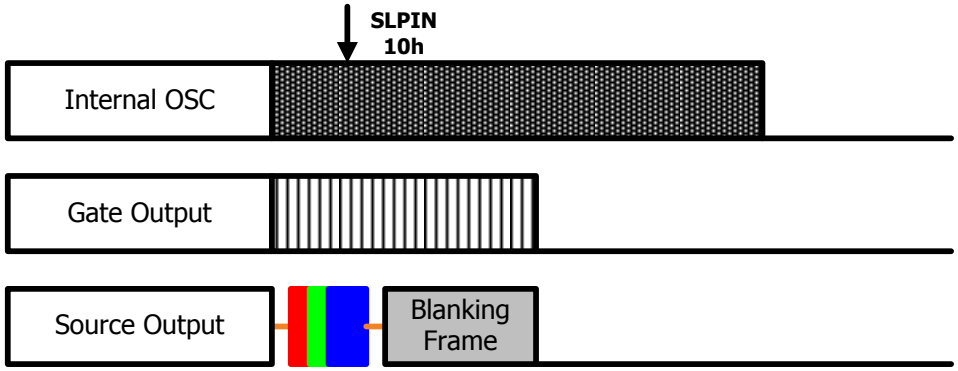
<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDDSDR (Read Display Self-Diagnostic Result)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">0Fh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>P[7]</td><td>P[6]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.

<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>P[7]</td><td>Register Leading Detection</td><td>—</td></tr>
<tr><td>P[6]</td><td>Functionality Detection</td><td>—</td></tr>
<tr><td>P[5]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[4]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[3]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[2]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[1]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[0]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

10.1.9 SLPIN (10h): Sleep In

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">SLPIN (Sleep In)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">10h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the TFT LCD module to enter the minimum power consumption mode.

In this mode the DC/DC converter is stopped, internal display oscillator is stopped, and panel scanning is stopped. Control Interface as well as display data and registers are still working.

 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).

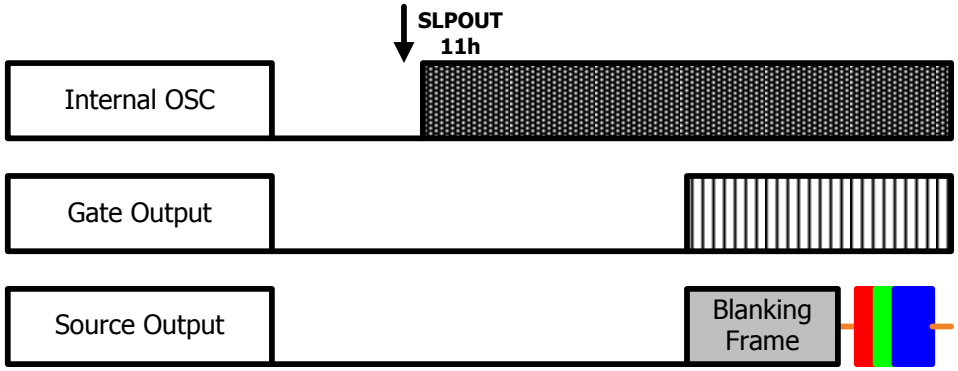
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.

It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
</table>

10.1.10 SLPOUT (11h): Sleep Out

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">SLPOUT (Sleep Out)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">11h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the display module to leave sleep mode.

In this mode the DC/DC converter is enabled, internal display oscillator is started, and panel scanning is started.

 
</td></tr>
<tr><td>Restriction</td><td colspan="10">Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W reset command (01h) or H/W reset.

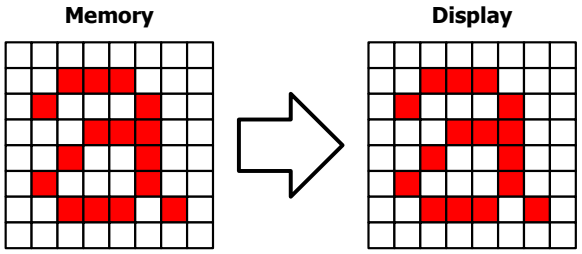
It will be necessary to wait 5msec before ending next command. The delay allows the supply voltages and clock circuits to stabilize.

It is necessary to wait 120 ms after sending Sleep In command(when in Sleep Out mode) before Sleep Out command can be sent.

The display module loads default values and command to the registers and there cannot be any abnormal visual effect on the display module when loading the registers if the factory default and registers values are the same or when the display module is not in sleep mode.

After this command is received, the display module runs the self-disgnostic function.</td></tr>
<tr><td>Default</td><td colspan="10"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr>
<tr><td>S/W Reset</td><td>Sleep In Mode</td></tr>
<tr><td>H/W Reset</td><td>Sleep In Mode</td></tr>
</table></td></tr>
</table>

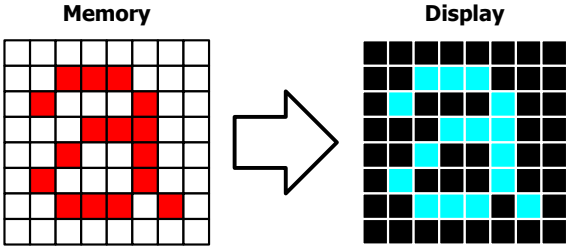
10.1.11 INVOFF (20h): Display Inversion Off

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">INVOFF (Display Inversion Off)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">20h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from display inversion mode. This command does not change any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Inversion Off mode.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

10.1.12 INVON (21h): Display Inversion On

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">INVON (Display Inversion On)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">21h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter display inversion mode. This command does not change any other status.

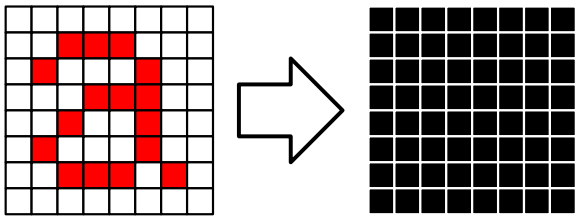
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Inversion On mode.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

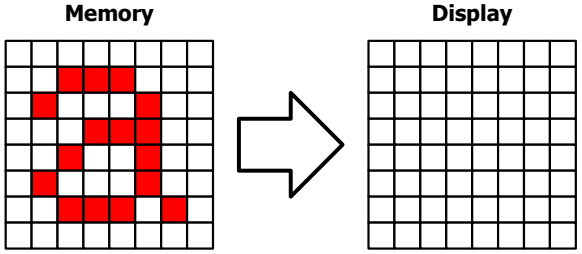
10.1.13 ALLPOFF (22h): All Pixel Off

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">ALLPOFF (All Pixel Off)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">22h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.

“All Pixels On” or “Normal Display Mode On” commands are used to leave this mode. The display panel is showing the display data after “Normal Display Mode On” command.

Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in ALL Pixel Off mode.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
</table>

10.1.14 ALLPON (23h): All Pixel On

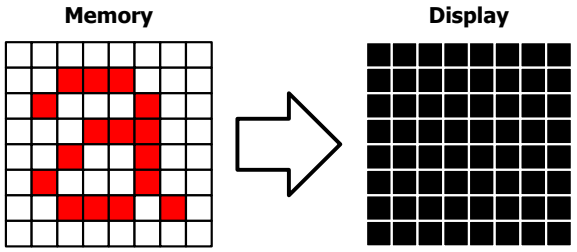
Command Set		ALLPON (All Pixel On)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	23h								—
1st Parameter	—	No Parameter								—
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. "All Pixels Off" or "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the display data after "Normal Display Mode On" command. 									
Restriction	This command has no effect when module is already in ALL Pixel On mode.									
Default										

Status	Default Value
Power On Sequence	Normal Display Mode On
S/W Reset	Normal Display Mode On
H/W Reset	Normal Display Mode On

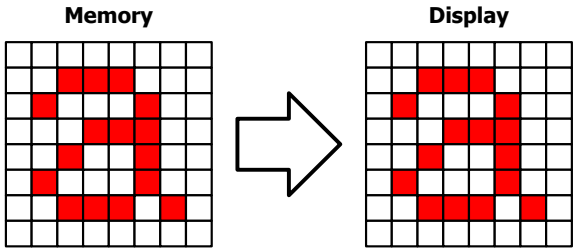
10.1.15 DISPOFF (28h): Display Off

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">DISPOFF (Display Off)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">28h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into DISPLAY OFF mode. In this mode, the display data is disabled and blank page inserted.

This command does not change any other status. There will be no abnormal visible effect on the display.

  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
</table>

10.1.16 DISPON (29h): Display On

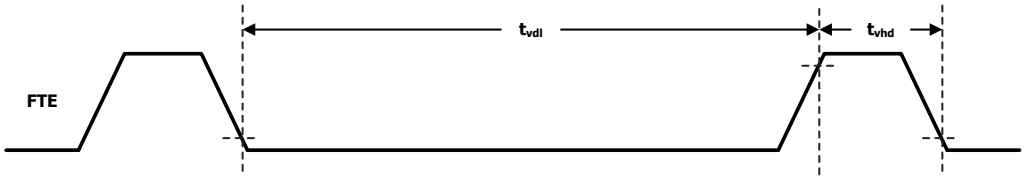
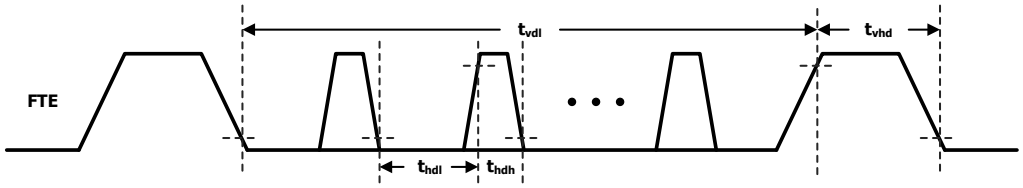
Command Set		DISPON (Display On)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	29h								—
1st Parameter	—	No Parameter								—
Description	This command is used to enter into DISPLAY OFF mode. Output from display data is enabled. This command does not change any other status. 									
Restriction	This command has no effect when module is already in Display On mode.									
Default										

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

10.1.17 TEOFF (34h): Tearing Effect Line OFF

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">TEOFF (Tearing Effect Line OFF)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">34h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Tearing Effect Line OFF</td></tr><tr><td>S/W Reset</td><td>Tearing Effect Line OFF</td></tr><tr><td>H/W Reset</td><td>Tearing Effect Line OFF</td></tr></table></td></tr>
</table>

10.1.18 TEON (35h): Tearing Effect Line ON

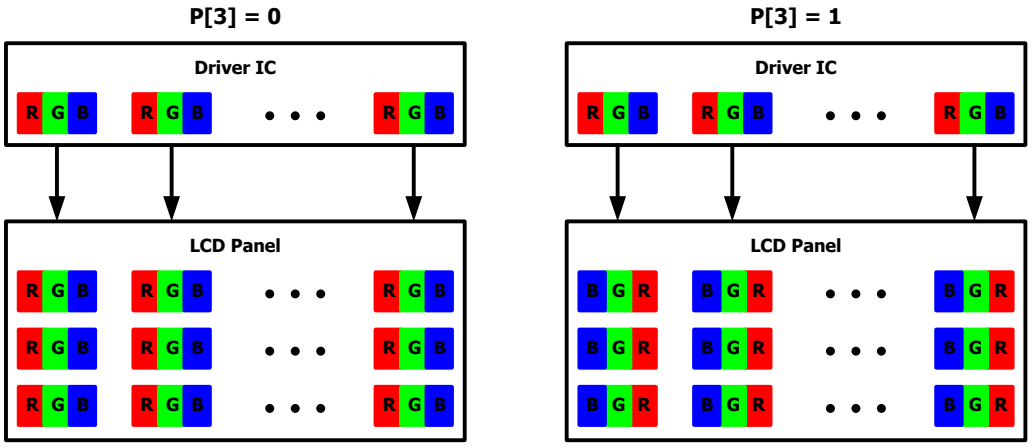
Command Set		TEON (Tearing Effect Line ON)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	35h								—
1st Parameter	Write	0	0	0	0	0	0	0	P[0]	00h
Description	This command is used to turn ON (Active Low) the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. When P[0] = “0”: The Tearing Effect Output line consists of V-Blanking information only.  When P[0] = “1”: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.  									
Restriction	This command has no effect when Tearing Effect output is already ON.									
Default										

Status	Default Value
Power On Sequence	Tearing Effect Line OFF
S/W Reset	Tearing Effect Line OFF
H/W Reset	Tearing Effect Line OFF

10.1.19 MADCTL (36h): Memory Data Access Control

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">MADCTL (Memory Data Access Control)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">36h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P[3]</td><td>0</td><td>P[1]</td><td>P[0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:

<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>P[7]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[6]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[5]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[4]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[3]</td><td>RGB/BGR Order</td><td>“1” = BGR
“0” = RGB</td></tr>
<tr><td>P[2]</td><td>Reserved</td><td>Set to “0” (not used)</td></tr>
<tr><td>P[1]</td><td>Source Scanning Order</td><td>“1” = Reverse
“0” = Normal</td></tr>
<tr><td>P[0]</td><td>Gate Scanning Order</td><td>“1” = Reverse
“0” = Normal</td></tr>
</table>



</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

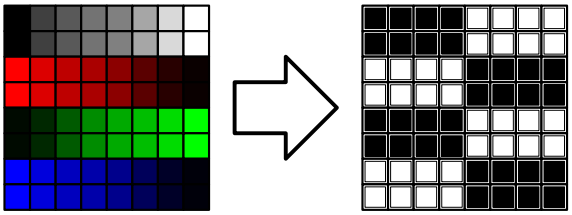
10.1.20 IDMOFF (38h): Idle Mode Off

Command Set		IDMOFF (Idle Mode Off)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	38h								—
1st Parameter	—	No Parameter								—
Description	This command is used to recover from Idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.									
Restriction	This command has no effect when module is already in Idle Off mode.									
Default										

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

10.1.21 IDMON (39h): Idle Mode On

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">IDMON (Idle Mode On)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">39h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>—</td><td colspan="8">No Parameter</td><td>—</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Memory, 8 color depth data is displayed.

Memory Display
 

<table>
<tr><th>Color</th><th>$R_7 – R_0$</th><th>$G_7 – G_0$</th><th>$B_7 – B_0$</th></tr>
<tr><td>Black</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr>
<tr><td>Blue</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr>
<tr><td>Green</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr>
<tr><td>Cyan</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr>
<tr><td>Red</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr>
<tr><td>Magenta</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr>
<tr><td>Yellow</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr>
<tr><td>White</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Idle On mode.</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr>
<tr><td>S/W Reset</td><td>Idle Mode Off</td></tr>
<tr><td>H/W Reset</td><td>Idle Mode Off</td></tr>
</table></td></tr>
</table>

10.1.22 WRDBV (51h): Write Display Brightness Value

Command Set		WRDBV (Write Display Brightness Value)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	51h								—
1st Parameter	Write	DBV[11:4]								FFh
2nd Parameter	Write	0	0	0	0	DBV[3:0]				0Fh
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	FFh, 0Fh
S/W Reset	FFh, 0Fh
H/W Reset	FFh, 0Fh

10.1.23 RDDBV (52h): Read Display Brightness Value

Command Set		RDDBV (Read Display Brightness Value)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	52h								—
1st Parameter	Read	DBV[11:4]								FFh
2nd Parameter	Read	0	0	0	0	DBV[3:0]				0Fh
Description	This command read out the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness. DBV [11:0] is reset when display is in Sleep In mode. DBV [11:0] is “0” when bit BCTRL of Write CTRL Display Value (53h) is “0”. DBV [11:0] is manual set brightness specified with Write CTRL Display Value (53h) when BCTRL bit is “1”. When bit BCTRL of Write CTRL Display Value (53h) is '1' and D1/D0 bit of Write Power Save (55h) are '0', DBV[11:0] output is the brightness value specified with Write Display Brightness Value (51h).									
Restriction	—									
Default		Status	Default Value							
		Power On Sequence	FFh, 0Fh							
		S/W Reset	FFh, 0Fh							
		H/W Reset	FFh, 0Fh							

10.1.24 WRCTRLD (53h): Write Ctrl Display

Command Set		WRCTRLD (Write Ctrl Display)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	53h								—
1st Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	00h
Description										
Restriction	—									
Default										

Name	Description
BCTRL	BCTRL=0, Brightness Control Block off BCTRL=1, Brightness Control Block on
DD	DD=0, Display Dimming off DD=1, Display Dimming on
BL	BL=0, Backlight Control off BL=1, Backlight Control on

Status	Default Value
Power On Sequence	00h, 00h
S/W Reset	00h, 00h
H/W Reset	00h, 00h

10.1.25 RDCTRLD (54h): Read Ctrl Display

Command Set		RDCTRLD (Read Ctrl Display)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	54h								—
1st Parameter	Read	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h

Description

HBM : High Brightness Mode

These bits control the high brightness mode.

HBM[1]	HBM[0]	Description
0	0	High brightness mode is off.
0	1	High brightness mode is on. LCD boost signal is on. LED PWM = 100% PWM
1	0	High brightness mode is on. LCD boost signal is on. LED PWM = 100% PWM
1	1	High brightness mode is on. LCD boost signal is on. LED PWM = 100% PWM

Name	Description
BCTRL	BCTRL=0, Brightness Control Block off BCTRL=1, Brightness Control Block on
DD	DD=0, Display Dimming off DD=1, Display Dimming on
BL	BL=0, Backlight Control off BL=1, Backlight Control on

Restriction —

Default

Status	Default Value
Power On Sequence	00h, 00h
S/W Reset	00h, 00h
H/W Reset	00h, 00h

10.1.26 PWRSAVE (55h) : Write Power Save

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">PWRSAVE (Write Power Save)</td><td>Default</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>(Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">55h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">CABC[1:0]</td><td>00h</td></tr>
<tr><td>0</td><td colspan="10">This command is used to set parameters for image content based adaptive brightness control and image enhancement level control functionality.
There are 4 different modes for content adaptive image functionality, which are defined on a table as below.
<table>
<tr><th>CABC1</th><th>CABC0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>CABC Off</td></tr>
<tr><td>0</td><td>1</td><td>User Interface Image (UI-Mode)</td></tr>
<tr><td>1</td><td>0</td><td>Still Picture Mode (Still Mode)</td></tr>
<tr><td>1</td><td>1</td><td>Moving Image (Moving Mode)</td></tr>
</table>
CABC = Content Adaptive Brightness Control</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

10.1.27 RDPWRSAVE (56h) : Read Power Save

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDPWRSAVE (Read Power Save)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">56h</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">CABC[1:0]</td><td>00h</td></tr>
<tr><td>0</td><td colspan="10">This command is used to read parameters for image content based adaptive brightness control and image enhancement level control functionality.
There are 4 different modes for content adaptive image functionality, which are defined on a table below.
<table>
<tr><th>CABC1</th><th>CABC0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>CABC Off</td></tr>
<tr><td>0</td><td>1</td><td>User Interface Image (UI-Mode)</td></tr>
<tr><td>1</td><td>0</td><td>Still Picture Mode (Still Mode)</td></tr>
<tr><td>1</td><td>1</td><td>Moving Image (Moving Mode)</td></tr>
</table>
CABC = Content Adaptive Brightness Control</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

10.1.28 WRCABCMB (5Eh): Write CABC Minimum Brightness

Command Set		WRCABCMB (Write CABC Minimum Brightness)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	5Eh								—
1st Parameter	Write	CMB[11:4]								00h
2nd Parameter	Write	0	0	0	0	CMB[3:0]				00h
Description	This command is used to set the minimum brightness value of the display for CABC function. CMB[11:0]: CABC minimum brightness control, this parameter is used to set a limit to the amount of brightness reduction allowed.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	00h, 00h
S/W Reset	00h, 00h
H/W Reset	00h, 00h

10.1.29 RDCABCMB (5Fh): Read CABC Minimum Brightness

Command Set		RDCABCMB (Read CABC Minimum Brightness)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	5Fh								—
1st Parameter	Read	CMB[11:4]								00h
2nd Parameter	Read	0	0	0	0	CMB[3:0]				00h
Description	This command is used to read the minimum brightness value of the display for CABC function. CMB[11:0]: CABC minimum brightness control, this parameter is used to set a limit to the amount of brightness reduction allowed.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	00h, 00h
S/W Reset	00h, 00h
H/W Reset	00h, 00h

10.1.30 RDDDBS (A1h): Read DDB Start

Command Set		RDDDBS (Read DDB Start)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	A1h								—
1st Parameter	Read	DDBID1[7:0]								00h
2nd Parameter	Read	DDBID2[7:0]								00h
⋮	Read	DDBIDx[7:0]								00h
16th Parameter	Read	DDBID16[7:0]								00h
17th Parameter	Read	1	1	1	1	1	1	1	1	FFh
Description	This command returns the first checksum calculated from User's area registers and the Frame Memory after the write access to those registers and/or Frame Memory has been done. This command returns supplier identification and display module model/revision information. 17th Parameter：FFh - Exit code – there is no more data in the Descriptor Block									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	00h, 00h, …, 00h, FFh
S/W Reset	00h, 00h, …, 00h, FFh
H/W Reset	00h, 00h, …, 00h, FFh

10.1.31 RDDDBC (A8h): Read DDB Continue

Command Set		RDDDBC (Read DDB Continue)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	A8h								—
1st Parameter	Read	DDBIDm[7:0]								00h
⋮	Read	DDBIDx[7:0]								00h
nth Parameter	Read	DDBIDn[7:0]								00h
Description	This command is used to return the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command. A read DDB start (RDDDBS) command should be executed at least once before a Read DDB Continue (A8h) (RDDDBC) to define the read location.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	00h, 00h, …, 00h
S/W Reset	00h, 00h, …, 00h
H/W Reset	00h, 00h, …, 00h

10.1.32 RDFCS (AAh): Read First Checksum

Command Set		RDFCS (Read First Checksum)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	AAh								—
1st Parameter	Read	FCS[15:8]								00h
2nd Parameter	Read	FCS[7:0]								00h
Description	This command returns the first checksum calculated from User's area registers.									
Restriction	—									
Default										

Status	Default Value
Power On Sequence	00h, 00h
S/W Reset	00h, 00h
H/W Reset	00h, 00h

10.1.33 RDCCS (AFh): Read Continuous Checksum

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDCCS (Read Continuous Checksum)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">AFh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">CCS[15:7]</td><td>00h</td></tr>
<tr><td>2nd Parameter</td><td>Read</td><td colspan="8">CCS[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command returns the continuous checksum that has been calculated continuously after the first checksum has been calculated with User defined area registers.</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>xxh</td></tr><tr><td>S/W Reset</td><td>xxh</td></tr><tr><td>H/W Reset</td><td>xxh</td></tr></table></td></tr>
</table>

10.1.34 RDID1 (DAh): Read ID1

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDID1 (Read ID1)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">DAh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID1[7:0]</td><td>40h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version.

It is defined by the display supplier (with User's agreement) and changes each time when a revision is made to the display, material or construction specifications.

The ID1 can be programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>40h</td><td>OTP Value</td></tr><tr><td>S/W Reset</td><td>40h</td><td>OTP Value</td></tr><tr><td>H/W Reset</td><td>40h</td><td>OTP Value</td></tr></table></td></tr>
</table>

10.1.35 RDID2 (DBh): Read ID2

<table>
<tr><td colspan="2">Command Set</td><td colspan="8">RDID2 (Read ID2)</td><td rowspan="2">Default (Hex)</td></tr>
<tr><td>Type</td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>Command</td><td>Write</td><td colspan="8">DBh</td><td>—</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID2[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version.

It is defined by the display supplier (with User's agreement) and changes each time when a revision is made to the display, material or construction specifications.

The ID2 can be programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10">—</td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value (Before OTP program)</th><th>Default Value (After OTP program)</th></tr><tr><td>Power On Sequence</td><td>00h</td><td>OTP Value</td></tr><tr><td>S/W Reset</td><td>00h</td><td>OTP Value</td></tr><tr><td>H/W Reset</td><td>00h</td><td>OTP Value</td></tr></table></td></tr>
</table>

10.1.36 RDID3 (DCh): Read ID3

Command Set		RDID3 (Read ID3)								Default
Type	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	(Hex)
Command	Write	DCh								—
1st Parameter	Read	ID3[7:0]								00h
Description	This read byte identifies the LCD module/driver. It is specified by User. The ID3 can be programmed by OTP function.									
Restriction	—									
Default										

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	00h	OTP Value
S/W Reset	00h	OTP Value
H/W Reset	00h	OTP Value

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +1.95	V
Power Supply Voltage 3	AVDD-VSS	-0.3 ~ +6.0	V
Power Supply Voltage 4	OTP_PWR-VSS	-0.3 ~ +8.25	V
Power Supply Voltage 5	VDD-VSS	-0.3 ~ +1.5	V
Power Supply Voltage 6	VSS-AVEE	-0.3 ~ +6.0	V
Power Supply Voltage 7	VGH-VGL	-0.3 ~ +32	V
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V
Operating Temperature	Topr	-30 ~ +70	˚C
Storage Temperature	Tstg	-55 ~ +110	˚C
Humidity		5 ~ 95	%

NOTE:

If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

11.2 DC Characteristics

11.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ	Max		
Power & Operation Voltage							
Analog power supply voltage	AVDD	Power supply voltage	4.5	5	6	V	Note 1
Analog power supply voltage	AVEE	Power supply voltage	-4.5	-5	-6	V	Note 1
Logic operating voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	Note 1
HiSSi interface operating voltage	VDDAM	Digital supply voltage	1.65	1.8	1.95	V	Note 1
Input / Output							
Logic high level input voltage	VIH	-	0.7VDDI	-	VDDI	V	Note 1, 2
Logic low level input voltage	VIL	-	VSS	-	0.3VDDI	V	Note 1, 2
Logic high level output voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1, 2
Logic low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDI	V	Note 1, 2
Logic High level input current	IIH	-		-	1	A	Note 1, 2
Logic Low level input current	IIL	-	-1	-		A	Note 1, 2
Logic input leakage current	IIL	VIN = VDDI or VSS	-0.1	-	0.1	A	Note 1, 2
VCOM Operation							
VCOM voltage	VCOM	-	-4	-	0	V	
Source Driver							
Source output range	V_{SOUT}	-	NGVDD	-	GVDD	V	Note3
Gamma positive reference voltage	GVDD	-	2.62	-	5.68	V	
Gamma negative reference voltage	NGVDD	-	-5.68	-	-2.62	V	
source output settling time	Tr	Below with 99% precision	-	5	-		
Output deviation voltage (positive channel)	Vdev	Sout >= +4.2V , Sout <= +0.8V	-	-	30	mV	
		+4.2V > Sout > 0.8V	-	-	20	mV	
Output deviation voltage (negative channel)	Vdev	Sout <= -4.2V , Sout >= -0.8V	-	-	30	mV	
		-4.2V < Sout < -0.8V	-	-	20	mV	
Output offset voltage	V_{OFFSET}	-	-	-	35	mV	
Reference Voltage							
Internal reference voltage	VREF	-	1.94	2	2.06	V	
Standby Mode Current Consumption							
Sleep In Mode	I_{VDDI}	Ta=25℃			TBD	uA	
	I_{VSP}	VDDI=1.8V			TBD	uA	
	I_{VSN}	VSP=5.5V			TBD	uA	
Deep Standby Mode	I_{VDDI}	VSN=-5.5V			TBD	uA	Note4

	I_{VSP}				TBD	uA	
	I_{VSN}				TBD	uA	

Note 1: VDDI=1.65 to 1.95V, VDDAM=1.65 to 1.95 V, AVDD=4.5 to 6.0V, AVEE=-6.0 to -4.5V, AVSS=VSS=0V, Ta=-30 to 75℃ (to +85℃ no damage)

Note 2: When the measurements are performed with LCD module, Measurement Points are like below.

CSX, RDX, WRX, D[23:0], DCX, RESX, SCL, IM[2 : 0] and Test pins

Note 3: Source channel loading= 40pF/channel

Note 4: If support deep standby mode.

11.2.2 DSI DC Characteristics

Parameter	Symbol	Conditions	Specification			Unit
			Min	Typ	Max	
Power supply voltage for MIPI RX	VDDAM		1.65	1.8	3.6	V
High speed / Low power mode operating voltage	VP_HSSI			1.2		V
MIPI Characteristics for High Speed Receiver						
Single-ended input low voltage	V_{ILHS}		-40			mV
Single-ended input high voltage	V_{IHHS}				460	mV
Common-mode voltage	V_{CMRXDC}		70		330	mV
Differential input impedance	ZID		80	100	125	ohm
HS transmit differential voltage (VOD=VDP-VDN)	$\|V_{OD}\|$		140	200	250	mV
Different input high threshold	V_{IDTH}				70	mV
Different input low threshold	V_{IDTL}		-70			mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$				450	
MIPI Characteristics for Low Power Mode						
Pad signal voltage range	VI		-50		1350	mV
Ground shift	V_{VSSSH}		-50		50	mV
Logic 0 input threshold	V_{IL}		0		550	mV
Logic 1 input threshold	V_{IH}		880		VDDAM	mV
Input hysteresis	V_{HYST}		25			mV
Output low level	V_{OL}		-50		50	mV
Output high level	V_{OH}		1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP		80	100	125	Ohm
Logic 0 contention threshold	$V_{IHCD,MAX}$		0		200	mV
Logic 1 contention threshold	$V_{ILCD,MIN}$		450		VDDAM	mV

Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). The complete set of electrical functions required for a fully featured PHY transceiver.

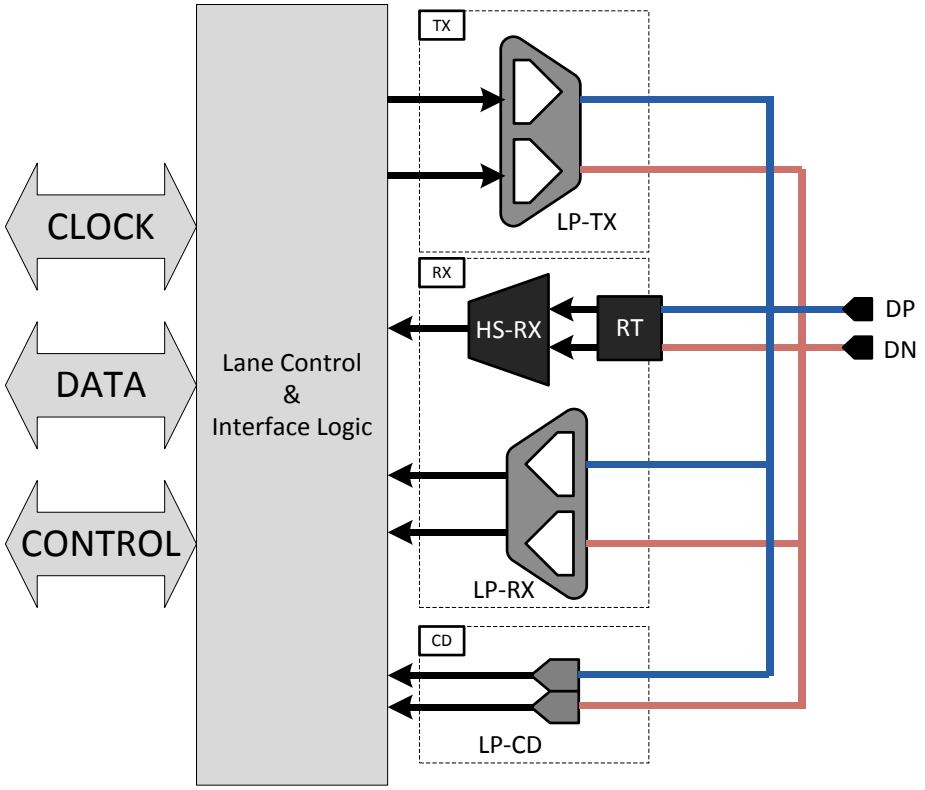


Figure 1. Electrical functions of a fully D-PHY transceiver.

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism.Both the HS and LP signal levels on the left and right sides, respectively. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

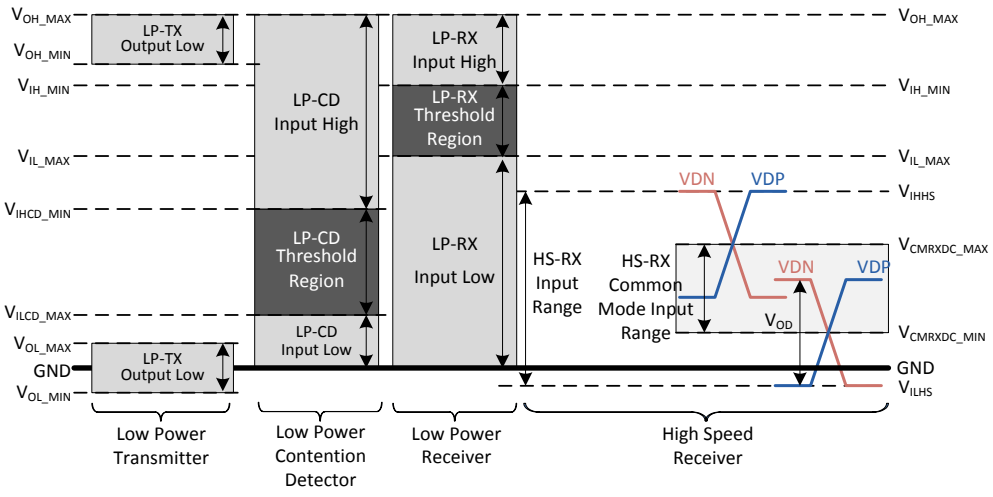


Figure 2. D-PHY Signaling and Contention Voltage Levels

11.2.3 Timing for DSI Video mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
BR_{PHY}	Bit rate per Lane	HD (720RGB x 1280)	300	-	1200	Mbps
t_L	Line time	HD (720RGB x 1280)	-	12.70 (Note 1)	-	us
t_{HBP}	Horizontal back porch	HD (720RGB x 1280)	TBD	-	-	us
t_{HACT}	Time for image data	4 data lane	TBD	-	(Note 2)	us
HACT	Active pixels per line	HD (720RGB x 1280)		720	-	pixels
t_{HFP}	Horizontal front porch		TBD	-	-	us
VSA	Vertical sync active		2 (Note 3)	-	-	H
VBP	Vertical back porch		2 (Note 3)	-	-	H
VACT	Active lines per frame	HD (720RGB x 1280)		1280 (Note 3)		H
VFP	Vertical front porch		4 (Note 3)	-	-	H

Note:

1. *Frame rate (Typ)= 60Hz, and VBP=16 / VFP=16*
2. *$t_{HACT}(Max)=t_L - t_{HFP} - t_{HBP}$*
3. *(VSA + VBP + VACT + VFP) must be a multiple of VCK/XVCK phase number.*

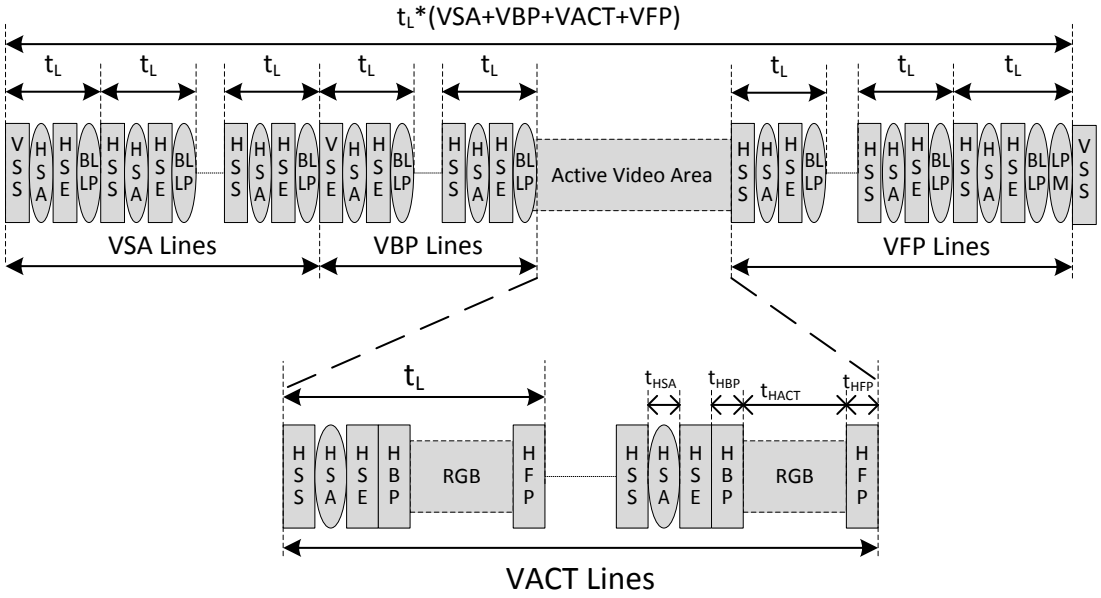


Figure 3. Video Mode Interface Timing

11.3 AC Characteristics

11.3.1 MIPI Interface Characteristics

High Speed Data Transmission: Data-Clock Timing

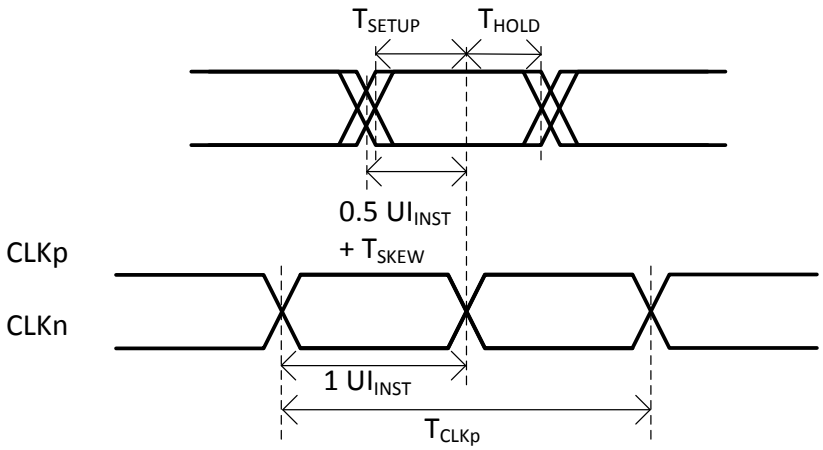


Figure 4. High Speed Data Transmission: Data-Clock Timing

Parameter	Symbol	Specification			Unit	Notes
		Min	Typ	Max		
UI instantaneous	UI_{INST}	1		12.5	ns	Note1,2
Data to Clock Skew [measured at transmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	-0.15		0.15	UI_{INST}	
Data to Clock Hold Time [measured at receiver]	T_{HOLD}[RX]	-0.15		0.15	UI_{INST}	
20% - 80% rise time and fall time	t_R/t_F	100			ps	Note3
				0.3	UI_{INST}	

Note:

1. *This value corresponds to a minimum 300 MHz data rate*
2. *MIPI speed limitation: Per lane bandwidth is 1.2Gbps*
3. *Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1.2 Gbps (UI ≥ 0.8334ns), should not use values below 100 ps.*

11.4 Reset Timing Characteristics

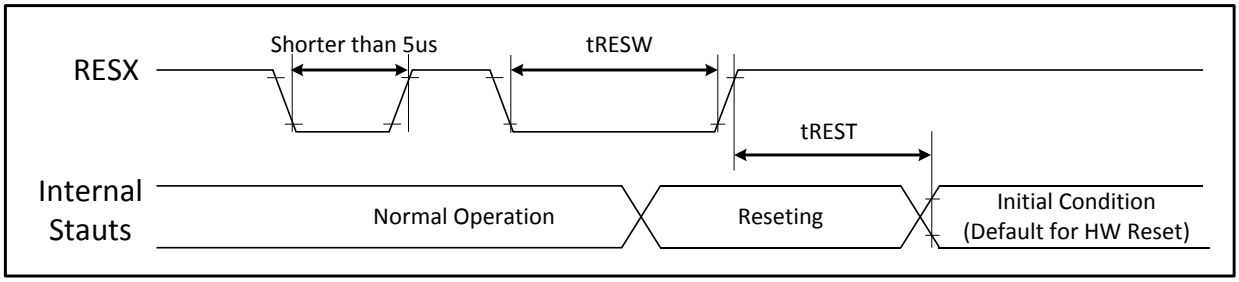


Figure 5. Reset Input Timing

Symbol	Parameter	Related Pins	Spec.			Unit	Note
			Min.	Typ.	Max.		
tRESW	Reset low pulse width	RESX	10	-	-	µs	-
tREST	Reset complete time	-	-	-	5	ms	During Sleep in mode
tREST	Reset complete time	-	-	-	120	ms	During Sleep out mode

Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset low pulse width
Longer than 10µs	Reset complete time
Between 5µs and 10µs	Reset start (by voltage and temperature condition)

During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) and then return to Default condition for H/W reset. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX. Spike Rejection also applies during a valid reset pulse as shown below:

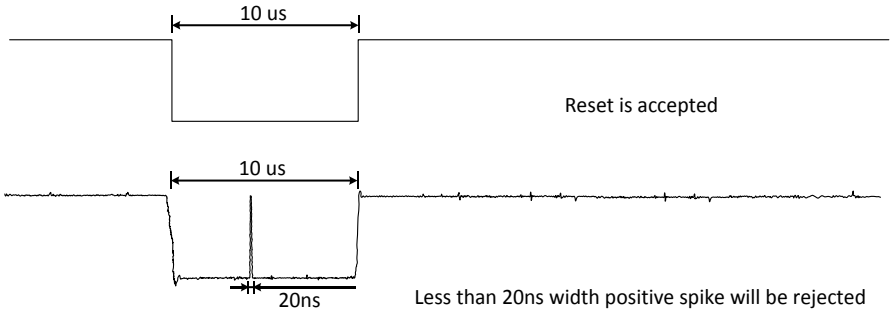
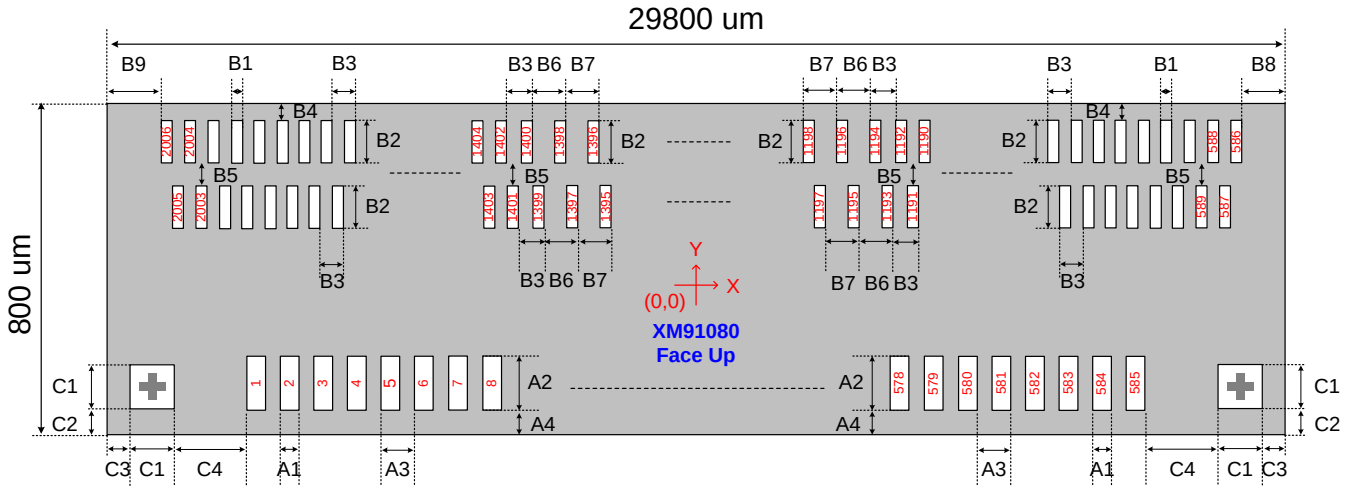


Figure 6. Reset Timing

It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

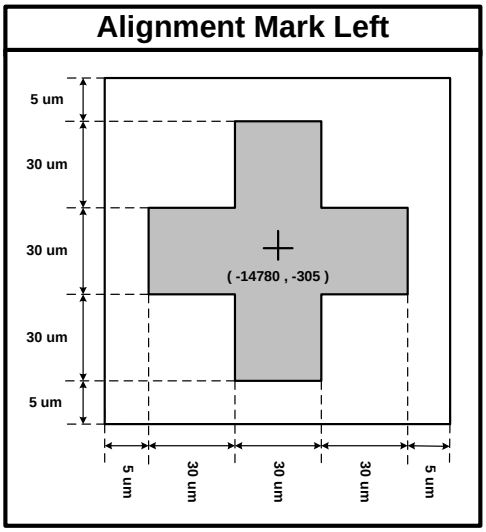
12 Chip Information

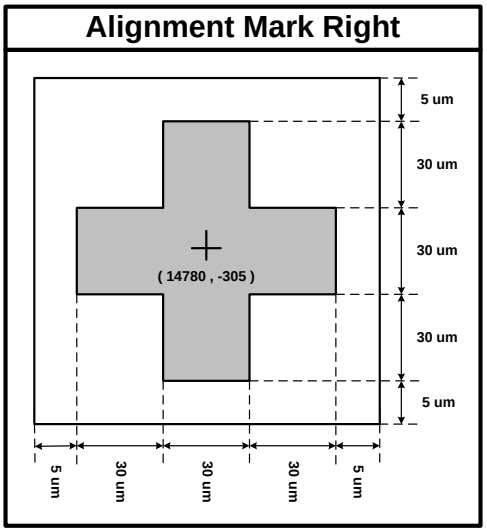
12.1 Bump Information



Scribe Line : 62um					
Symbol	**Size**	**Symbol**	**Size**	**Symbol**	**Size**
A1	25	B3	36	B9	284
A2	120	B4	49	C1	100
A3	50	B5	30	C2	45
A4	49	B6	54	C3	70
B1	18	B7	72	C4	117.5
B2	90	B8	266	um	

12.2 Alignment Mark





12.3 Pad Assignment

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1	OTP_PWR	-14600	-291	36	VGHO	-12850	-291
2	OTP_PWR	-14550	-291	37	VGH	-12800	-291
3	OTP_PWR	-14500	-291	38	VGH	-12750	-291
4	VCOMDC	-14450	-291	39	VGH	-12700	-291
5	VCOMDC	-14400	-291	40	VGH	-12650	-291
6	VCOMDC	-14350	-291	41	VGH	-12600	-291
7	VCOMDC	-14300	-291	42	VGH	-12550	-291
8	VCOMDC	-14250	-291	43	C21P	-12500	-291
9	VCOMDC	-14200	-291	44	C21P	-12450	-291
10	AVSS	-14150	-291	45	C21P	-12400	-291
11	AVSS	-14100	-291	46	C21P	-12350	-291
12	AVSS	-14050	-291	47	C21P	-12300	-291
13	VGLO	-14000	-291	48	C21P	-12250	-291
14	VGLO	-13950	-291	49	C21P	-12200	-291
15	VGLO	-13900	-291	50	C21P	-12150	-291
16	VSS	-13850	-291	51	C21P	-12100	-291
17	VSS	-13800	-291	52	C21M	-12050	-291
18	VSS	-13750	-291	53	C21M	-12000	-291
19	DUMMY1	-13700	-291	54	C21M	-11950	-291
20	DUMMY1	-13650	-291	55	C21M	-11900	-291
21	DUMMY1	-13600	-291	56	C21M	-11850	-291
22	DUMMY1	-13550	-291	57	C21M	-11800	-291
23	DUMMY2	-13500	-291	58	C21M	-11750	-291
24	DUMMY2	-13450	-291	59	C21M	-11700	-291
25	DUMMY2	-13400	-291	60	VSS	-11650	-291
26	DUMMY2	-13350	-291	61	AVDD	-11600	-291
27	DUMMY3	-13300	-291	62	AVDD	-11550	-291
28	DUMMY3	-13250	-291	63	AVDD	-11500	-291
29	DUMMY3	-13200	-291	64	AVDD	-11450	-291
30	DUMMY3	-13150	-291	65	AVDD	-11400	-291
31	VGHO	-13100	-291	66	AVDD	-11350	-291
32	VGHO	-13050	-291	67	AVDD	-11300	-291
33	VGHO	-13000	-291	68	AVDD	-11250	-291
34	VGHO	-12950	-291	69	AVDD	-11200	-291
35	VGHO	-12900	-291	70	AVDD	-11150	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
71	AVDD	-11100	-291	107	C41M	-9300	-291
72	AVDD	-11050	-291	108	C41M	-9250	-291
73	AVDD	-11000	-291	109	C41P	-9200	-291
74	AVDD	-10950	-291	110	C41P	-9150	-291
75	AVDD	-10900	-291	111	C41P	-9100	-291
76	AVDD	-10850	-291	112	C41P	-9050	-291
77	AVDD	-10800	-291	113	C41P	-9000	-291
78	AVDD	-10750	-291	114	C41P	-8950	-291
79	AVDD	-10700	-291	115	VCL	-8900	-291
80	AVDD	-10650	-291	116	VCL	-8850	-291
81	VSS	-10600	-291	117	VCL	-8800	-291
82	EXTP	-10550	-291	118	VCL	-8750	-291
83	EXTP	-10500	-291	119	VCL	-8700	-291
84	EXTP	-10450	-291	120	VCL	-8650	-291
85	AVEE	-10400	-291	121	AVDD	-8600	-291
86	AVEE	-10350	-291	122	AVDD	-8550	-291
87	AVEE	-10300	-291	123	AVDD	-8500	-291
88	AVEE	-10250	-291	124	AVDD	-8450	-291
89	AVEE	-10200	-291	125	AVDD	-8400	-291
90	AVEE	-10150	-291	126	AVDD	-8350	-291
91	AVEE	-10100	-291	127	AVDD	-8300	-291
92	AVEE	-10050	-291	128	AVDD	-8250	-291
93	AVEE	-10000	-291	129	AVDD	-8200	-291
94	AVEE	-9950	-291	130	GVDDP	-8150	-291
95	AVEE	-9900	-291	131	VREFM	-8100	-291
96	AVEE	-9850	-291	132	GVDDN	-8050	-291
97	VSS	-9800	-291	133	VCOMDC	-8000	-291
98	VSS	-9750	-291	134	VCOMDC	-7950	-291
99	VSS	-9700	-291	135	VCOMDC	-7900	-291
100	VSS	-9650	-291	136	VCOMDC	-7850	-291
101	VSS	-9600	-291	137	VCOMDC	-7800	-291
102	VSS	-9550	-291	138	VCOMDC	-7750	-291
103	C41M	-9500	-291	139	VCOMDC	-7700	-291
104	C41M	-9450	-291	140	VCOMDC	-7650	-291
105	C41M	-9400	-291	141	VCOMDC	-7600	-291
106	C41M	-9350	-291	142	AVSS	-7550	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
143	AVSS	-7500	-291	179	RDX	-5700	-291
144	AVSS	-7450	-291	180	TESTIN2	-5650	-291
145	AVSS	-7400	-291	181	TESTIN1	-5600	-291
146	AVSS	-7350	-291	182	DBIST	-5550	-291
147	AVSS	-7300	-291	183	VSSDUM	-5500	-291
148	VDD	-7250	-291	184	VSSDUM	-5450	-291
149	VDD	-7200	-291	185	DSWAP1	-5400	-291
150	VDD	-7150	-291	186	TESTDUM	-5350	-291
151	VDD	-7100	-291	187	VSSDUM	-5300	-291
152	VDD	-7050	-291	188	DSWAP0	-5250	-291
153	VDD	-7000	-291	189	TEST19	-5200	-291
154	VDDI	-6950	-291	190	TEST18	-5150	-291
155	VDDI	-6900	-291	191	PSWAP	-5100	-291
156	VDDI	-6850	-291	192	TEST17	-5050	-291
157	VDDI	-6800	-291	193	TEST16	-5000	-291
158	VDDI	-6750	-291	194	IM2	-4950	-291
159	VDDI	-6700	-291	195	TEST15	-4900	-291
160	VDDI	-6650	-291	196	TEST14	-4850	-291
161	VDDI	-6600	-291	197	IM1	-4800	-291
162	VDDI	-6550	-291	198	TEST13	-4750	-291
163	VDDI	-6500	-291	199	TESTIN0	-4700	-291
164	VDDI	-6450	-291	200	IM0	-4650	-291
165	VDDI	-6400	-291	201	VSYNC	-4600	-291
166	VSS	-6350	-291	202	HSYNC	-4550	-291
167	VSS	-6300	-291	203	VSOUT	-4500	-291
168	VSS	-6250	-291	204	VSSDUM	-4450	-291
169	VSS	-6200	-291	205	VSSDUM	-4400	-291
170	VSS	-6150	-291	206	HSOUT	-4350	-291
171	VSS	-6100	-291	207	VSSDUM	-4300	-291
172	VSS	-6050	-291	208	VSSDUM	-4250	-291
173	VSS	-6000	-291	209	FTE1	-4200	-291
174	EN4PWR	-5950	-291	210	TEST12	-4150	-291
175	VSSDUM	-5900	-291	211	TEST11	-4100	-291
176	LEDPWM	-5850	-291	212	FTE	-4050	-291
177	BOOSTM1	-5800	-291	213	DE	-4000	-291
178	BOOSTM0	-5750	-291	214	TEST10	-3950	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
215	CSX	-3900	-291	251	AVSS	-2100	-291
216	TEST9	-3850	-291	252	AVSS	-2050	-291
217	TEST8	-3800	-291	253	AVSS	-2000	-291
218	DCX	-3750	-291	254	AVSS	-1950	-291
219	TEST7	-3700	-291	255	AVSS	-1900	-291
220	TEST6	-3650	-291	256	AVSS	-1850	-291
221	WRX_SCL	-3600	-291	257	AVSS	-1800	-291
222	TEST5	-3550	-291	258	AVSS	-1750	-291
223	TEST4	-3500	-291	259	AVSS	-1700	-291
224	SDO	-3450	-291	260	AVSS	-1650	-291
225	TEST3	-3400	-291	261	AVSS	-1600	-291
226	SDI	-3350	-291	262	AVDD	-1550	-291
227	TEST2	-3300	-291	263	AVDD	-1500	-291
228	TEST1	-3250	-291	264	AVDD	-1450	-291
229	TEST0	-3200	-291	265	AVDD	-1400	-291
230	RESX	-3150	-291	266	AVDD	-1350	-291
231	VSS	-3100	-291	267	AVDD	-1300	-291
232	VDDI	-3050	-291	268	AVDD	-1250	-291
233	VDDI	-3000	-291	269	AVDD	-1200	-291
234	VDDI	-2950	-291	270	AVDD	-1150	-291
235	VDDI	-2900	-291	271	AVDD	-1100	-291
236	VDDI	-2850	-291	272	AVDD	-1050	-291
237	VDDI	-2800	-291	273	AVDD	-1000	-291
238	VSS	-2750	-291	274	AVDD	-950	-291
239	VSS	-2700	-291	275	AVDD	-900	-291
240	VSS	-2650	-291	276	AVDD	-850	-291
241	VSS	-2600	-291	277	AVDD	-800	-291
242	VSS	-2550	-291	278	AVDD	-750	-291
243	VSS	-2500	-291	279	AVDD	-700	-291
244	VSS	-2450	-291	280	AVDD	-650	-291
245	VSS	-2400	-291	281	AVDD	-600	-291
246	VSS	-2350	-291	282	AVDD	-550	-291
247	VSS	-2300	-291	283	AVDD	-500	-291
248	VSS	-2250	-291	284	AVDD	-450	-291
249	VSS	-2200	-291	285	AVDD	-400	-291
250	AVSS	-2150	-291	286	AVDD	-350	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
287	AVDD	-300	-291	323	AVSS	1500	-291
288	AVDD	-250	-291	324	AVSS	1550	-291
289	VGS	-200	-291	325	AVSS	1600	-291
290	VGS	-150	-291	326	AVSS	1650	-291
291	VGS	-100	-291	327	AVSS	1700	-291
292	VGS	-50	-291	328	AVSS	1750	-291
293	VGS	0	-291	329	AVSS	1800	-291
294	VGS	50	-291	330	AVSS	1850	-291
295	AVEE	100	-291	331	AVSS	1900	-291
296	AVEE	150	-291	332	AVSS	1950	-291
297	AVEE	200	-291	333	AVSS	2000	-291
298	AVEE	250	-291	334	VSS	2050	-291
299	AVEE	300	-291	335	VSS	2100	-291
300	AVEE	350	-291	336	VSS	2150	-291
301	AVEE	400	-291	337	VSS	2200	-291
302	AVEE	450	-291	338	VSS	2250	-291
303	AVEE	500	-291	339	VSS	2300	-291
304	AVEE	550	-291	340	VSS	2350	-291
305	AVEE	600	-291	341	VSS	2400	-291
306	AVEE	650	-291	342	VSS	2450	-291
307	AVEE	700	-291	343	VSS	2500	-291
308	AVEE	750	-291	344	VSS	2550	-291
309	AVEE	800	-291	345	VSS	2600	-291
310	VCL	850	-291	346	VDD	2650	-291
311	VCL	900	-291	347	VDD	2700	-291
312	VCL	950	-291	348	VDD	2750	-291
313	VCL	1000	-291	349	VDD	2800	-291
314	VCL	1050	-291	350	VDD	2850	-291
315	VCL	1100	-291	351	VDD	2900	-291
316	VCL	1150	-291	352	VDDI	2950	-291
317	VCL	1200	-291	353	VDDI	3000	-291
318	VCL	1250	-291	354	VDDI	3050	-291
319	VCL	1300	-291	355	VSS	3100	-291
320	VCL	1350	-291	356	VSS	3150	-291
321	VCL	1400	-291	357	VSS	3200	-291
322	AVSS	1450	-291	358	VSS	3250	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
359	VSS	3300	-291	395	D1_N	5100	-291
360	VSS	3350	-291	396	D1_N	5150	-291
361	LVDSVSS	3400	-291	397	LVDSVSS	5200	-291
362	LVDSVSS	3450	-291	398	LVDSVSS	5250	-291
363	LVDSVSS	3500	-291	399	LVDSVSS	5300	-291
364	LVDSVSS	3550	-291	400	CLK_P	5350	-291
365	LVDSVSS	3600	-291	401	CLK_P	5400	-291
366	LVDSVSS	3650	-291	402	CLK_P	5450	-291
367	LVDSVSS	3700	-291	403	CLK_P	5500	-291
368	LVDSVSS	3750	-291	404	CLK_P	5550	-291
369	LVDSVSS	3800	-291	405	CLK_P	5600	-291
370	D2_P	3850	-291	406	CLK_N	5650	-291
371	D2_P	3900	-291	407	CLK_N	5700	-291
372	D2_P	3950	-291	408	CLK_N	5750	-291
373	D2_P	4000	-291	409	CLK_N	5800	-291
374	D2_P	4050	-291	410	CLK_N	5850	-291
375	D2_P	4100	-291	411	CLK_N	5900	-291
376	D2_N	4150	-291	412	LVDSVSS	5950	-291
377	D2_N	4200	-291	413	LVDSVSS	6000	-291
378	D2_N	4250	-291	414	LVDSVSS	6050	-291
379	D2_N	4300	-291	415	D0_P	6100	-291
380	D2_N	4350	-291	416	D0_P	6150	-291
381	D2_N	4400	-291	417	D0_P	6200	-291
382	LVDSVSS	4450	-291	418	D0_P	6250	-291
383	LVDSVSS	4500	-291	419	D0_P	6300	-291
384	LVDSVSS	4550	-291	420	D0_P	6350	-291
385	D1_P	4600	-291	421	D0_N	6400	-291
386	D1_P	4650	-291	422	D0_N	6450	-291
387	D1_P	4700	-291	423	D0_N	6500	-291
388	D1_P	4750	-291	424	D0_N	6550	-291
389	D1_P	4800	-291	425	D0_N	6600	-291
390	D1_P	4850	-291	426	D0_N	6650	-291
391	D1_N	4900	-291	427	LVDSVSS	6700	-291
392	D1_N	4950	-291	428	LVDSVSS	6750	-291
393	D1_N	5000	-291	429	LVDSVSS	6800	-291
394	D1_N	5050	-291	430	D3_P	6850	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
431	D3_P	6900	-291	467	AVSS	8700	-291
432	D3_P	6950	-291	468	AVSS	8750	-291
433	D3_P	7000	-291	469	AVSS	8800	-291
434	D3_P	7050	-291	470	AVSS	8850	-291
435	D3_P	7100	-291	471	AVSS	8900	-291
436	D3_N	7150	-291	472	AVSS	8950	-291
437	D3_N	7200	-291	473	AVSS	9000	-291
438	D3_N	7250	-291	474	AVSS	9050	-291
439	D3_N	7300	-291	475	COGTEST	9100	-291
440	D3_N	7350	-291	476	VCI1	9150	-291
441	D3_N	7400	-291	477	VCI1	9200	-291
442	VDDAM	7450	-291	478	VCI1	9250	-291
443	VDDAM	7500	-291	479	VCI1	9300	-291
444	VDDAM	7550	-291	480	COGTEST	9350	-291
445	VDDAM	7600	-291	481	VCL	9400	-291
446	VDDAM	7650	-291	482	VCL	9450	-291
447	VDDAM	7700	-291	483	VCL	9500	-291
448	VDDAM	7750	-291	484	VCL	9550	-291
449	VDDAM	7800	-291	485	VCL	9600	-291
450	VDDAM	7850	-291	486	VCL	9650	-291
451	LVDSVDD	7900	-291	487	AVDD	9700	-291
452	LVDSVDD	7950	-291	488	AVDD	9750	-291
453	LVDSVDD	8000	-291	489	AVDD	9800	-291
454	LVDSVDD	8050	-291	490	AVDD	9850	-291
455	LVDSVDD	8100	-291	491	AVDD	9900	-291
456	LVDSVDD	8150	-291	492	AVDD	9950	-291
457	VSS	8200	-291	493	AVDD	10000	-291
458	VSS	8250	-291	494	AVDD	10050	-291
459	VSS	8300	-291	495	AVDD	10100	-291
460	VSS	8350	-291	496	AVDD	10150	-291
461	VSS	8400	-291	497	AVDD	10200	-291
462	VSS	8450	-291	498	AVDD	10250	-291
463	VSS	8500	-291	499	AVDD	10300	-291
464	VSS	8550	-291	500	AVDD	10350	-291
465	VSS	8600	-291	501	AVDD	10400	-291
466	AVSS	8650	-291	502	AVDD	10450	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
503	AVDD	10500	-291	539	C31P	12300	-291
504	AVDD	10550	-291	540	C31P	12350	-291
505	AVDD	10600	-291	541	C31M	12400	-291
506	AVDD	10650	-291	542	C31M	12450	-291
507	AVDD	10700	-291	543	C31M	12500	-291
508	AVDD	10750	-291	544	C31M	12550	-291
509	AVDD	10800	-291	545	C31M	12600	-291
510	VSS	10850	-291	546	C31M	12650	-291
511	AVEE	10900	-291	547	C31M	12700	-291
512	AVEE	10950	-291	548	C31M	12750	-291
513	AVEE	11000	-291	549	C31M	12800	-291
514	AVEE	11050	-291	550	VGL	12850	-291
515	AVEE	11100	-291	551	VGL	12900	-291
516	AVEE	11150	-291	552	VGL	12950	-291
517	AVEE	11200	-291	553	VGL	13000	-291
518	AVEE	11250	-291	554	VGL	13050	-291
519	AVEE	11300	-291	555	VGL	13100	-291
520	AVEE	11350	-291	556	VGLO	13150	-291
521	AVEE	11400	-291	557	VGLO	13200	-291
522	AVEE	11450	-291	558	VGLO	13250	-291
523	AVEE	11500	-291	559	VGLO	13300	-291
524	AVEE	11550	-291	560	VGLO	13350	-291
525	AVEE	11600	-291	561	VGLO	13400	-291
526	AVEE	11650	-291	562	VSS	13450	-291
527	AVEE	11700	-291	563	VSS	13500	-291
528	AVEE	11750	-291	564	VSS	13550	-291
529	EXTN	11800	-291	565	VSS	13600	-291
530	EXTN	11850	-291	566	VSS	13650	-291
531	VSS	11900	-291	567	VSS	13700	-291
532	C31P	11950	-291	568	VGHO	13750	-291
533	C31P	12000	-291	569	VGHO	13800	-291
534	C31P	12050	-291	570	VGHO	13850	-291
535	C31P	12100	-291	571	AVSS	13900	-291
536	C31P	12150	-291	572	AVSS	13950	-291
537	C31P	12200	-291	573	AVSS	14000	-291
538	C31P	12250	-291	574	AVSS	14050	-291

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
575	AVSS	14100	-291	611	CGOUT7_R	14175	186
576	AVSS	14150	-291	612	CGOUT8_R	14157	306
577	VCOMDC	14200	-291	613	CGOUT8_R	14139	186
578	VCOMDC	14250	-291	614	CGOUT9_R	14121	306
579	VCOMDC	14300	-291	615	CGOUT9_R	14103	186
580	VCOMDC	14350	-291	616	CGOUT10_R	14085	306
581	VCOMDC	14400	-291	617	CGOUT10_R	14067	186
582	VCOMDC	14450	-291	618	VCOMDC	14049	306
583	DUMMY4	14500	-291	619	VCOMDC	14031	186
584	DUMMY4	14550	-291	620	VCOMDC	14013	306
585	DUMMY4	14600	-291	621	VCOMDC	13995	186
586	CGDUM_R1	14625	306	622	VCOMDC	13977	306
587	CGDUM_R1	14607	186	623	VCOMDC	13959	186
588	CGDUM_R1	14589	306	624	VCOMDC	13941	306
589	CGDUM_R1	14571	186	625	VCOMDC	13923	186
590	CGDUM_R1	14553	306	626	VCOMDC	13905	306
591	CGDUM_R1	14535	186	627	VCOMDC	13887	186
592	CGDUM_R1	14517	306	628	VCOMDC	13869	306
593	CGDUM_R1	14499	186	629	VCOMDC	13851	186
594	CGDUM_R1	14481	306	630	CGOUT11_R	13833	306
595	CGDUM_R1	14463	186	631	CGOUT11_R	13815	186
596	CGDUM_R1	14445	306	632	CGOUT12_R	13797	306
597	CGDUM_R1	14427	186	633	CGOUT12_R	13779	186
598	CGOUT1_R	14409	306	634	CGOUT13_R	13761	306
599	CGOUT1_R	14391	186	635	CGOUT13_R	13743	186
600	CGOUT2_R	14373	306	636	CGOUT14_R	13725	306
601	CGOUT2_R	14355	186	637	CGOUT14_R	13707	186
602	CGOUT3_R	14337	306	638	CGOUT15_R	13689	306
603	CGOUT3_R	14319	186	639	CGOUT15_R	13671	186
604	CGOUT4_R	14301	306	640	CGOUT16_R	13653	306
605	CGOUT4_R	14283	186	641	CGOUT16_R	13635	186
606	CGOUT5_R	14265	306	642	CGDUM_R2	13617	306
607	CGOUT5_R	14247	186	643	CGDUM_R2	13599	186
608	CGOUT6_R	14229	306	644	CGDUM_R2	13581	306
609	CGOUT6_R	14211	186	645	CGDUM_R2	13563	186
610	CGOUT7_R	14193	306	646	CGDUM_R2	13545	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
647	CGDUM_R2	13527	186	683	S1046	12879	186
648	SR1	13509	306	684	S1045	12861	306
649	S1080	13491	186	685	S1044	12843	186
650	S1079	13473	306	686	S1043	12825	306
651	S1078	13455	186	687	S1042	12807	186
652	S1077	13437	306	688	S1041	12789	306
653	S1076	13419	186	689	S1040	12771	186
654	S1075	13401	306	690	S1039	12753	306
655	S1074	13383	186	691	S1038	12735	186
656	S1073	13365	306	692	S1037	12717	306
657	S1072	13347	186	693	S1036	12699	186
658	S1071	13329	306	694	S1035	12681	306
659	S1070	13311	186	695	S1034	12663	186
660	S1069	13293	306	696	S1033	12645	306
661	S1068	13275	186	697	S1032	12627	186
662	S1067	13257	306	698	S1031	12609	306
663	S1066	13239	186	699	S1030	12591	186
664	S1065	13221	306	700	S1029	12573	306
665	S1064	13203	186	701	S1028	12555	186
666	S1063	13185	306	702	S1027	12537	306
667	S1062	13167	186	703	S1026	12519	186
668	S1061	13149	306	704	S1025	12501	306
669	S1060	13131	186	705	S1024	12483	186
670	S1059	13113	306	706	S1023	12465	306
671	S1058	13095	186	707	S1022	12447	186
672	S1057	13077	306	708	S1021	12429	306
673	S1056	13059	186	709	S1020	12411	186
674	S1055	13041	306	710	S1019	12393	306
675	S1054	13023	186	711	S1018	12375	186
676	S1053	13005	306	712	S1017	12357	306
677	S1052	12987	186	713	S1016	12339	186
678	S1051	12969	306	714	S1015	12321	306
679	S1050	12951	186	715	S1014	12303	186
680	S1049	12933	306	716	S1013	12285	306
681	S1048	12915	186	717	S1012	12267	186
682	S1047	12897	306	718	S1011	12249	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
719	S1010	12231	186	755	S974	11583	186
720	S1009	12213	306	756	S973	11565	306
721	S1008	12195	186	757	S972	11547	186
722	S1007	12177	306	758	S971	11529	306
723	S1006	12159	186	759	S970	11511	186
724	S1005	12141	306	760	S969	11493	306
725	S1004	12123	186	761	S968	11475	186
726	S1003	12105	306	762	S967	11457	306
727	S1002	12087	186	763	S966	11439	186
728	S1001	12069	306	764	S965	11421	306
729	S1000	12051	186	765	S964	11403	186
730	S999	12033	306	766	S963	11385	306
731	S998	12015	186	767	S962	11367	186
732	S997	11997	306	768	S961	11349	306
733	S996	11979	186	769	S960	11331	186
734	S995	11961	306	770	S959	11313	306
735	S994	11943	186	771	S958	11295	186
736	S993	11925	306	772	S957	11277	306
737	S992	11907	186	773	S956	11259	186
738	S991	11889	306	774	S955	11241	306
739	S990	11871	186	775	S954	11223	186
740	S989	11853	306	776	S953	11205	306
741	S988	11835	186	777	S952	11187	186
742	S987	11817	306	778	S951	11169	306
743	S986	11799	186	779	S950	11151	186
744	S985	11781	306	780	S949	11133	306
745	S984	11763	186	781	S948	11115	186
746	S983	11745	306	782	S947	11097	306
747	S982	11727	186	783	S946	11079	186
748	S981	11709	306	784	S945	11061	306
749	S980	11691	186	785	S944	11043	186
750	S979	11673	306	786	S943	11025	306
751	S978	11655	186	787	S942	11007	186
752	S977	11637	306	788	S941	10989	306
753	S976	11619	186	789	S940	10971	186
754	S975	11601	306	790	S939	10953	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
791	S938	10935	186	827	S902	10287	186
792	S937	10917	306	828	S901	10269	306
793	S936	10899	186	829	S900	10251	186
794	S935	10881	306	830	S899	10233	306
795	S934	10863	186	831	S898	10215	186
796	S933	10845	306	832	S897	10197	306
797	S932	10827	186	833	S896	10179	186
798	S931	10809	306	834	S895	10161	306
799	S930	10791	186	835	S894	10143	186
800	S929	10773	306	836	S893	10125	306
801	S928	10755	186	837	S892	10107	186
802	S927	10737	306	838	S891	10089	306
803	S926	10719	186	839	S890	10071	186
804	S925	10701	306	840	S889	10053	306
805	S924	10683	186	841	S888	10035	186
806	S923	10665	306	842	S887	10017	306
807	S922	10647	186	843	S886	9999	186
808	S921	10629	306	844	S885	9981	306
809	S920	10611	186	845	S884	9963	186
810	S919	10593	306	846	S883	9945	306
811	S918	10575	186	847	S882	9927	186
812	S917	10557	306	848	S881	9909	306
813	S916	10539	186	849	S880	9891	186
814	S915	10521	306	850	S879	9873	306
815	S914	10503	186	851	S878	9855	186
816	S913	10485	306	852	S877	9837	306
817	S912	10467	186	853	S876	9819	186
818	S911	10449	306	854	S875	9801	306
819	S910	10431	186	855	S874	9783	186
820	S909	10413	306	856	S873	9765	306
821	S908	10395	186	857	S872	9747	186
822	S907	10377	306	858	S871	9729	306
823	S906	10359	186	859	S870	9711	186
824	S905	10341	306	860	S869	9693	306
825	S904	10323	186	861	S868	9675	186
826	S903	10305	306	862	S867	9657	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
863	S866	9639	186	899	S830	8991	186
864	S865	9621	306	900	S829	8973	306
865	S864	9603	186	901	S828	8955	186
866	S863	9585	306	902	S827	8937	306
867	S862	9567	186	903	S826	8919	186
868	S861	9549	306	904	S825	8901	306
869	S860	9531	186	905	S824	8883	186
870	S859	9513	306	906	S823	8865	306
871	S858	9495	186	907	S822	8847	186
872	S857	9477	306	908	S821	8829	306
873	S856	9459	186	909	S820	8811	186
874	S855	9441	306	910	S819	8793	306
875	S854	9423	186	911	S818	8775	186
876	S853	9405	306	912	S817	8757	306
877	S852	9387	186	913	S816	8739	186
878	S851	9369	306	914	S815	8721	306
879	S850	9351	186	915	S814	8703	186
880	S849	9333	306	916	S813	8685	306
881	S848	9315	186	917	S812	8667	186
882	S847	9297	306	918	S811	8649	306
883	S846	9279	186	919	S810	8631	186
884	S845	9261	306	920	S809	8613	306
885	S844	9243	186	921	S808	8595	186
886	S843	9225	306	922	S807	8577	306
887	S842	9207	186	923	S806	8559	186
888	S841	9189	306	924	S805	8541	306
889	S840	9171	186	925	S804	8523	186
890	S839	9153	306	926	S803	8505	306
891	S838	9135	186	927	S802	8487	186
892	S837	9117	306	928	S801	8469	306
893	S836	9099	186	929	S800	8451	186
894	S835	9081	306	930	S799	8433	306
895	S834	9063	186	931	S798	8415	186
896	S833	9045	306	932	S797	8397	306
897	S832	9027	186	933	S796	8379	186
898	S831	9009	306	934	S795	8361	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
935	S794	8343	186	971	S758	7695	186
936	S793	8325	306	972	S757	7677	306
937	S792	8307	186	973	S756	7659	186
938	S791	8289	306	974	S755	7641	306
939	S790	8271	186	975	S754	7623	186
940	S789	8253	306	976	S753	7605	306
941	S788	8235	186	977	S752	7587	186
942	S787	8217	306	978	S751	7569	306
943	S786	8199	186	979	S750	7551	186
944	S785	8181	306	980	S749	7533	306
945	S784	8163	186	981	S748	7515	186
946	S783	8145	306	982	S747	7497	306
947	S782	8127	186	983	S746	7479	186
948	S781	8109	306	984	S745	7461	306
949	S780	8091	186	985	S744	7443	186
950	S779	8073	306	986	S743	7425	306
951	S778	8055	186	987	S742	7407	186
952	S777	8037	306	988	S741	7389	306
953	S776	8019	186	989	S740	7371	186
954	S775	8001	306	990	S739	7353	306
955	S774	7983	186	991	S738	7335	186
956	S773	7965	306	992	S737	7317	306
957	S772	7947	186	993	S736	7299	186
958	S771	7929	306	994	S735	7281	306
959	S770	7911	186	995	S734	7263	186
960	S769	7893	306	996	S733	7245	306
961	S768	7875	186	997	S732	7227	186
962	S767	7857	306	998	S731	7209	306
963	S766	7839	186	999	S730	7191	186
964	S765	7821	306	1000	S729	7173	306
965	S764	7803	186	1001	S728	7155	186
966	S763	7785	306	1002	S727	7137	306
967	S762	7767	186	1003	S726	7119	186
968	S761	7749	306	1004	S725	7101	306
969	S760	7731	186	1005	S724	7083	186
970	S759	7713	306	1006	S723	7065	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1007	S722	7047	186	1043	S686	6399	186
1008	S721	7029	306	1044	S685	6381	306
1009	S720	7011	186	1045	S684	6363	186
1010	S719	6993	306	1046	S683	6345	306
1011	S718	6975	186	1047	S682	6327	186
1012	S717	6957	306	1048	S681	6309	306
1013	S716	6939	186	1049	S680	6291	186
1014	S715	6921	306	1050	S679	6273	306
1015	S714	6903	186	1051	S678	6255	186
1016	S713	6885	306	1052	S677	6237	306
1017	S712	6867	186	1053	S676	6219	186
1018	S711	6849	306	1054	S675	6201	306
1019	S710	6831	186	1055	S674	6183	186
1020	S709	6813	306	1056	S673	6165	306
1021	S708	6795	186	1057	S672	6147	186
1022	S707	6777	306	1058	S671	6129	306
1023	S706	6759	186	1059	S670	6111	186
1024	S705	6741	306	1060	S669	6093	306
1025	S704	6723	186	1061	S668	6075	186
1026	S703	6705	306	1062	S667	6057	306
1027	S702	6687	186	1063	S666	6039	186
1028	S701	6669	306	1064	S665	6021	306
1029	S700	6651	186	1065	S664	6003	186
1030	S699	6633	306	1066	S663	5985	306
1031	S698	6615	186	1067	S662	5967	186
1032	S697	6597	306	1068	S661	5949	306
1033	S696	6579	186	1069	S660	5931	186
1034	S695	6561	306	1070	S659	5913	306
1035	S694	6543	186	1071	S658	5895	186
1036	S693	6525	306	1072	S657	5877	306
1037	S692	6507	186	1073	S656	5859	186
1038	S691	6489	306	1074	S655	5841	306
1039	S690	6471	186	1075	S654	5823	186
1040	S689	6453	306	1076	S653	5805	306
1041	S688	6435	186	1077	S652	5787	186
1042	S687	6417	306	1078	S651	5769	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1079	S650	5751	186	1115	S614	5103	186
1080	S649	5733	306	1116	S613	5085	306
1081	S648	5715	186	1117	S612	5067	186
1082	S647	5697	306	1118	S611	5049	306
1083	S646	5679	186	1119	S610	5031	186
1084	S645	5661	306	1120	S609	5013	306
1085	S644	5643	186	1121	S608	4995	186
1086	S643	5625	306	1122	S607	4977	306
1087	S642	5607	186	1123	S606	4959	186
1088	S641	5589	306	1124	S605	4941	306
1089	S640	5571	186	1125	S604	4923	186
1090	S639	5553	306	1126	S603	4905	306
1091	S638	5535	186	1127	S602	4887	186
1092	S637	5517	306	1128	S601	4869	306
1093	S636	5499	186	1129	S600	4851	186
1094	S635	5481	306	1130	S599	4833	306
1095	S634	5463	186	1131	S598	4815	186
1096	S633	5445	306	1132	S597	4797	306
1097	S632	5427	186	1133	S596	4779	186
1098	S631	5409	306	1134	S595	4761	306
1099	S630	5391	186	1135	S594	4743	186
1100	S629	5373	306	1136	S593	4725	306
1101	S628	5355	186	1137	S592	4707	186
1102	S627	5337	306	1138	S591	4689	306
1103	S626	5319	186	1139	S590	4671	186
1104	S625	5301	306	1140	S589	4653	306
1105	S624	5283	186	1141	S588	4635	186
1106	S623	5265	306	1142	S587	4617	306
1107	S622	5247	186	1143	S586	4599	186
1108	S621	5229	306	1144	S585	4581	306
1109	S620	5211	186	1145	S584	4563	186
1110	S619	5193	306	1146	S583	4545	306
1111	S618	5175	186	1147	S582	4527	186
1112	S617	5157	306	1148	S581	4509	306
1113	S616	5139	186	1149	S580	4491	186
1114	S615	5121	306	1150	S579	4473	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1151	S578	4455	186	1187	S542	3807	186
1152	S577	4437	306	1188	S541	3789	306
1153	S576	4419	186	1189	DUMMY	3771	186
1154	S575	4401	306	1190	DUMMY	3753	306
1155	S574	4383	186	1191	DUMMY	3735	186
1156	S573	4365	306	1192	DUMMY	3717	306
1157	S572	4347	186	1193	DUMMY	3699	186
1158	S571	4329	306	1194	DUMMY	3681	306
1159	S570	4311	186	1195	DUMMY	3645	186
1160	S569	4293	306	1196	DUMMY	3627	306
1161	S568	4275	186	1197	DUMMY	3573	186
1162	S567	4257	306	1198	DUMMY	3555	306
1163	S566	4239	186	1199	DUMMY	3501	186
1164	S565	4221	306	1200	DUMMY	3483	306
1165	S564	4203	186	1201	DUMMY	3429	186
1166	S563	4185	306	1202	DUMMY	3411	306
1167	S562	4167	186	1203	DUMMY	3357	186
1168	S561	4149	306	1204	DUMMY	3339	306
1169	S560	4131	186	1205	DUMMY	3285	186
1170	S559	4113	306	1206	DUMMY	3267	306
1171	S558	4095	186	1207	DUMMY	3213	186
1172	S557	4077	306	1208	DUMMY	3195	306
1173	S556	4059	186	1209	DUMMY	3141	186
1174	S555	4041	306	1210	DUMMY	3123	306
1175	S554	4023	186	1211	DUMMY	3069	186
1176	S553	4005	306	1212	DUMMY	3051	306
1177	S552	3987	186	1213	DUMMY	2997	186
1178	S551	3969	306	1214	DUMMY	2979	306
1179	S550	3951	186	1215	DUMMY	2925	186
1180	S549	3933	306	1216	DUMMY	2907	306
1181	S548	3915	186	1217	DUMMY	2853	186
1182	S547	3897	306	1218	DUMMY	2835	306
1183	S546	3879	186	1219	DUMMY	2781	186
1184	S545	3861	306	1220	DUMMY	2763	306
1185	S544	3843	186	1221	DUMMY	2709	186
1186	S543	3825	306	1222	DUMMY	2691	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1223	DUMMY	2637	186	1259	DUMMY	1341	186
1224	DUMMY	2619	306	1260	DUMMY	1323	306
1225	DUMMY	2565	186	1261	DUMMY	1269	186
1226	DUMMY	2547	306	1262	DUMMY	1251	306
1227	DUMMY	2493	186	1263	DUMMY	1197	186
1228	DUMMY	2475	306	1264	DUMMY	1179	306
1229	DUMMY	2421	186	1265	DUMMY	1125	186
1230	DUMMY	2403	306	1266	DUMMY	1107	306
1231	DUMMY	2349	186	1267	DUMMY	1053	186
1232	DUMMY	2331	306	1268	DUMMY	1035	306
1233	DUMMY	2277	186	1269	DUMMY	981	186
1234	DUMMY	2259	306	1270	DUMMY	963	306
1235	DUMMY	2205	186	1271	DUMMY	909	186
1236	DUMMY	2187	306	1272	DUMMY	891	306
1237	DUMMY	2133	186	1273	DUMMY	837	186
1238	DUMMY	2115	306	1274	DUMMY	819	306
1239	DUMMY	2061	186	1275	DUMMY	765	186
1240	DUMMY	2043	306	1276	DUMMY	747	306
1241	DUMMY	1989	186	1277	DUMMY	693	186
1242	DUMMY	1971	306	1278	DUMMY	675	306
1243	DUMMY	1917	186	1279	DUMMY	621	186
1244	DUMMY	1899	306	1280	DUMMY	603	306
1245	DUMMY	1845	186	1281	DUMMY	549	186
1246	DUMMY	1827	306	1282	DUMMY	531	306
1247	DUMMY	1773	186	1283	DUMMY	477	186
1248	DUMMY	1755	306	1284	DUMMY	459	306
1249	DUMMY	1701	186	1285	DUMMY	405	186
1250	DUMMY	1683	306	1286	DUMMY	387	306
1251	DUMMY	1629	186	1287	DUMMY	333	186
1252	DUMMY	1611	306	1288	DUMMY	315	306
1253	DUMMY	1557	186	1289	DUMMY	261	186
1254	DUMMY	1539	306	1290	DUMMY	243	306
1255	DUMMY	1485	186	1291	DUMMY	189	186
1256	DUMMY	1467	306	1292	DUMMY	171	306
1257	DUMMY	1413	186	1293	DUMMY	117	186
1258	DUMMY	1395	306	1294	DUMMY	99	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1295	DUMMY	45	186	1331	DUMMY	-1251	186
1296	DUMMY	27	306	1332	DUMMY	-1269	306
1297	DUMMY	-27	186	1333	DUMMY	-1323	186
1298	DUMMY	-45	306	1334	DUMMY	-1341	306
1299	DUMMY	-99	186	1335	DUMMY	-1395	186
1300	DUMMY	-117	306	1336	DUMMY	-1413	306
1301	DUMMY	-171	186	1337	DUMMY	-1467	186
1302	DUMMY	-189	306	1338	DUMMY	-1485	306
1303	DUMMY	-243	186	1339	DUMMY	-1539	186
1304	DUMMY	-261	306	1340	DUMMY	-1557	306
1305	DUMMY	-315	186	1341	DUMMY	-1611	186
1306	DUMMY	-333	306	1342	DUMMY	-1629	306
1307	DUMMY	-387	186	1343	DUMMY	-1683	186
1308	DUMMY	-405	306	1344	DUMMY	-1701	306
1309	DUMMY	-459	186	1345	DUMMY	-1755	186
1310	DUMMY	-477	306	1346	DUMMY	-1773	306
1311	DUMMY	-531	186	1347	DUMMY	-1827	186
1312	DUMMY	-549	306	1348	DUMMY	-1845	306
1313	DUMMY	-603	186	1349	DUMMY	-1899	186
1314	DUMMY	-621	306	1350	DUMMY	-1917	306
1315	DUMMY	-675	186	1351	DUMMY	-1971	186
1316	DUMMY	-693	306	1352	DUMMY	-1989	306
1317	DUMMY	-747	186	1353	DUMMY	-2043	186
1318	DUMMY	-765	306	1354	DUMMY	-2061	306
1319	DUMMY	-819	186	1355	DUMMY	-2115	186
1320	DUMMY	-837	306	1356	DUMMY	-2133	306
1321	DUMMY	-891	186	1357	DUMMY	-2187	186
1322	DUMMY	-909	306	1358	DUMMY	-2205	306
1323	DUMMY	-963	186	1359	DUMMY	-2259	186
1324	DUMMY	-981	306	1360	DUMMY	-2277	306
1325	DUMMY	-1035	186	1361	DUMMY	-2331	186
1326	DUMMY	-1053	306	1362	DUMMY	-2349	306
1327	DUMMY	-1107	186	1363	DUMMY	-2403	186
1328	DUMMY	-1125	306	1364	DUMMY	-2421	306
1329	DUMMY	-1179	186	1365	DUMMY	-2475	186
1330	DUMMY	-1197	306	1366	DUMMY	-2493	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1367	DUMMY	-2547	186	1403	DUMMY	-3753	186
1368	DUMMY	-2565	306	1404	DUMMY	-3771	306
1369	DUMMY	-2619	186	1405	S540	-3789	186
1370	DUMMY	-2637	306	1406	S539	-3807	306
1371	DUMMY	-2691	186	1407	S538	-3825	186
1372	DUMMY	-2709	306	1408	S537	-3843	306
1373	DUMMY	-2763	186	1409	S536	-3861	186
1374	DUMMY	-2781	306	1410	S535	-3879	306
1375	DUMMY	-2835	186	1411	S534	-3897	186
1376	DUMMY	-2853	306	1412	S533	-3915	306
1377	DUMMY	-2907	186	1413	S532	-3933	186
1378	DUMMY	-2925	306	1414	S531	-3951	306
1379	DUMMY	-2979	186	1415	S530	-3969	186
1380	DUMMY	-2997	306	1416	S529	-3987	306
1381	DUMMY	-3051	186	1417	S528	-4005	186
1382	DUMMY	-3069	306	1418	S527	-4023	306
1383	DUMMY	-3123	186	1419	S526	-4041	186
1384	DUMMY	-3141	306	1420	S525	-4059	306
1385	DUMMY	-3195	186	1421	S524	-4077	186
1386	DUMMY	-3213	306	1422	S523	-4095	306
1387	DUMMY	-3267	186	1423	S522	-4113	186
1388	DUMMY	-3285	306	1424	S521	-4131	306
1389	DUMMY	-3339	186	1425	S520	-4149	186
1390	DUMMY	-3357	306	1426	S519	-4167	306
1391	DUMMY	-3411	186	1427	S518	-4185	186
1392	DUMMY	-3429	306	1428	S517	-4203	306
1393	DUMMY	-3483	186	1429	S516	-4221	186
1394	DUMMY	-3501	306	1430	S515	-4239	306
1395	DUMMY	-3555	186	1431	S514	-4257	186
1396	DUMMY	-3573	306	1432	S513	-4275	306
1397	DUMMY	-3627	186	1433	S512	-4293	186
1398	DUMMY	-3645	306	1434	S511	-4311	306
1399	DUMMY	-3681	186	1435	S510	-4329	186
1400	DUMMY	-3699	306	1436	S509	-4347	306
1401	DUMMY	-3717	186	1437	S508	-4365	186
1402	DUMMY	-3735	306	1438	S507	-4383	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1439	S506	-4401	186	1475	S470	-5049	186
1440	S505	-4419	306	1476	S469	-5067	306
1441	S504	-4437	186	1477	S468	-5085	186
1442	S503	-4455	306	1478	S467	-5103	306
1443	S502	-4473	186	1479	S466	-5121	186
1444	S501	-4491	306	1480	S465	-5139	306
1445	S500	-4509	186	1481	S464	-5157	186
1446	S499	-4527	306	1482	S463	-5175	306
1447	S498	-4545	186	1483	S462	-5193	186
1448	S497	-4563	306	1484	S461	-5211	306
1449	S496	-4581	186	1485	S460	-5229	186
1450	S495	-4599	306	1486	S459	-5247	306
1451	S494	-4617	186	1487	S458	-5265	186
1452	S493	-4635	306	1488	S457	-5283	306
1453	S492	-4653	186	1489	S456	-5301	186
1454	S491	-4671	306	1490	S455	-5319	306
1455	S490	-4689	186	1491	S454	-5337	186
1456	S489	-4707	306	1492	S453	-5355	306
1457	S488	-4725	186	1493	S452	-5373	186
1458	S487	-4743	306	1494	S451	-5391	306
1459	S486	-4761	186	1495	S450	-5409	186
1460	S485	-4779	306	1496	S449	-5427	306
1461	S484	-4797	186	1497	S448	-5445	186
1462	S483	-4815	306	1498	S447	-5463	306
1463	S482	-4833	186	1499	S446	-5481	186
1464	S481	-4851	306	1500	S445	-5499	306
1465	S480	-4869	186	1501	S444	-5517	186
1466	S479	-4887	306	1502	S443	-5535	306
1467	S478	-4905	186	1503	S442	-5553	186
1468	S477	-4923	306	1504	S441	-5571	306
1469	S476	-4941	186	1505	S440	-5589	186
1470	S475	-4959	306	1506	S439	-5607	306
1471	S474	-4977	186	1507	S438	-5625	186
1472	S473	-4995	306	1508	S437	-5643	306
1473	S472	-5013	186	1509	S436	-5661	186
1474	S471	-5031	306	1510	S435	-5679	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1511	S434	-5697	186	1547	S398	-6345	186
1512	S433	-5715	306	1548	S397	-6363	306
1513	S432	-5733	186	1549	S396	-6381	186
1514	S431	-5751	306	1550	S395	-6399	306
1515	S430	-5769	186	1551	S394	-6417	186
1516	S429	-5787	306	1552	S393	-6435	306
1517	S428	-5805	186	1553	S392	-6453	186
1518	S427	-5823	306	1554	S391	-6471	306
1519	S426	-5841	186	1555	S390	-6489	186
1520	S425	-5859	306	1556	S389	-6507	306
1521	S424	-5877	186	1557	S388	-6525	186
1522	S423	-5895	306	1558	S387	-6543	306
1523	S422	-5913	186	1559	S386	-6561	186
1524	S421	-5931	306	1560	S385	-6579	306
1525	S420	-5949	186	1561	S384	-6597	186
1526	S419	-5967	306	1562	S383	-6615	306
1527	S418	-5985	186	1563	S382	-6633	186
1528	S417	-6003	306	1564	S381	-6651	306
1529	S416	-6021	186	1565	S380	-6669	186
1530	S415	-6039	306	1566	S379	-6687	306
1531	S414	-6057	186	1567	S378	-6705	186
1532	S413	-6075	306	1568	S377	-6723	306
1533	S412	-6093	186	1569	S376	-6741	186
1534	S411	-6111	306	1570	S375	-6759	306
1535	S410	-6129	186	1571	S374	-6777	186
1536	S409	-6147	306	1572	S373	-6795	306
1537	S408	-6165	186	1573	S372	-6813	186
1538	S407	-6183	306	1574	S371	-6831	306
1539	S406	-6201	186	1575	S370	-6849	186
1540	S405	-6219	306	1576	S369	-6867	306
1541	S404	-6237	186	1577	S368	-6885	186
1542	S403	-6255	306	1578	S367	-6903	306
1543	S402	-6273	186	1579	S366	-6921	186
1544	S401	-6291	306	1580	S365	-6939	306
1545	S400	-6309	186	1581	S364	-6957	186
1546	S399	-6327	306	1582	S363	-6975	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1583	S362	-6993	186	1619	S326	-7641	186
1584	S361	-7011	306	1620	S325	-7659	306
1585	S360	-7029	186	1621	S324	-7677	186
1586	S359	-7047	306	1622	S323	-7695	306
1587	S358	-7065	186	1623	S322	-7713	186
1588	S357	-7083	306	1624	S321	-7731	306
1589	S356	-7101	186	1625	S320	-7749	186
1590	S355	-7119	306	1626	S319	-7767	306
1591	S354	-7137	186	1627	S318	-7785	186
1592	S353	-7155	306	1628	S317	-7803	306
1593	S352	-7173	186	1629	S316	-7821	186
1594	S351	-7191	306	1630	S315	-7839	306
1595	S350	-7209	186	1631	S314	-7857	186
1596	S349	-7227	306	1632	S313	-7875	306
1597	S348	-7245	186	1633	S312	-7893	186
1598	S347	-7263	306	1634	S311	-7911	306
1599	S346	-7281	186	1635	S310	-7929	186
1600	S345	-7299	306	1636	S309	-7947	306
1601	S344	-7317	186	1637	S308	-7965	186
1602	S343	-7335	306	1638	S307	-7983	306
1603	S342	-7353	186	1639	S306	-8001	186
1604	S341	-7371	306	1640	S305	-8019	306
1605	S340	-7389	186	1641	S304	-8037	186
1606	S339	-7407	306	1642	S303	-8055	306
1607	S338	-7425	186	1643	S302	-8073	186
1608	S337	-7443	306	1644	S301	-8091	306
1609	S336	-7461	186	1645	S300	-8109	186
1610	S335	-7479	306	1646	S299	-8127	306
1611	S334	-7497	186	1647	S298	-8145	186
1612	S333	-7515	306	1648	S297	-8163	306
1613	S332	-7533	186	1649	S296	-8181	186
1614	S331	-7551	306	1650	S295	-8199	306
1615	S330	-7569	186	1651	S294	-8217	186
1616	S329	-7587	306	1652	S293	-8235	306
1617	S328	-7605	186	1653	S292	-8253	186
1618	S327	-7623	306	1654	S291	-8271	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1655	S290	-8289	186	1691	S254	-8937	186
1656	S289	-8307	306	1692	S253	-8955	306
1657	S288	-8325	186	1693	S252	-8973	186
1658	S287	-8343	306	1694	S251	-8991	306
1659	S286	-8361	186	1695	S250	-9009	186
1660	S285	-8379	306	1696	S249	-9027	306
1661	S284	-8397	186	1697	S248	-9045	186
1662	S283	-8415	306	1698	S247	-9063	306
1663	S282	-8433	186	1699	S246	-9081	186
1664	S281	-8451	306	1700	S245	-9099	306
1665	S280	-8469	186	1701	S244	-9117	186
1666	S279	-8487	306	1702	S243	-9135	306
1667	S278	-8505	186	1703	S242	-9153	186
1668	S277	-8523	306	1704	S241	-9171	306
1669	S276	-8541	186	1705	S240	-9189	186
1670	S275	-8559	306	1706	S239	-9207	306
1671	S274	-8577	186	1707	S238	-9225	186
1672	S273	-8595	306	1708	S237	-9243	306
1673	S272	-8613	186	1709	S236	-9261	186
1674	S271	-8631	306	1710	S235	-9279	306
1675	S270	-8649	186	1711	S234	-9297	186
1676	S269	-8667	306	1712	S233	-9315	306
1677	S268	-8685	186	1713	S232	-9333	186
1678	S267	-8703	306	1714	S231	-9351	306
1679	S266	-8721	186	1715	S230	-9369	186
1680	S265	-8739	306	1716	S229	-9387	306
1681	S264	-8757	186	1717	S228	-9405	186
1682	S263	-8775	306	1718	S227	-9423	306
1683	S262	-8793	186	1719	S226	-9441	186
1684	S261	-8811	306	1720	S225	-9459	306
1685	S260	-8829	186	1721	S224	-9477	186
1686	S259	-8847	306	1722	S223	-9495	306
1687	S258	-8865	186	1723	S222	-9513	186
1688	S257	-8883	306	1724	S221	-9531	306
1689	S256	-8901	186	1725	S220	-9549	186
1690	S255	-8919	306	1726	S219	-9567	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1727	S218	-9585	186	1763	S182	-10233	186
1728	S217	-9603	306	1764	S181	-10251	306
1729	S216	-9621	186	1765	S180	-10269	186
1730	S215	-9639	306	1766	S179	-10287	306
1731	S214	-9657	186	1767	S178	-10305	186
1732	S213	-9675	306	1768	S177	-10323	306
1733	S212	-9693	186	1769	S176	-10341	186
1734	S211	-9711	306	1770	S175	-10359	306
1735	S210	-9729	186	1771	S174	-10377	186
1736	S209	-9747	306	1772	S173	-10395	306
1737	S208	-9765	186	1773	S172	-10413	186
1738	S207	-9783	306	1774	S171	-10431	306
1739	S206	-9801	186	1775	S170	-10449	186
1740	S205	-9819	306	1776	S169	-10467	306
1741	S204	-9837	186	1777	S168	-10485	186
1742	S203	-9855	306	1778	S167	-10503	306
1743	S202	-9873	186	1779	S166	-10521	186
1744	S201	-9891	306	1780	S165	-10539	306
1745	S200	-9909	186	1781	S164	-10557	186
1746	S199	-9927	306	1782	S163	-10575	306
1747	S198	-9945	186	1783	S162	-10593	186
1748	S197	-9963	306	1784	S161	-10611	306
1749	S196	-9981	186	1785	S160	-10629	186
1750	S195	-9999	306	1786	S159	-10647	306
1751	S194	-10017	186	1787	S158	-10665	186
1752	S193	-10035	306	1788	S157	-10683	306
1753	S192	-10053	186	1789	S156	-10701	186
1754	S191	-10071	306	1790	S155	-10719	306
1755	S190	-10089	186	1791	S154	-10737	186
1756	S189	-10107	306	1792	S153	-10755	306
1757	S188	-10125	186	1793	S152	-10773	186
1758	S187	-10143	306	1794	S151	-10791	306
1759	S186	-10161	186	1795	S150	-10809	186
1760	S185	-10179	306	1796	S149	-10827	306
1761	S184	-10197	186	1797	S148	-10845	186
1762	S183	-10215	306	1798	S147	-10863	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1799	S146	-10881	186	1835	S110	-11529	186
1800	S145	-10899	306	1836	S109	-11547	306
1801	S144	-10917	186	1837	S108	-11565	186
1802	S143	-10935	306	1838	S107	-11583	306
1803	S142	-10953	186	1839	S106	-11601	186
1804	S141	-10971	306	1840	S105	-11619	306
1805	S140	-10989	186	1841	S104	-11637	186
1806	S139	-11007	306	1842	S103	-11655	306
1807	S138	-11025	186	1843	S102	-11673	186
1808	S137	-11043	306	1844	S101	-11691	306
1809	S136	-11061	186	1845	S100	-11709	186
1810	S135	-11079	306	1846	S99	-11727	306
1811	S134	-11097	186	1847	S98	-11745	186
1812	S133	-11115	306	1848	S97	-11763	306
1813	S132	-11133	186	1849	S96	-11781	186
1814	S131	-11151	306	1850	S95	-11799	306
1815	S130	-11169	186	1851	S94	-11817	186
1816	S129	-11187	306	1852	S93	-11835	306
1817	S128	-11205	186	1853	S92	-11853	186
1818	S127	-11223	306	1854	S91	-11871	306
1819	S126	-11241	186	1855	S90	-11889	186
1820	S125	-11259	306	1856	S89	-11907	306
1821	S124	-11277	186	1857	S88	-11925	186
1822	S123	-11295	306	1858	S87	-11943	306
1823	S122	-11313	186	1859	S86	-11961	186
1824	S121	-11331	306	1860	S85	-11979	306
1825	S120	-11349	186	1861	S84	-11997	186
1826	S119	-11367	306	1862	S83	-12015	306
1827	S118	-11385	186	1863	S82	-12033	186
1828	S117	-11403	306	1864	S81	-12051	306
1829	S116	-11421	186	1865	S80	-12069	186
1830	S115	-11439	306	1866	S79	-12087	306
1831	S114	-11457	186	1867	S78	-12105	186
1832	S113	-11475	306	1868	S77	-12123	306
1833	S112	-11493	186	1869	S76	-12141	186
1834	S111	-11511	306	1870	S75	-12159	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1871	S74	-12177	186	1907	S38	-12825	186
1872	S73	-12195	306	1908	S37	-12843	306
1873	S72	-12213	186	1909	S36	-12861	186
1874	S71	-12231	306	1910	S35	-12879	306
1875	S70	-12249	186	1911	S34	-12897	186
1876	S69	-12267	306	1912	S33	-12915	306
1877	S68	-12285	186	1913	S32	-12933	186
1878	S67	-12303	306	1914	S31	-12951	306
1879	S66	-12321	186	1915	S30	-12969	186
1880	S65	-12339	306	1916	S29	-12987	306
1881	S64	-12357	186	1917	S28	-13005	186
1882	S63	-12375	306	1918	S27	-13023	306
1883	S62	-12393	186	1919	S26	-13041	186
1884	S61	-12411	306	1920	S25	-13059	306
1885	S60	-12429	186	1921	S24	-13077	186
1886	S59	-12447	306	1922	S23	-13095	306
1887	S58	-12465	186	1923	S22	-13113	186
1888	S57	-12483	306	1924	S21	-13131	306
1889	S56	-12501	186	1925	S20	-13149	186
1890	S55	-12519	306	1926	S19	-13167	306
1891	S54	-12537	186	1927	S18	-13185	186
1892	S53	-12555	306	1928	S17	-13203	306
1893	S52	-12573	186	1929	S16	-13221	186
1894	S51	-12591	306	1930	S15	-13239	306
1895	S50	-12609	186	1931	S14	-13257	186
1896	S49	-12627	306	1932	S13	-13275	306
1897	S48	-12645	186	1933	S12	-13293	186
1898	S47	-12663	306	1934	S11	-13311	306
1899	S46	-12681	186	1935	S10	-13329	186
1900	S45	-12699	306	1936	S9	-13347	306
1901	S44	-12717	186	1937	S8	-13365	186
1902	S43	-12735	306	1938	S7	-13383	306
1903	S42	-12753	186	1939	S6	-13401	186
1904	S41	-12771	306	1940	S5	-13419	306
1905	S40	-12789	186	1941	S4	-13437	186
1906	S39	-12807	306	1942	S3	-13455	306

No.	PAD	X-axis	Y-axis	No.	PAD	X-axis	Y-axis
1943	S2	-13473	186	1979	CGOUT9_L	-14121	186
1944	S1	-13491	306	1980	CGOUT8_L	-14139	306
1945	SL1	-13509	186	1981	CGOUT8_L	-14157	186
1946	CGDUM_L2	-13527	306	1982	CGOUT7_L	-14175	306
1947	CGDUM_L2	-13545	186	1983	CGOUT7_L	-14193	186
1948	CGDUM_L2	-13563	306	1984	CGOUT6_L	-14211	306
1949	CGDUM_L2	-13581	186	1985	CGOUT6_L	-14229	186
1950	CGDUM_L2	-13599	306	1986	CGOUT5_L	-14247	306
1951	CGDUM_L2	-13617	186	1987	CGOUT5_L	-14265	186
1952	CGOUT16_L	-13635	306	1988	CGOUT4_L	-14283	306
1953	CGOUT16_L	-13653	186	1989	CGOUT4_L	-14301	186
1954	CGOUT15_L	-13671	306	1990	CGOUT3_L	-14319	306
1955	CGOUT15_L	-13689	186	1991	CGOUT3_L	-14337	186
1956	CGOUT14_L	-13707	306	1992	CGOUT2_L	-14355	306
1957	CGOUT14_L	-13725	186	1993	CGOUT2_L	-14373	186
1958	CGOUT13_L	-13743	306	1994	CGOUT1_L	-14391	306
1959	CGOUT13_L	-13761	186	1995	CGOUT1_L	-14409	186
1960	CGOUT12_L	-13779	306	1996	CGDUM_L1	-14427	306
1961	CGOUT12_L	-13797	186	1997	CGDUM_L1	-14445	186
1962	CGOUT11_L	-13815	306	1998	CGDUM_L1	-14463	306
1963	CGOUT11_L	-13833	186	1999	CGDUM_L1	-14481	186
1964	VCOMDC	-13851	306	2000	CGDUM_L1	-14499	306
1965	VCOMDC	-13869	186	2001	CGDUM_L1	-14517	186
1966	VCOMDC	-13887	306	2002	CGDUM_L1	-14535	306
1967	VCOMDC	-13905	186	2003	CGDUM_L1	-14553	186
1968	VCOMDC	-13923	306	2004	CGDUM_L1	-14571	306
1969	VCOMDC	-13941	186	2005	CGDUM_L1	-14589	186
1970	VCOMDC	-13959	306	2006	CGDUM_L1	-14607	306
1971	VCOMDC	-13977	186				
1972	VCOMDC	-13995	306				
1973	VCOMDC	-14013	186				
1974	VCOMDC	-14031	306				
1975	VCOMDC	-14049	186				
1976	CGOUT10_L	-14067	306				
1977	CGOUT10_L	-14085	186				
1978	CGOUT9_L	-14103	306				