XN06435 (XN6435)

Silicon PNP epitaxial planar type

For high-frequency amplification

■ Features

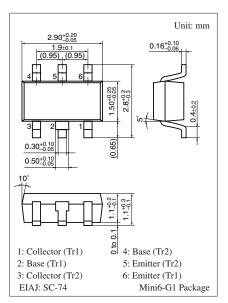
- Two elements incorporated into one package
- Reduction of the mounting area and assembly cost by one half

■ Basic Part Number

• 2SA1022 × 2

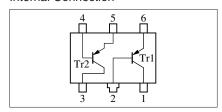
■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V_{CBO}	-30	V	
Collector-emitter voltage (Base open)	V _{CEO}	-20	V	
Emitter-base voltage (Collector open)	V _{EBO}	-5	V	
Collector current	I_C	-30	mA	
Total power dissipation	P _T	300	mW	
Junction temperature	T _j	150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	



Marking Symbol: 7W

Internal Connection



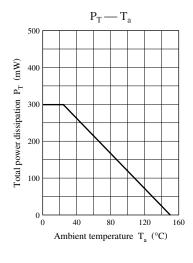
■ Electrical Characteristics $T_a = 25$ °C ± 3 °C

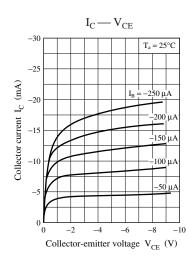
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Base-emitter voltage	V _{BE}	$V_{CE} = -10 \text{ V}, I_{C} = -1 \text{ mA}$		- 0.7		V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -10 \text{ V}, I_E = 0$			- 0.1	μΑ
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -20 \text{ V}, I_B = 0$			-100	μΑ
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -5 \text{ V}, I_C = 0$			-10	μΑ
Forward current transfer ratio	h _{FE}	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}$	50		220	_
h _{FE} ratio *	h _{FE(Small}	$V_{CB} = -10 \text{ V}, I_{E} = 1 \text{ mA}$	0.50	0.99		_
	/Large)					
Collector-emitter saturation voltage	V _{CE(sat)}	$I_C = -10 \text{ mA}, I_B = -1 \text{ mA}$		- 0.1		V
Transition frequency	f_T	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 200 \text{ MHz}$	150			MHz
Noise figure	NF	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 5 \text{ MHz}$		2.8		dB
Reverse transfer impedance	Z _{rb}	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 2 \text{ MHz}$		22		Ω
Reverse transfer capacitance	C _{re}	$V_{CE} = -10 \text{ V}, I_{E} = 1 \text{ mA}, f = 10.7 \text{ MHz}$		1.2		pF
(Common emitter)						

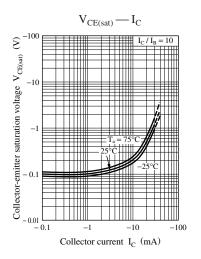
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

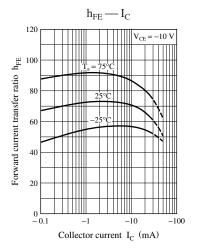
2. *: Ratio between 2 elements

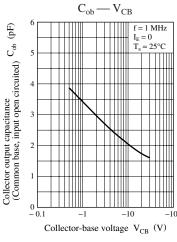
Note) The part number in the parenthesis shows conventional part number.

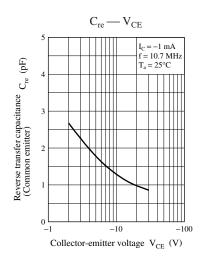


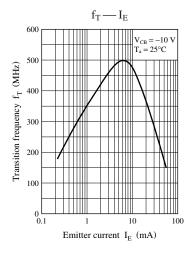


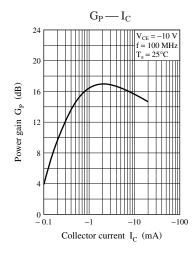


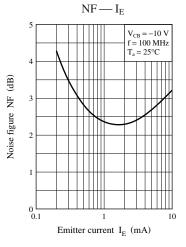












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