

# XN6114

## Silicon PNP epitaxial planer transistor

For switching/digital circuits

### ■ Features

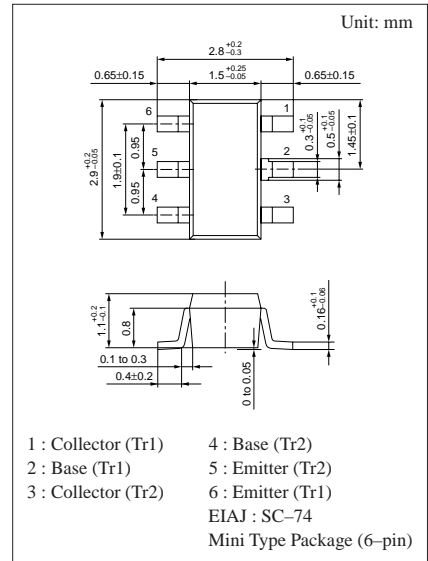
- Two elements incorporated into one package.  
(Transistors with built-in resistor)
- Reduction of the mounting area and assembly cost by one half.

### ■ Basic Part Number of Element

- UN1114 × 2 elements

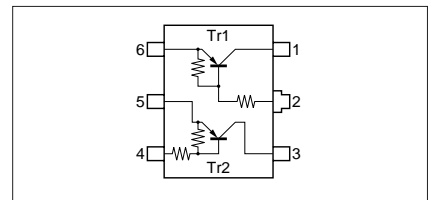
### ■ Absolute Maximum Ratings (Ta=25°C)

	Parameter	Symbol	Ratings	Unit
Rating of element	Collector to base voltage	$V_{CBO}$	-50	V
	Collector to emitter voltage	$V_{CEO}$	-50	V
	Collector current	$I_C$	-100	mA
Overall	Total power dissipation	$P_T$	300	mW
	Junction temperature	$T_j$	150	°C
	Storage temperature	$T_{stg}$	-55 to +150	°C



Marking Symbol: CK

Internal Connection



### ■ Electrical Characteristics (Ta=25°C)

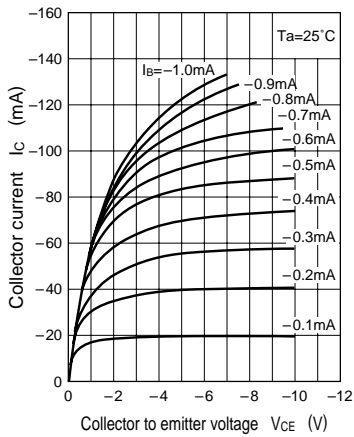
Parameter	Symbol	Conditions	min	typ	max	Unit
Collector to base voltage	$V_{CBO}$	$I_C = -10\mu A, I_E = 0$	-50			V
Collector to emitter voltage	$V_{CEO}$	$I_C = -2mA, I_B = 0$	-50			V
Collector cutoff current	$I_{CBO}$	$V_{CB} = -50V, I_E = 0$			-0.1	$\mu A$
	$I_{CEO}$	$V_{CE} = -50V, I_B = 0$			-0.5	$\mu A$
Emitter cutoff current	$I_{EBO}$	$V_{EB} = -6V, I_C = 0$			-0.2	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = -10V, I_C = -5mA$	80			
Forward current transfer $h_{FE}$ ratio	$h_{FE} (small/large)^{*1}$	$V_{CE} = -10V, I_C = -5mA$	0.5	0.99		
Collector to emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10mA, I_B = -0.3mA$			-0.25	V
Output voltage high level	$V_{OH}$	$V_{CC} = -5V, V_B = -0.5V, R_L = 1k\Omega$	-4.9			V
Output voltage low level	$V_{OL}$	$V_{CC} = -5V, V_B = -2.5V, R_L = 1k\Omega$			-0.2	V
Transition frequency	$f_T$	$V_{CB} = -10V, I_E = 1mA, f = 200MHz$		80		MHz
Input resistance	$R_1$		-30%	10	+30%	k $\Omega$
Resistance ratio	$R_1/R_2$		0.17	0.21	0.25	

\*1 Ratio between 2 elements

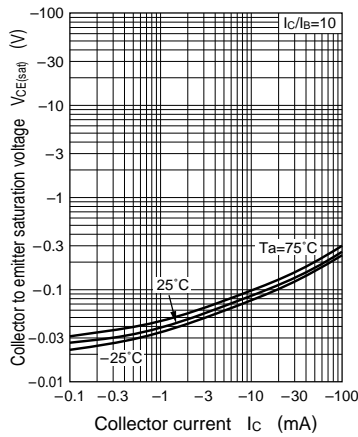
$P_T - T_a$



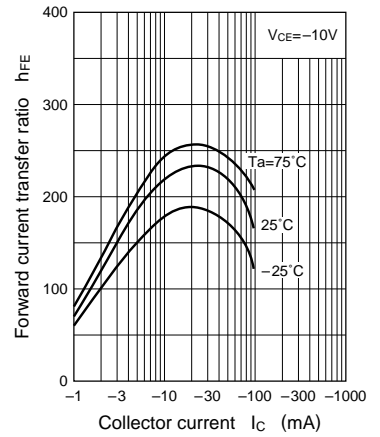
$I_C - V_{CE}$



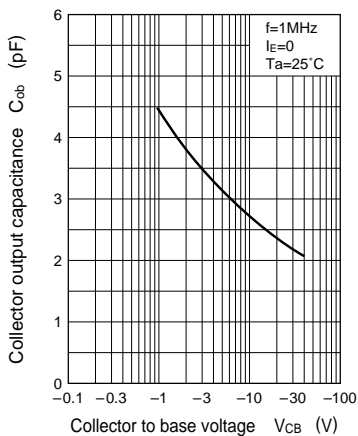
$V_{CE(sat)} - I_C$



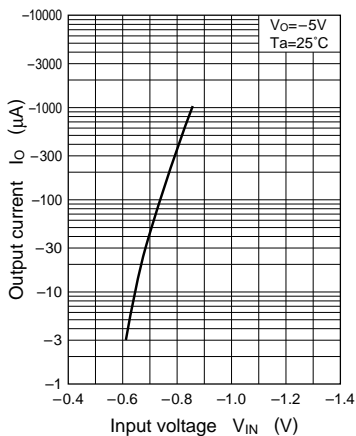
$h_{FE} - I_C$



$C_{ob} - V_{CB}$



$I_O - V_{IN}$



$V_{IN} - I_O$

