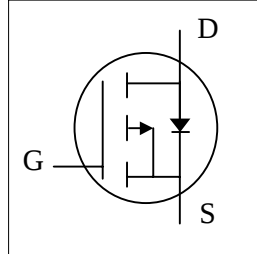


- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low Gate Charge
- ▼ RoHS Compliant & Halogen-Free

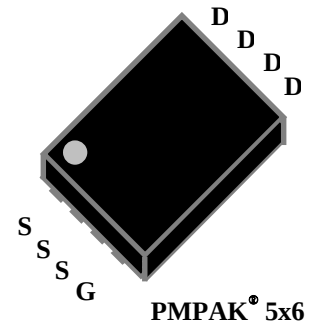


BV_{DSS}	-100V
$R_{DS(ON)}$	52m Ω

Description

XP1011AL series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



Absolute Maximum Ratings@ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V	-16	A
$I_D@T_C=100^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V	-10.1	A
$I_D@T_A=25^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V ³	-7.1	A
$I_D@T_A=70^{\circ}\text{C}$	Drain Current, V_{GS} @ 10V ³	-5.7	A
I_{DM}	Pulsed Drain Current ¹	-60	A
$P_D@T_C=25^{\circ}\text{C}$	Total Power Dissipation	25	W
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy ⁴	12.5	mJ
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-c}	Maximum Thermal Resistance, Junction-case	5	$^{\circ}\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-1mA	-100	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-6A	-	-	52	mΩ
		V _{GS} =-4.5V, I _D =-3A	-	-	72	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1.4	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-6A	-	15	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-80V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±0.1	uA
Q _g	Total Gate Charge ²	I _D =-6A V _{DS} =-50V V _{GS} =-10V	-	35	56	nC
Q _{gs}	Gate-Source Charge		-	6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge		-	9	-	nC
t _{d(on)}	Turn-on Delay Time		-	13.5	-	ns
t _r	Rise Time	I _D =-1A R _G =3.3Ω	-	6	-	ns
t _{d(off)}	Turn-off Delay Time		-	37	-	ns
t _f	Fall Time		-	42	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1530	2448	pF
C _{oss}	Output Capacitance	V _{DS} =-80V	-	200	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	20	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2	4	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-6A, V _{GS} =0V	-	-	-1.3	V
t _{rr}	Reverse Recovery Time	I _S =-6A, V _{GS} =0V, dI/dt=100A/μs	-	71	-	ns
Q _{rr}	Reverse Recovery Charge		-	215	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 85 °C/W on steady state.
- 4.Starting T_j=25°C , V_{DD}=-50V , L=1mH , R_G=25Ω , V_{GS}=10V

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.
XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED
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XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE
RELIABILITY, FUNCTION OR DESIGN.

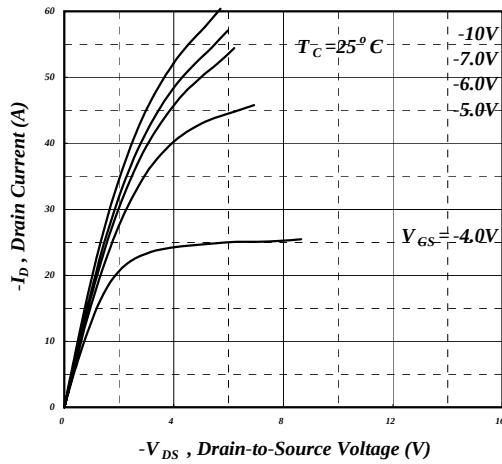


Fig 1. Typical Output Characteristics

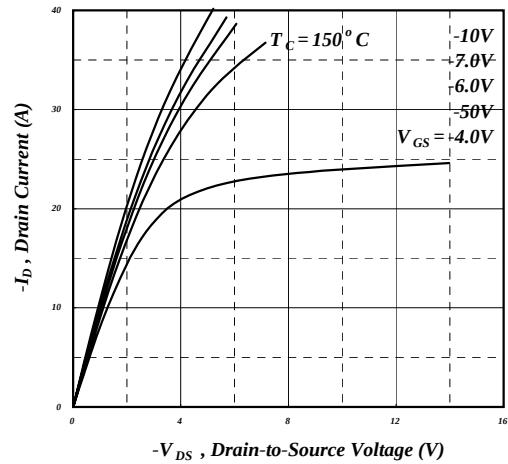


Fig 2. Typical Output Characteristics

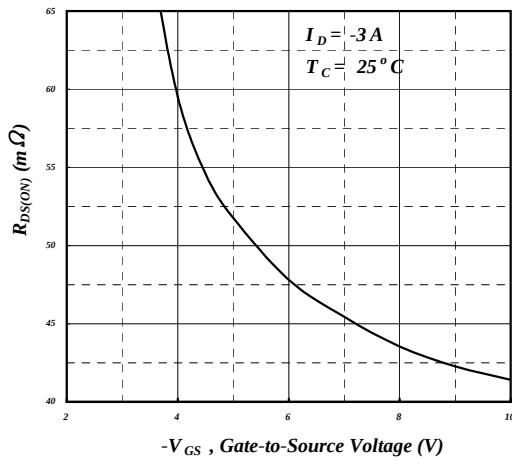
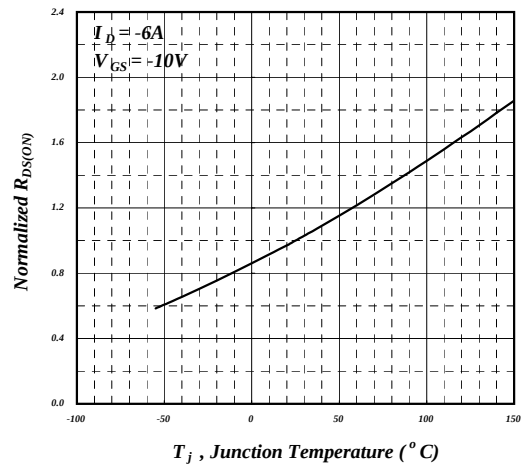
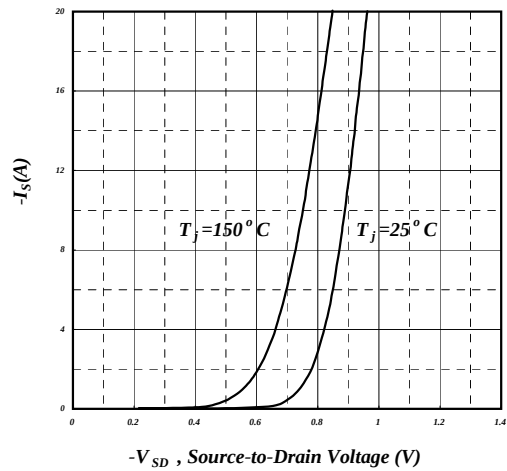


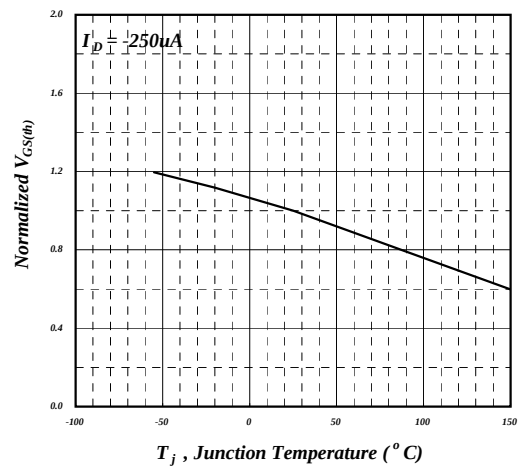
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

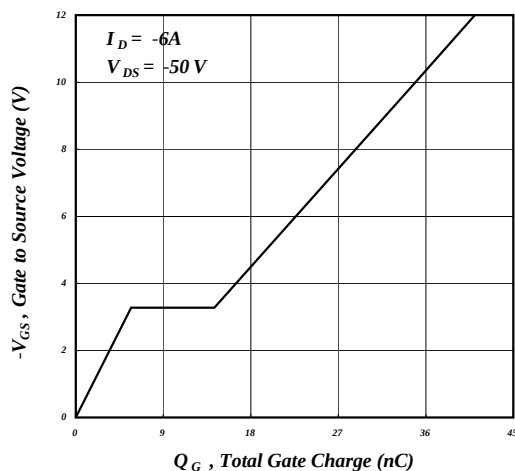


Fig 7. Gate Charge Characteristics

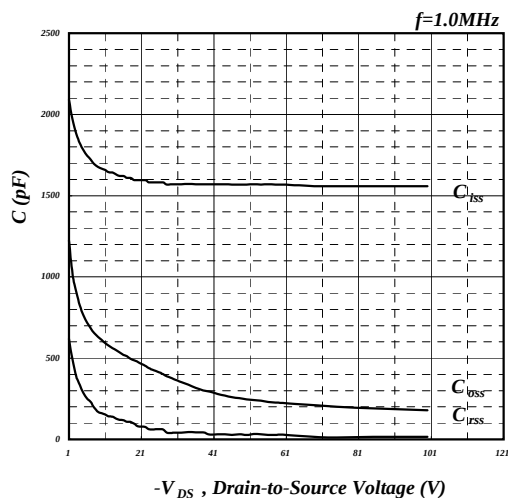


Fig 8. Typical Capacitance Characteristics

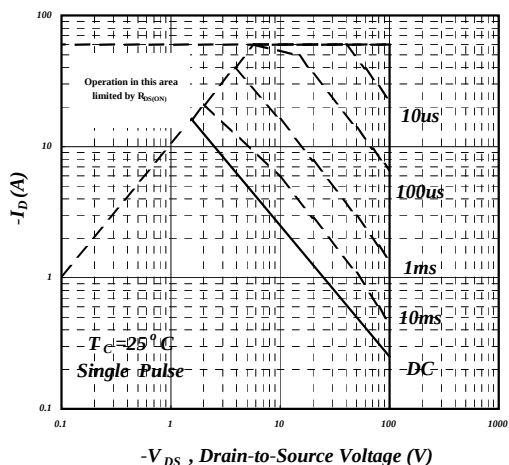


Fig 9. Maximum Safe Operating Area

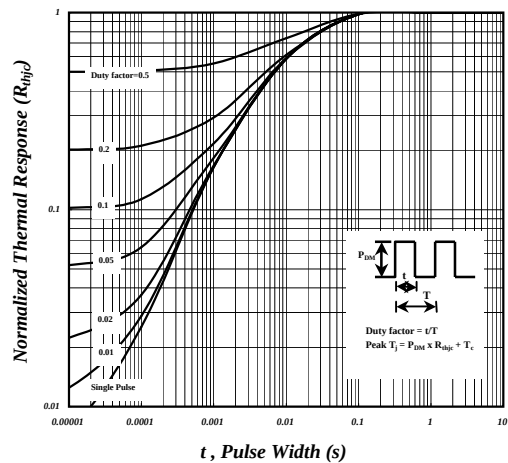


Fig 10. Effective Transient Thermal Impedance

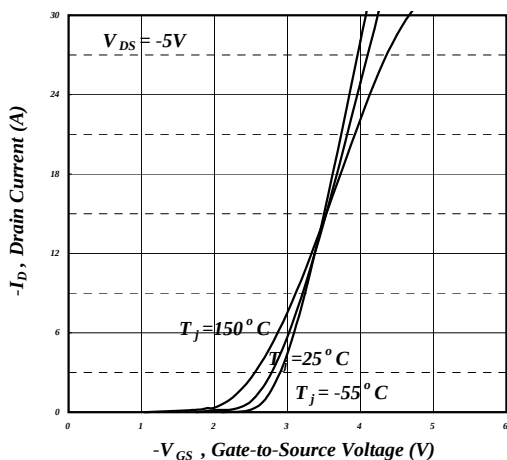


Fig 11. Transfer Characteristics

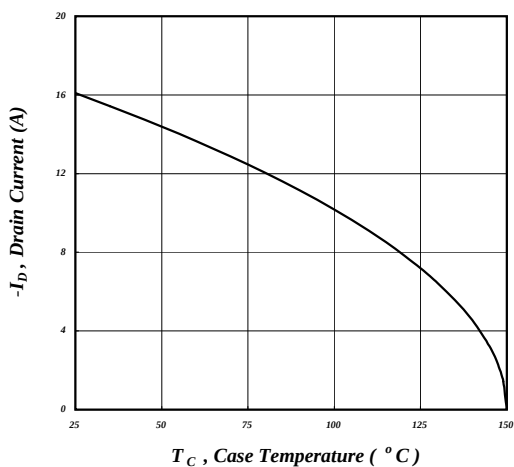


Fig 12. Drain Current v.s. Case Temperature

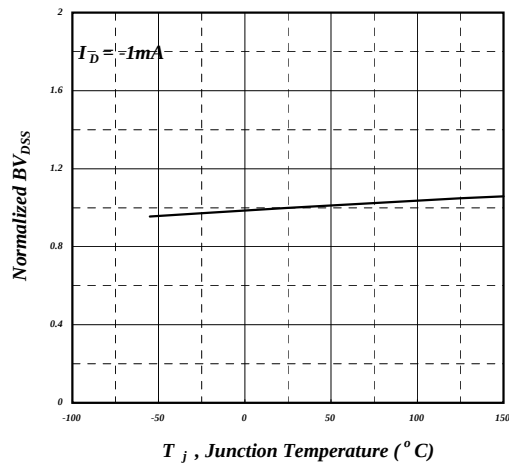


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

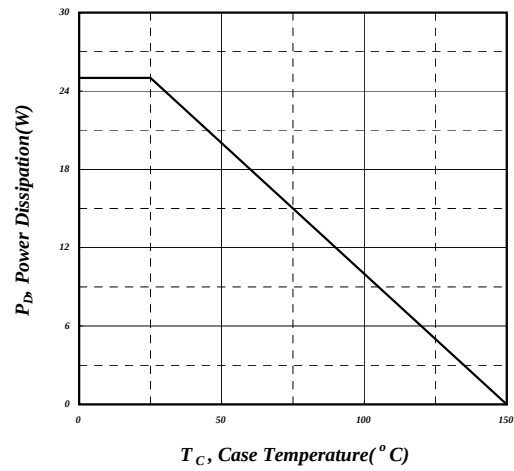


Fig 14. Total Power Dissipation

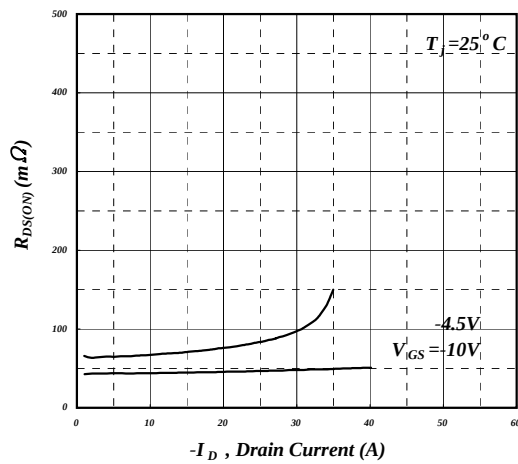
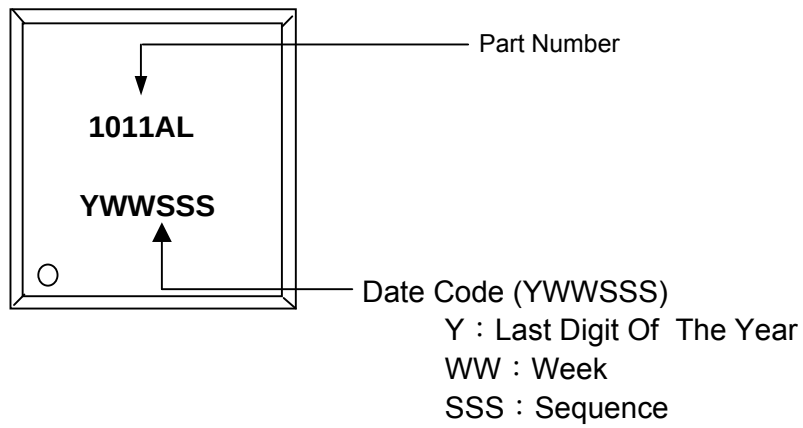
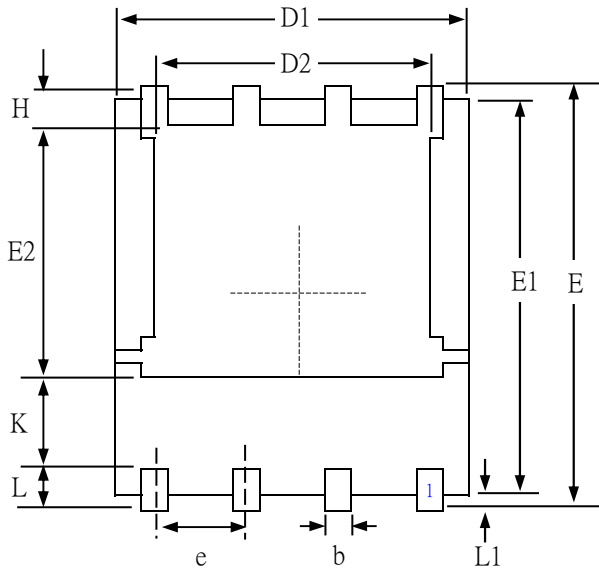


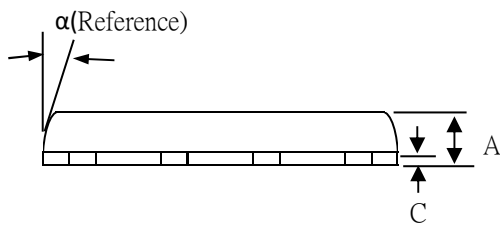
Fig 15. Typ. Drain-Source on State Resistance

MARKING INFORMATION

Package Outline : PMPAK 5x6



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.254(Ref.)		
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
$\alpha(\text{Ref.})$	0°	—	12°

- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

Technical drawing showing the front and top views of a mechanical part with the following dimensions:

- Front View (Top):**
 - Overall width: 5.1
 - Distance from left edge to centerline: 2.55
 - Height of the top section: 0.9
 - Height of the main body: 4.45
 - Distance from right edge to centerline: 3.25
 - Overall height: 6.5
- Top View (Bottom):**
 - Distance from left edge to first hole center: 0.95
 - Distance between first and second hole centers: 1.27
 - Distance between second and third hole centers: 0.72
 - Distance from fourth hole center to right edge: 0.55
 - Distance from top edge to first hole center: 1.1

Draw No. M1-MT-8-EIFMRL-G-v08