CoolRunner™ XPLA3 CPLD

DS012 (v1.1) March 3, 2000 — Advance Product Specification

Features

- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- Innovative XPLA3 architecture combines high speed with extreme flexibility
- Based on industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Advanced 0.35µ five metal layer E^2CMOS process
  - 1,000 erase/program cycles guaranteed
  - 20 years data retention guaranteed
- 3V, In-System Programmable (ISP) using JTAG IEEE 1149.1 interface
  - Full Boundary Scan Test (IEEE 1149.1)
- Ultra-low static power of less than 100 µA
- Simple deterministic timing model
- Support for complex asynchronous clocking
  - 16 product term clocks and four local control term clocks per logic block
  - Four global clocks and one universal control term clock per device
- Excellent pin retention during design changes
- 5V tolerant I/O pins
- Input register set up time of 1.7 ns
- Logic expandable to 48 product terms
- High-speed pin-to-pin delays of 5.0 ns
- Slew rate control per macrocell
- 100% routable
- Security bit prevents unauthorized access
- Supports hot-plugging capability
- Design entry/verification using Xilinx or industry standard CAE tools
- Innovative Control Term structure provides:
  - Asynchronous macrocell clocking
  - Asynchronous macrocell register preset/reset
  - Clock enable control per macrocell
- Four output enable controls per logic block
- Foldback NAND for synthesis optimization
- Global 3-state which facilitates "bed of nails" testing
- Available in Chip-scale BGA, and QFP packages
- Commercial and extended voltage industrial grades
- Pin compatible with existing CoolRunner low-power family devices

Family Overview

The CoolRunner XPLA3 (eXtended Programmable Logic Array) family of CPLDs is targeted for low power systems that include portable, handheld, and power sensitive applications. Each member of the XPLA3 family includes Fast Zero Power (FZP) design technology that combines low power and high speed. With this design technique, the XPLA3 family offers true pin-to-pin speeds of 5.0 ns, while simultaneously delivering power that is less than 100 µA at standby without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique.

To the original XPLA architecture, XPLA3 adds a direct input register path, multiple clocks (both dedicated and product term generated), and both reset and preset for each macrocell, with a full PLA structure. These enhancements deliver high speed coupled with very flexible logic allocation which results in the ability to make design changes without changing pinout. The XPLA3 logic block includes a pool of 48 product terms that can be allocated to any macrocell in the logic block. Logic that is common to multiple macrocells can be placed on a single PLA product term and shared, effectively increasing design density.

XPLA3 CPLDs are supported by WebPACK from Xilinx and industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Viewlogic, andd Synplicity), using text (ABEL, VHDL, Verilog) and schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses Xilinx developed tools including WebFITTER.

The XPLA3 family features also include industry-standard, IEEE 1149.1, JTAG interface through which In-System Programming (ISP) and reprogramming of the device can

occur. The XPLA3 CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, and SMS.

XPLA3 Architecture

Figure 1 shows a high-level block diagram of a 128 macrocell device implementing the XPLA3 architecture. The XPLA3 architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block has 36 inputs from the ZIA and 16 macrocells.

From this point of view, this architecture looks like many other CPLD architectures. What makes the XPLA3 family unique is logic allocation inside each logic block and the design technique used to implement these logic blocks.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains a PLA array that generates control terms, clock terms, and logic cells. There are 36 pairs of true and complement inputs from the ZIA that feed the 48 product terms in the array. Within the 48 P-terms there are eight local control terms (LCT[0:7]) available as control inputs to each macrocell for use as asynchronous clocks, resets, presets and output enables. The other P-terms serve as additional single inputs into each macrocell.

There are eight foldback NAND P-terms that are available for ease of fitting and pin locking. Sixteen product terms are coupled with the associated programmable OR gate into the VFM (Variable Function Multiplexer). The VFM increases logic optimization by implementing any two input logic funtion before entering the macrocell (see Figure 3).

Each macrocell can support combinatorial or registered inputs, preset and reset on a per macrocell basis and configurable D, T registers, or latch function. If a macrocell needs more product terms, it simply gets the additional product terms from the PLA array.

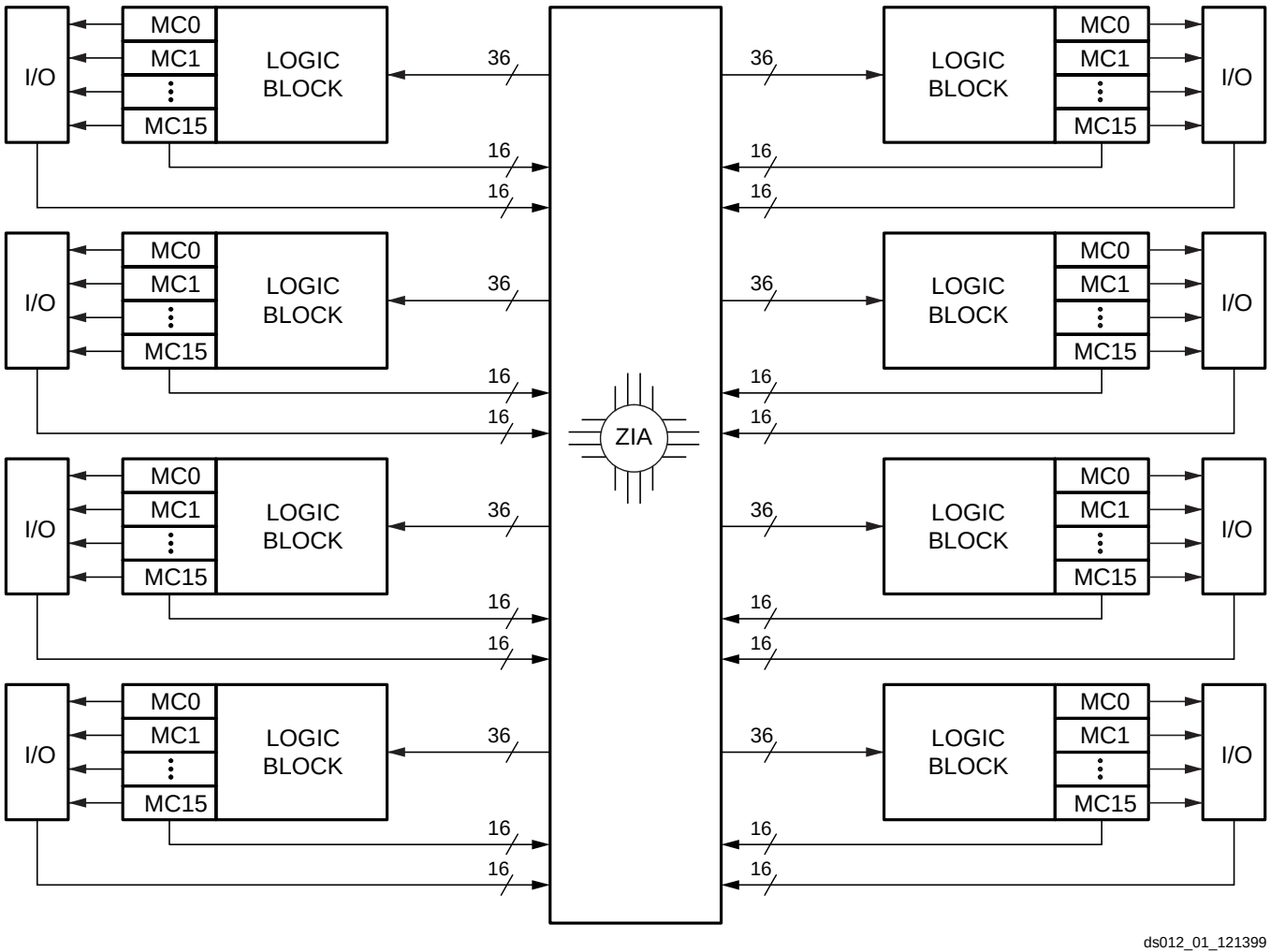


Figure 1: Xilinx XPLA3 CPLD Architecture

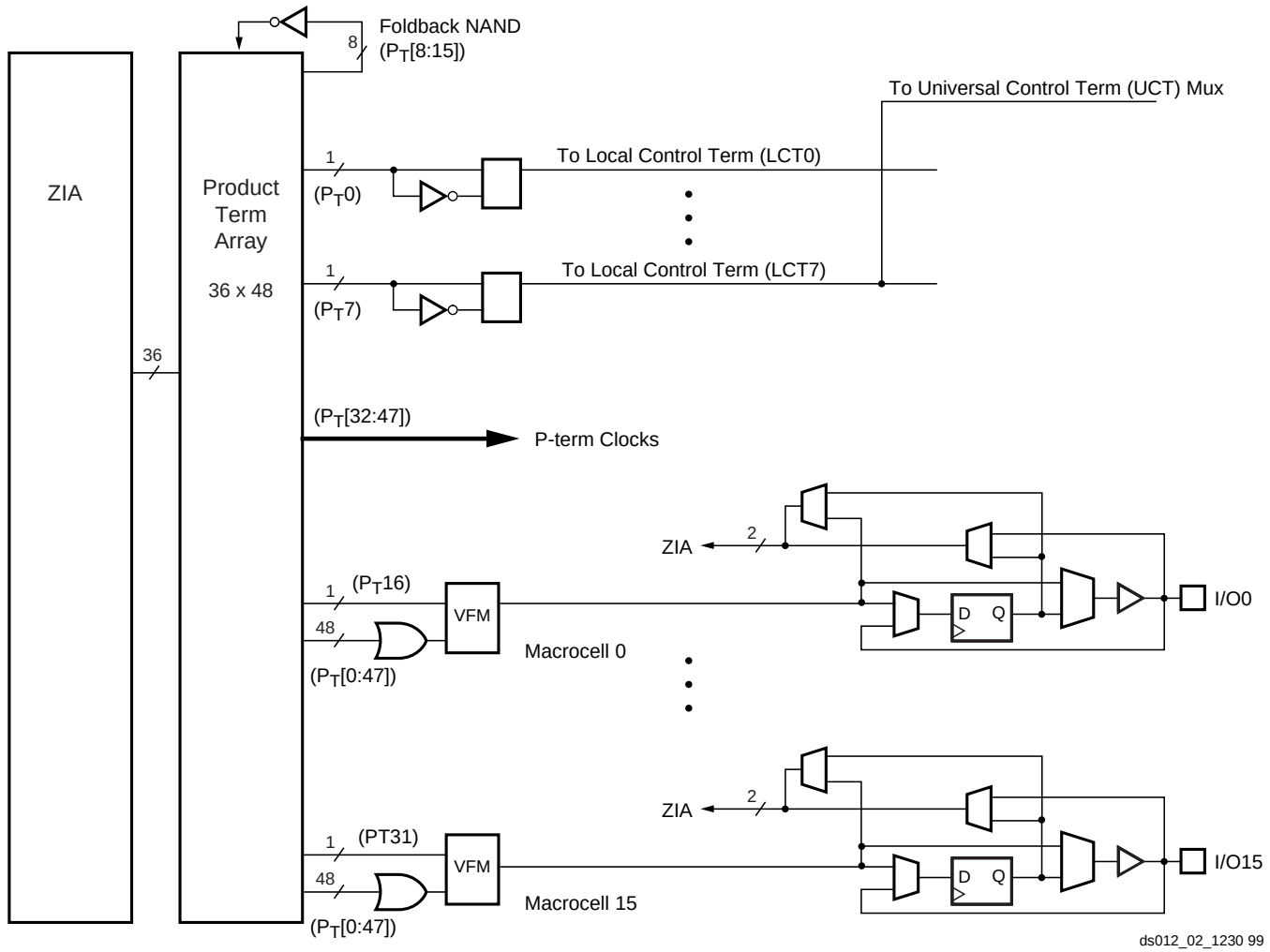


Figure 2: Xilinx XPLA3 Logic Block Architecture

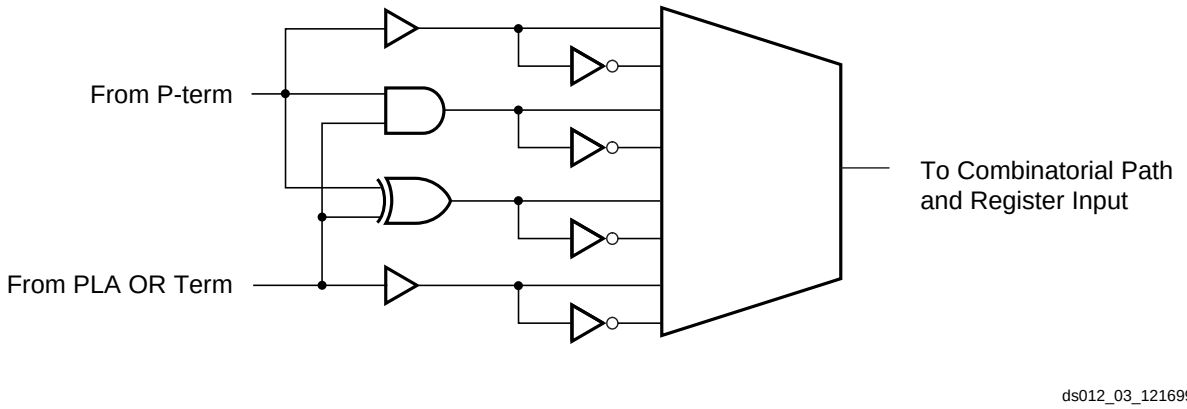


Figure 3: Variable Function Multiplexer

FoldBack NANDs

XPLA3 utilizes FoldBack NANDs to increase the effective product term width of a programmable logic device. These structures effectively provide an inverted product term to be used as a logic input by all of the local product terms. Refer to Figure 4 for an example of this technique. .

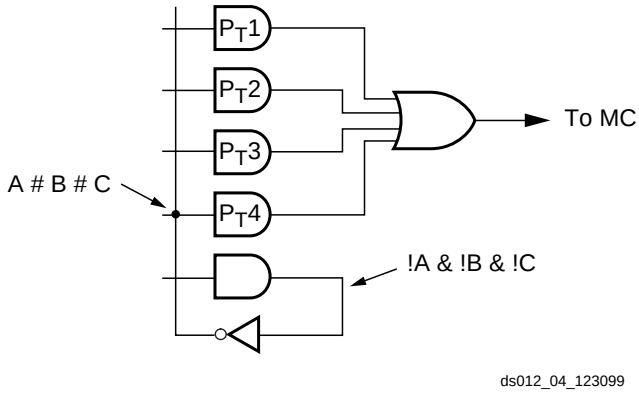


Figure 4: Basic FoldBack NAND Structure

As seen in Figure 4, the output signal is determined by the following equation:

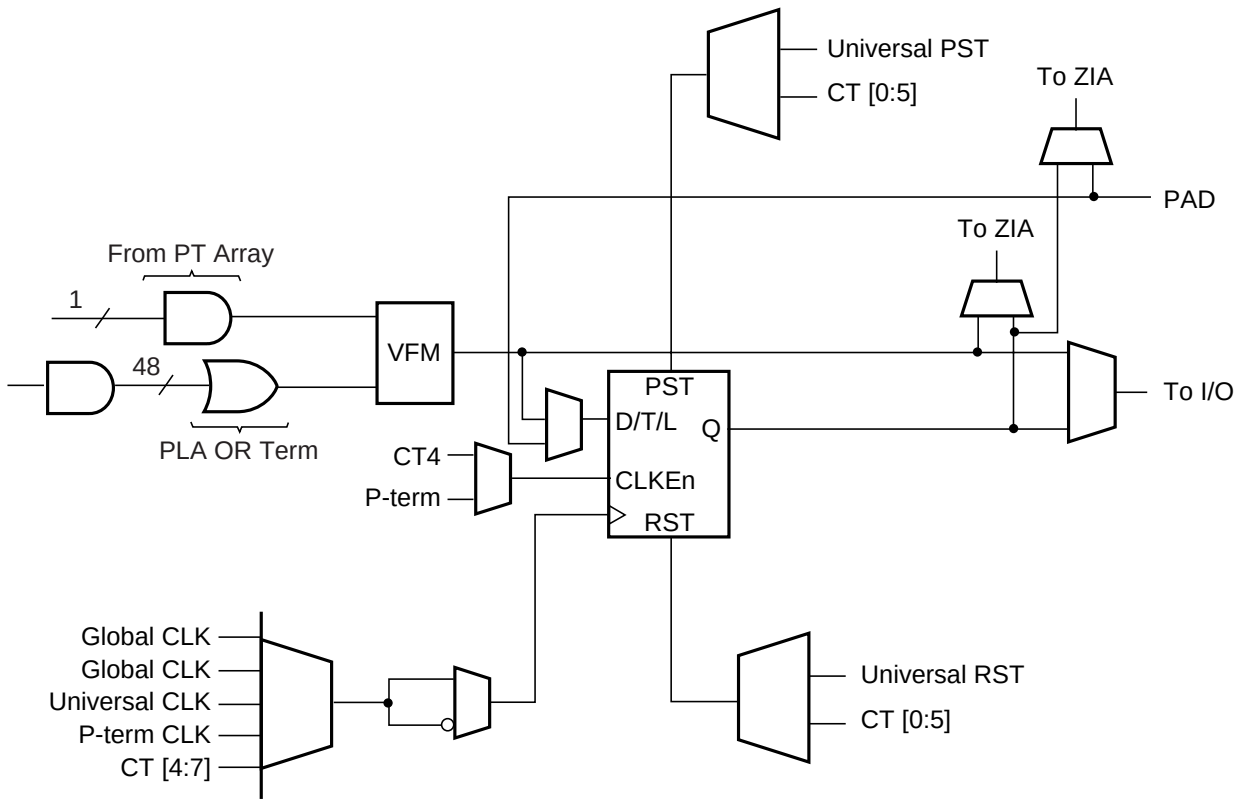
MC logic = PT1 # PT2 # PT3 # (PT4) &(A # B # C)

Macrocell Architecture

Figure 5 shows the architecture of the macrocell used in the CoolRunner XPLA3. Any macrocell can be reset or preset on power-up. Each macrocell register can be configured as a D-, T-, or Latch-type flip-flop, or combinatorial logic function. Each of these flip-flops can be clocked from any one of eight sources. There are two global synchronous clocks that are derived from the four external clock pins. There is one universal clock signal. The clock input signals CT[4:7] (Local Control Terms) can be individually configured as either a PRODUCT term or SUM term equation created from the 36 signals available inside the logic block..

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. When the I/O pin is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feed back the logic implemented in the macrocell. When an I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path. The logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path.

If the macrocell is configured as an input, there is a path to the register to provide a fast input setup time.



Note: Global CLK signals come from pins.

ds012_05_122299

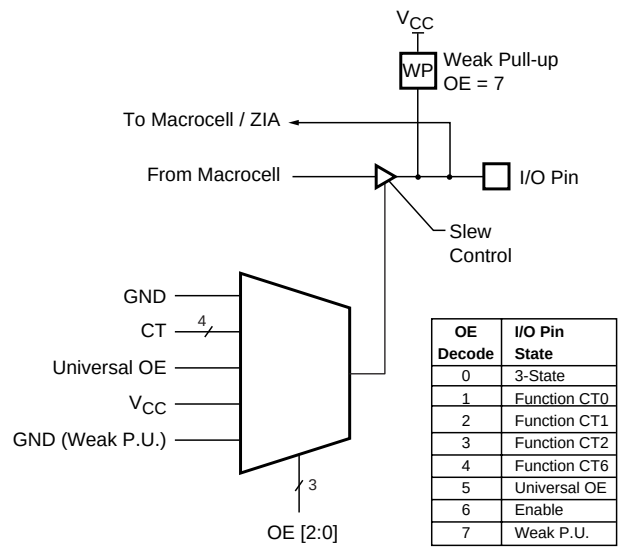
Figure 5: XPLA3 Macrocell Architecture

I/O Cell

The OE (Output Enable) multiplexer has eight possible modes (Figure 6), including a programmable weak pull-up (WPU) eliminating the need for external termination on unused I/Os.

The I/O Cell is 5V tolerant, and has a single-bit slew-rate control for reducing EMI generation.

Outputs are 3.3V PCI electrical specification compatible (no internal clamp diode).



OE Decode	I/O Pin State
0	3-State
1	Function CT0
2	Function CT1
3	Function CT2
4	Function CT6
5	Universal OE
6	Enable
7	Weak P.U.

ds012_06_121699

Figure 6: I/O Cell

Simple Timing Model

Figure 7 shows the XPLA3 timing model which has three main timing parameters, including T_{PD}, T_{SU}, and T_{CO}. In other architectures, the user may be able to fit the design into the CPLD, but may not be sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of other architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA3 architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

Slew Rate Control

XPLA3 devices have slew rate control for each macrocell output pin. The user has the option to enable the slew rate control to reduce EMI. The nominal delay for using this option is 2.0 ns.

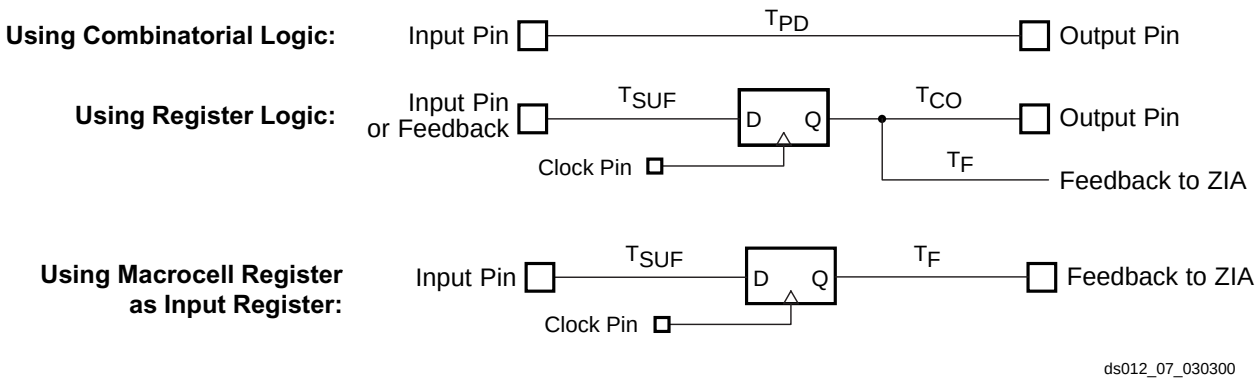


Figure 7: XPLA3 Timing Model

JTAG Testing Capability

JTAG is the commonly used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands that facilitate both board and device level testing without the use of specialized test equipment. XPLA3 devices use the JTAG Interface for In-System Programming/Reprogramming. The full JTAG command set is implemented (see Table 1), including the use of a port enable signal.

As implemented in XPLA3, the JTAG Port includes four of the five pins (refer to Table 2) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST (Test Reset). TRST is considered an optional signal, since it is not actually required to perform BST or ISP. The XPLA3 saves an I/O pin for general purpose use by not implementing the optional TRST signal in the JTAG interface. Instead, the XPLA3 supports the test reset functionality through the use of its power-up reset circuit, which is included in all CoolRunner CPLDs. It should be noted that the pins associated with the JTAG Port should connect to an external pull-up resistor (typical 10K) to keep the JTAG signals from floating when they are not being used.

The Port Enable pin is used to reclaim TMS, TDO, TDI, and TCK for JTAG ISP programming if the user has defined these pins as general purpose I/O during device programming. For ease of use, XPLA3 devices are shipped with the JTAG port pins enabled. Please note that the Port Enable pin must be low logic level during the power-up sequence for the device to operate properly.

During device programming, the JTAG ISP pins can be left as is or reconfigured as user specific I/O pins. If the JTAG ISP pins have been used for I/O pins, simply applying high logic level to the Port Enable pin converts the JTAG ISP pins back to their respective programming function and the device can be reprogrammed. After completing the desired JTAG ISP programming function, simply return Port Enable to Ground. This will re-establish the JTAG ISP pins to their respective I/O function. Note that reconfiguring the JTAG port pins as I/Os makes these pins non-JTAG ISP functional.

The XPLA3 family allows the macrocells associated with these pins to be used as buried logic when the JTAG/ISP function is enabled.

Table 1: XPLA3 Low-level JTAG Boundary-scan Commands

Instruction (Instruction Code) Register Used	Description
Sample/Preload (00010) Boundary-scan Register	The mandatory Sample/Preload instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded into the latched parallel outputs of the Boundary-scan Shift Register prior to selection of the other boundary-scan test instructions.
Extest (00000) Boundary-scan Register	The mandatory Extest instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-scan Shift Register using the Sample/Preload instruction prior to selection of the Extest instruction.
Bypass (11111) Bypass Register	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-scan cycle.
Idcode (00001) Boundary-scan Register	Selects the Idcode register and places it between TDI and TDO, allowing the Idcode to be serially shifted out of TDO. The Idcode instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
High-Z (00101) Bypass Register	The High-Z instruction places the component in a state which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The High-Z instruction also forces the Bypass Register between TDI and TDO
Intest (00011) Boundary-scan Register	The Intest instruction selects the boundary scan register preparatory to applying tests to the logic core of the device. This permits testing of on-chip system logic while the component is already on the board

Table 2: JTAG Pin Description

Pin	Name	Description
TCK	Test Clock Input	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is 3-stated if data is not being shifted out of the device.

3V, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-functional hardware
  - Reconfigurability for Test
  - Eliminates handling of "fine lead-pitch" components for programming
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, reconfiguration, and customization

XPLA3 allows for 3V, in-system programming/reprogramming of its EEPROM cells via a JTAG interface. An on-chip charge pump eliminates the need for externally provided super-voltages. This allows programming on the circuit board using only the 3V supply required by the device for normal operation. The ISP commands implemented in XPLA3 are specified in Table 3.

Table 3: Low -level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	01001	Enables the Erase, Program, and Verify commands. Using the Enable instruction before the Erase, Program, and Verify instructions allows the user to specify the outputs of the device using the JTAG Boundary-Scan Sample/Preload command.
Erase (ISP Shift Register)	01010	Erases the entire EEPROM array. User can define the outputs during this operation by using the JTAG Sample/Preload command.
Program (ISP Shift Register)	01011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs can be defined by using the JTAG Sample/Preload command.
Disable (ISP Shift Register)	10000	Disable instruction allows the user to leave ISP mode. It selects the ISP register to be directly connected between TDO and TDI.
Verify (ISP Shift Register)	01100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The user can define the outputs during this operation.

Terminations

The CoolRunner XPLA3 CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The XPLA3 CPLDs have programmable on-chip weak pull-up resistors on each I/O pin. These resistors are automatically activated by fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the weak pull-up resistors will be turned on. It is recommended that any unused I/O pins on the XPLA3 family of CPLDs be left unconnected. As with all CMOS devices, do not allow inputs to float.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLDs and other integrated circuits. The XPLA3 family supports the following methods:

- Xilinx HW 130
- PC Parallel Port
- Workstation or PC Serial Port
- Embedded Processor
- Automated Test Equipment
- Third Party Programmers
- Xilinx ISP Programming Tools

For more details on JTAG and ISP, refer to the related application note: *JTAG and ISP in Xilinx CPLDs*. see also Table 4 below:

Table 4: Programming Specifications

Symbol	Parameter	Min.	Max.	Unit
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	3.0 (com) 2.7 (ind)	3.6	V
I_{CCP}	I_{CC} limit program/verify		80	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{OL}	Output voltage (Low)		0.4	V
V_{OH}	Output voltage (High)	2.4		V
AC Parameters				
F_{MAX}	TCK maximum frequency		10	MHz
P_{WE}	Pulse width erase	100		ms
P_{WP}	Pulse width program	10		ms
P_{WV}	Pulse width verify	10		µs
T_{INIT}	Initialization time	50		µs
T_{MS_SU}	TMS setup time before TCK ↑	10		ns
T_{DI_SU}	TDI setup time before TCK ↑	10		ns
T_{MS_H}	TMS hold time after TCK ↑	20		ns
T_{DI_H}	TDI hold time after TCK ↑	20		ns
T_{DO_CO}	TDO valid after TCK ↓		30	ns

Absolute Maximum Ratings(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage(2) relative to GND	–0.5	3.6	V
V_I	Input voltage(3) relative to GND	–0.5	5.5	V
I_{OUT}	Output current	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to 7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
4. External I/O voltage may not be applied for more than 100 milliseconds without the presence of V_{CC}.

Recommended Operation Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage f	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	2.7	3.6	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CC}	V
T_R	Input rise time			20	ns
T_F	Input fall time			20	ns

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

Device Families

Parameter	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL
Macrocells	32	64	128	256	384
Usable gates	750	1,500	3,000	6,000	9,000
Registers	32	64	128	256	384
I/Os	32	64	104	160	216
T_{PD} (ns)	5.0	6.0	6.0	7.5	7.5
T_{SUF} (ns)	TBD	TBD	TBD	2.0	TBD
T_{CO} (ns)	4.0	4.0	4.5	4.5	5.0
FSYSTEM (MHz)	200	167	167	140	TBD
	Preliminary Information				

Available Packages

Package Type	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL
CS280				160 I/O	216 I/O
PQ208				160 I/O	
TQ144			104 I/O	116 I/O	
CS144			104 I/O		
VQ100		64 I/O	80 I/O		
CP56		44 I/O			
CS48	32 I/O	32 I/O(1)			
VQ44	32 I/O	32 I/O			
	Preliminary Information				

Note:
1. Future package.

Revision Table

Date	Version #	Revision
01/20/2000	1.0	Initial Xilinx release.
03/03/00	1.1	Minor update.