

Summary of Radiation Hardened QPro™ Virtex™-II Features

- Industry First Radiation Hardened Platform FPGA Solution
- Guaranteed total ionizing dose to 200K Rad(si)
- Latch-up immune to LET > 160 MeV-cm²/mg
- SEU in GEO upsets < 1.5E-6 per device day achievable with recommended redundancy implementation
- Certified to MIL-PRF-38535 (Qualified Manufacturer Listing)
- Guaranteed over the full military temperature range (-55° C to +125° C)
- Ceramic and Plastic Wire-Bond and Flip-Chip Grid Array Packages
- IP-Immersion Architecture
 - Densities from 1M to 6M system gates
 - 300+ MHz internal clock speed (Advance Data)
 - 622+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
 - 2.5 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
 - Up to 1 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
 - DRAM interfaces
 - SDR/DDR SDRAM
 - Network FCRAM
 - Reduced Latency DRAM
 - SRAM interfaces
 - SDR/DDR SRAM
 - QDR SRAM
 - CAM interfaces
- Arithmetic Functions
 - Dedicated 18-bit x 18-bit multiplier blocks
 - Fast look-ahead carry logic chains
- Flexible Logic Resources
 - Up to 67,584 internal registers/latches with Clock Enable
 - Up to 67,584 look-up tables (LUTs) or cascadable 16-bit shift registers
 - Wide multiplexers and wide-input function support
 - Horizontal cascade chain and sum-of-products support
 - Internal 3-state busing
- High-Performance Clock Management Circuitry
 - Up to 12 DCM (Digital Clock Manager) modules
 - Precise clock de-skew
 - Flexible frequency synthesis
 - High-resolution phase shifting
- 16 global clock multiplexer buffers
- Active Interconnect Technology
 - Fourth generation segmented routing structure
 - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
 - Up to 824 user I/Os
 - 19 single-ended and six differential standards
 - Programmable sink current (2 mA to 24 mA) per I/O
 - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
 - Differential Signaling
 - 622 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
 - Bus LVDS I/O
 - Lightning Data Transport (LDT) I/O with current driver buffers
 - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
 - Built-in DDR input and output registers
 - Proprietary high-performance SelectLink Technology
 - High-bandwidth data path
 - Double Data Rate (DDR) link
 - Web-based HDL generation methodology
- Supported by Xilinx Foundation Series™ and Alliance Series™ Development Systems
 - Integrated VHDL and Verilog design flows
 - Compilation of 10M system gates designs
 - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
 - Fast SelectMAP configuration
 - IEEE 1532 support
 - Partial reconfiguration
 - Unlimited reprogrammability
 - Readback capability
- 0.15 μm 8-Layer Metal Process with 0.12 μm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support

Table 1: Virtex-II Field-Programmable Gate Array Family Members

| Device | System Gates | CLB (1 CLB = 4 slices = Max 128 bits) | | | Multiplier Blocks | SelectRAM Blocks | | DCMs | Max I/O Pads ⁽¹⁾ |
|-----------|--------------|--|--------|-------------------------------|-------------------|------------------|-----------------|------|-----------------------------|
| | | Array Row x Col. | Slices | Maximum Distributed RAM Kbits | | 18 Kbit Blocks | Max RAM (Kbits) | | |
| XQR2V1000 | 1M | 40 x 32 | 5,120 | 160 | 40 | 40 | 720 | 8 | 432 |
| XQR2V3000 | 3M | 64 x 56 | 14,336 | 448 | 96 | 96 | 1,728 | 12 | 720 |
| XQR2V6000 | 6M | 96 x 88 | 33,792 | 1,056 | 144 | 144 | 2,592 | 12 | 1,104 |

Notes:

1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The QPro Virtex-II radiation hardened family includes platform FPGAs developed for high performance, high-density, aerospace designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 μm /0.12 μm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 6 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays and other one-time-programmable devices. As shown in Table 1, the QPro Virtex-II radiation hardened family comprises three members, ranging from 1M to 6M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 1.00 mm and 1.27 mm pitches. In addition to traditional

Radiation Assurance

The Virtex-II Radiation Hardened Platform FPGAs are guaranteed for Total Ionizing Dose (TID) life and Single Event Latch-Up immunity (SEL).

Total Ionizing Dose

Each Wafer Lot is sampled and tested per Method 1019.5 to assure that device performance meets or exceeds the guaranteed DC electrical specification requirements, as well as AC and Timing parameters at maximum guaranteed total dose levels.

Single Event Latch-Up

The Radiation hardened Virtex-II technology incorporates a thin epitaxial layer in the wafer manufacturing process for latch-up immunity assurance. The qualified mask set is ver-

wire-bond interconnects, flip-chip interconnect is used in some of the CGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 on page 5) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: Maximum Number of User I/O Pads

| Device | Wire-Bond | Flip-Chip |
|-----------|-----------|-----------|
| XQR2V1000 | 328 | - |
| XQR2V3000 | 516 | - |
| XQR2V6000 | - | 824 |

ified in a heavy ion environment under vacuum, and tested with an LET that exceeds Space environment phenomenon, to a fluence that exceeds 1E7 particles/cm².

Single Event Upset

Additional experiments are conducted in heavy ion, proton, and neutron environments in order to measure and document the susceptibility and consequence of SEU(s). An industry consortium oversees and validates the test methods, empirical data collected, and resulting analysis. Conclusions are published on the website as well as International Conferences. The Single Event Effects Consortium Reports can be found at http://www.xilinx.com/products/hirel_qml.htm

Radiation Specifications⁽¹⁾

Table 3: Minimum Radiation Tolerances

| Symbol | Description | Min | Max | Units |
|--------|--|-----|--------|---------------------------|
| TID | Total Ionizing Dose Method 1019.5, Dose Rate ~50.0 rad(Si)/sec | 200 | - | krad(Si) |
| SEL | Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET) | 160 | - | (MeV-cm ² /mg) |
| SEFI | Single Event Functional Interrupt GEO 36,000km Typical Day | | 1.5E-6 | Upsets/Device/ Day |

Notes:

- For more information, refer to "Single Event Effects Consortium Report, Static SEU Response for the Rad Hard Virtex-II" at http://www.xilinx.com/products/hirel_qml.htm.

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

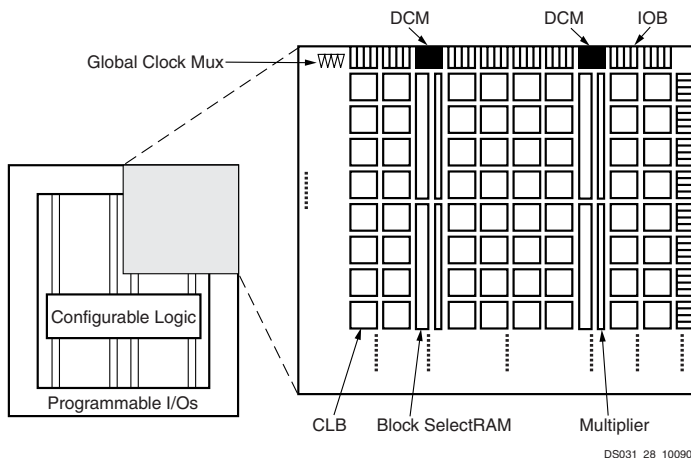


Figure 1: Virtex-II Architecture Overview

The internal configurable logic includes four major elements organized in a regular array:

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these

elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI compatible (33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP
- HSTL (Class I, II, III, and IV)
- SSTL (3.3V and 2.5V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F and G)
- Two storage elements

- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F and G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of dual-port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascaded to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in [Table 4](#).

Table 4: Dual-Port And Single-Port Configurations

| | |
|-------------|---------------|
| 16K x 1 bit | 2K x 9 bits |
| 8K x 2 bits | 1K x 18 bits |
| 4K x 4 bits | 512 x 36 bits |

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where M and D are two integers. For the exact

timing parameters, see **QPro Virtex-II Switching Characteristics**, page 51.

Virtex-II devices have 16 global clock MUX buffers with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout, and the interconnect layout is designed to minimize crosstalk.

Virtex-II Device/Package Combinations and Maximum I/O

Wire-bond and flip-chip packages are available. **Table 5** shows the maximum possible number of user I/Os in wire-bond and flip-chip packages. **Table 6** shows the number of available user I/Os for all device/package combinations.

- FG denotes wire-bond fine-pitch Plastic BGA (1.00 mm pitch).
- BG denotes wire-bond standard Plastic BGA (1.27 mm pitch).

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

Boundary Scan

Boundary-scan instructions and associated data registers support a standard methodology for accessing and configuring Virtex-II devices that complies with IEEE standards 1149.1 — 1993 and 1532. A system mode and a test mode are implemented. In system mode, a Virtex-II device performs its intended mission even while executing non-test boundary-scan instructions. In test mode, boundary-scan test instructions control the I/O pins for testing purposes. The Virtex-II Test Access Port (TAP) supports BYPASS, PRELOAD, SAMPLE, IDCODE, and USERCODE non-test instructions. The EXTTEST, INTEST, and HIGHZ test instructions are also supported.

- CG denotes wire-bond fine-pitch Hermetic Ceramic Column Grid Array (1.27 mm pitch).
- CF denotes flip-chip fine-pitch non-Hermetic Ceramic Column Grid Array (1.00 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, and RSVD) and VBATT.

Table 5: Package Information

| Package | FG456 | BG575 | BG728 & CG717 | CF1144 |
|------------|---------|---------|---------------|---------|
| Pitch (mm) | 1.00 | 1.27 | 1.27 | 1.00 |
| Size (mm) | 23 x 23 | 31 x 31 | 35 x 35 | 35 x 35 |

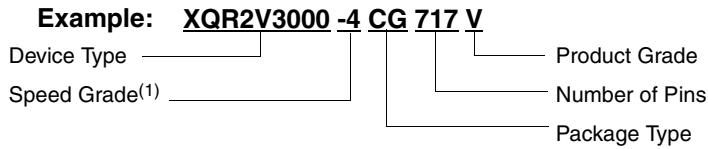
Table 6: Virtex-II Device/Package Combinations and Maximum Number of Available I/Os

| Package | Available I/Os | | |
|---------|----------------|-----------|-----------|
| | XQR2V1000 | XQR2V3000 | XQR2V6000 |
| FG456 | 324 | - | - |
| BG575 | 328 | - | - |
| BG728 | - | 516 | - |
| CG717 | - | 516 | - |
| CF1144 | - | - | 824 |

Notes:

1. The BG728 and CG717 packages are pinout (footprint) compatible.
2. The CF1144 is pinout (footprint) compatible with the FF1152.

Virtex-II Ordering Information



Device Ordering Options

| Device Type | Package | | Product Grade | Manufacturing Flow ⁽²⁾ | Temperature Range |
|-------------|---------|--|---------------|-----------------------------------|--|
| XQR2V1000 | FG456 | 456-ball Plastic Fine Pitch BGA Package | M | M-Grade | Military Ceramic T _C = -55° C to +125° C |
| XQR2V3000 | BG575 | 575-ball Plastic BGA Package | V | QPRO-PLUS | |
| XQR2V6000 | BG728 | 728-ball Plastic BGA Package | H | QPRO-FCC | |
| | CG717 | 717-column Hermetic Ceramic CGA Package | N | Class N | Military Plastic T _J = -55° C to +125° C |
| | CF1144 | 1144-column Non-hermetic Ceramic Flip-Chip Package | R | QPRO+PLUS PEM | |

Notes:

- 4 is the only supported speed grade.
- A detailed explanation of the Manufacturing and Test Flows is available at <http://www.xilinx.com/products/milaero/rpt003.pdf>

Valid Ordering Combinations

| Grade | XQR2V1000 | XQR2V3000 | XQR2V6000 |
|-------|-------------------|-------------------|---------------------------------|
| N | XQR2V1000-4FG456N | XQR2V3000-4BG728N | |
| | XQR2V1000-4BG575N | | |
| R | XQR2V1000-4FG456R | XQR2V3000-4BG728R | |
| | XQR2V1000-4BG575R | | |
| M | | XQR2V3000-4CG717M | XQR2V6000-4CF1144M ¹ |
| V | | XQR2V3000-4CG717V | |
| H | | | XQR2V6000-4CF1144H ¹ |

Notes:

- CF1144 is non-Hermetic Ceramic.

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as an input and/or an output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in [Figure 2](#).

IOB blocks are designed for high-performance I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.

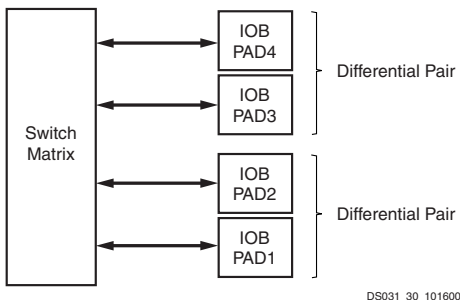


Figure 2: Virtex-II Input/Output Tile

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage ($V_{CCINT} = 1.5V$), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see [Table 7](#)). An auxiliary supply voltage ($V_{CCAUX} = 3.3 V$) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see [DC Input and Output Levels](#).

Table 7: Supported Single-Ended I/O Standards

| I/O Standard | Output V_{CCO} | Input V_{CCO} | Input V_{REF} | Board Termination Voltage (V_{TT}) |
|--------------|------------------|-----------------|-----------------|--|
| LVTTTL | 3.3 | 3.3 | N/A | N/A |
| LVC MOS33 | 3.3 | 3.3 | N/A | N/A |
| LVC MOS25 | 2.5 | 2.5 | N/A | N/A |
| LVC MOS18 | 1.8 | 1.8 | N/A | N/A |
| LVC MOS15 | 1.5 | 1.5 | N/A | N/A |
| PCI33_3 | 3.3 | 3.3 | N/A | N/A |
| PCI66_3 | 3.3 | 3.3 | N/A | N/A |
| PCI-X | 3.3 | 3.3 | N/A | N/A |
| GTL | Note 1 | Note 1 | 0.8 | 1.2 |
| GTL P | Note 1 | Note 1 | 1.0 | 1.5 |
| HSTL_I | 1.5 | N/A | 0.75 | 0.75 |
| HSTL_II | 1.5 | N/A | 0.75 | 0.75 |
| HSTL_III | 1.5 | N/A | 0.9 | 1.5 |
| HSTL_IV | 1.5 | N/A | 0.9 | 1.5 |
| HSTL_I | 1.8 | N/A | 0.9 | 0.9 |
| HSTL_II | 1.8 | N/A | 0.9 | 0.9 |
| HSTL_III | 1.8 | N/A | 1.1 | 1.8 |
| HSTL_IV | 1.8 | N/A | 1.1 | 1.8 |
| SSTL2_I | 2.5 | N/A | 1.25 | 1.25 |
| SSTL2_II | 2.5 | N/A | 1.25 | 1.25 |
| SSTL3_I | 3.3 | N/A | 1.5 | 1.5 |
| SSTL3_II | 3.3 | N/A | 1.5 | 1.5 |
| AGP-2X/AGP | 3.3 | N/A | 1.32 | N/A |

Notes:

1. V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad.

Table 8: Supported Differential Signal I/O Standards

| I/O Standard | Output V _{CCO} | Input V _{CCO} | Input V _{REF} | Output V _{OD} |
|--------------|-------------------------|------------------------|------------------------|------------------------|
| LVPECL_33 | 3.3 | N/A | N/A | 490 mV to 1.22V |
| LDT_25 | 2.5 | N/A | N/A | 0.430 - 0.670 |
| LVDS_33 | 3.3 | N/A | N/A | 0.250 - 0.400 |
| LVDS_25 | 2.5 | N/A | N/A | 0.250 - 0.400 |
| LVDS_EXT_33 | 3.3 | N/A | N/A | 0.330 - 0.700 |
| LVDS_EXT_25 | 2.5 | N/A | N/A | 0.330 - 0.700 |
| BLVDS_25 | 2.5 | N/A | N/A | 0.250 - 0.450 |
| ULVDS_25 | 2.5 | N/A | N/A | 0.430 - 0.670 |

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the “5V Tolerant I/Os” Tech Topic at <http://www.xilinx.com>.

Table 9 lists supported I/O standards with Digitally Controlled Impedance. See **Digitally Controlled Impedance (DCI)**, page 13.

Table 9: Supported DCI I/O Standards

| I/O Standard | Output V _{CCO} | Input V _{CCO} | Input V _{REF} | Termination Type |
|-----------------------------|-------------------------|------------------------|------------------------|------------------|
| LVDCI_33 ⁽¹⁾ | 3.3 | 3.3 | N/A | Series |
| LVDCI_DV2_33 ⁽¹⁾ | 3.3 | 3.3 | N/A | Series |
| LVDCI_25 ⁽¹⁾ | 2.5 | 2.5 | N/A | Series |
| LVDCI_DV2_25 ⁽¹⁾ | 2.5 | 2.5 | N/A | Series |
| LVDCI_18 ⁽¹⁾ | 1.8 | 1.8 | N/A | Series |
| LVDCI_DV2_18 ⁽¹⁾ | 1.8 | 1.8 | N/A | Series |
| LVDCI_15 ⁽¹⁾ | 1.5 | 1.5 | N/A | Series |
| LVDCI_DV2_15 ⁽¹⁾ | 1.5 | 1.5 | N/A | Series |
| GTL_DC1 | 1.2 | 1.2 | 0.8 | Single |
| GTL_P_DC1 | 1.5 | 1.5 | 1.0 | Single |
| HSTL_I_DC1 | 1.5 | 1.5 | 0.75 | Split |
| HSTL_II_DC1 | 1.5 | 1.5 | 0.75 | Split |
| HSTL_III_DC1 | 1.5 | 1.5 | 0.9 | Single |
| HSTL_IV_DC1 | 1.5 | 1.5 | 0.9 | Single |
| HSTL_I_DC1 | 1.8 | N/A | 0.9 | Split |
| HSTL_II_DC1 | 1.8 | N/A | 0.9 | Split |
| HSTL_III_DC1 | 1.8 | N/A | 1.1 | Single |
| HSTL_IV_DC1 | 1.8 | N/A | 1.1 | Single |
| SSTL2_I_DC1 ⁽²⁾ | 2.5 | 2.5 | 1.25 | Split |
| SSTL2_II_DC1 ⁽²⁾ | 2.5 | 2.5 | 1.25 | Split |
| SSTL3_I_DC1 ⁽²⁾ | 3.3 | 3.3 | 1.5 | Split |
| SSTL3_II_DC1 ⁽²⁾ | 3.3 | 3.3 | 1.5 | Split |

Notes:

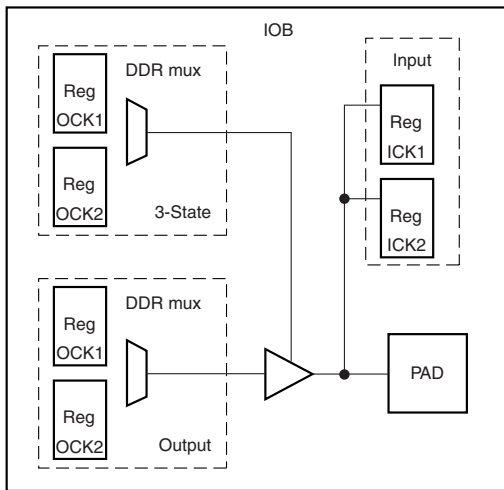
1. LVDCI_XX and LVDCI_DV2_XX are LVCMOS controlled impedance buffers, matching the reference resistors or half of the reference resistors.
2. These are SSTL compatible.

Logic Resources

IOB blocks include six storage elements, as shown in Figure 3.

Each storage element can be configured either as an edge-triggered D-type flip-flop or as a level-sensitive latch. On the input, output, and 3-state path, one or two DDR registers can be used.

Double data rate is directly accomplished by the two registers on each path, clocked by the rising edges (or falling



DS031_29_100900

Figure 3: Virtex-II IOB Block

edges) from two different clock nets. The two clock signals are generated by the DCM and must be 180 degrees out of

phase, as shown in Figure 4. There are two input, output, and 3-state data signals, each being alternately clocked out.

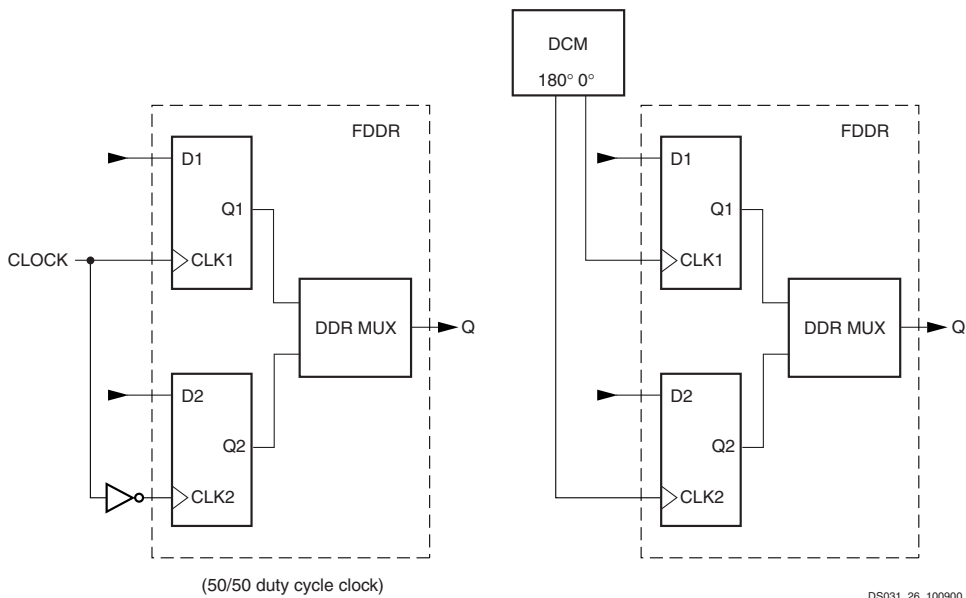


Figure 4: Double Data Rate Registers

The DDR mechanism shown in Figure 4 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLow attribute. SRHIGH forces a logic "1". SRLow forces a logic "0". When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default,

the SRLow attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLow, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set/reset is consistent in an IOB block.

All the control signals have independent polarities. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 5) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

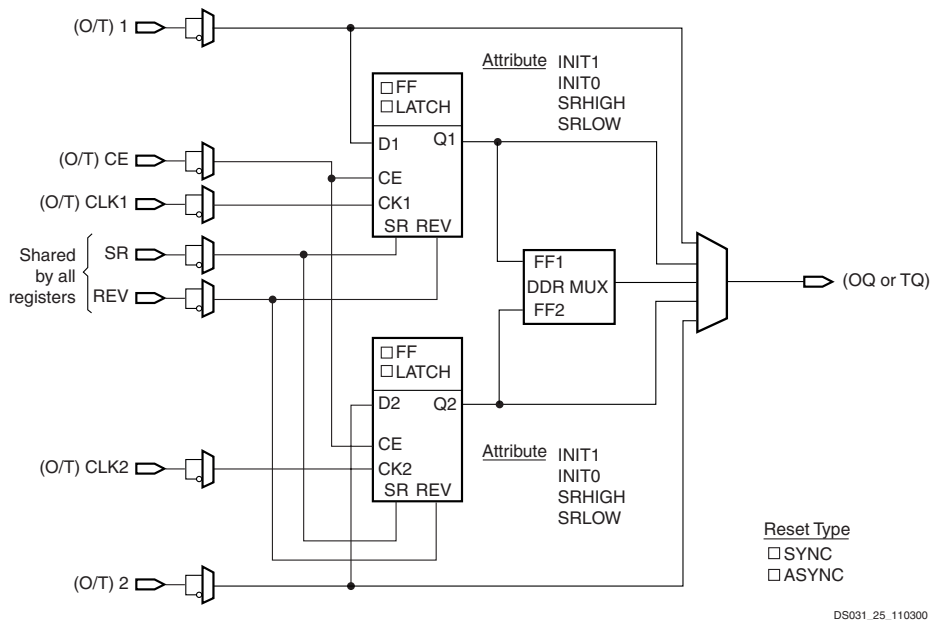


Figure 5: Register/Latch Configuration in an IOB Block

Input/Output Individual Options

Each device pad has optional pull-up and pull-down resistors in all SelectI/O-Ultra configurations. Each device pad has an optional weak-keeper in LVTTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 6.

Values of the optional pull-up and pull-down resistors are in the range 10 - 60 K Ω , which is the specification for V_{CCO} when operating at 3.3V (from 3.0V to 3.6V only). The clamp diode is always present, even when power is not.

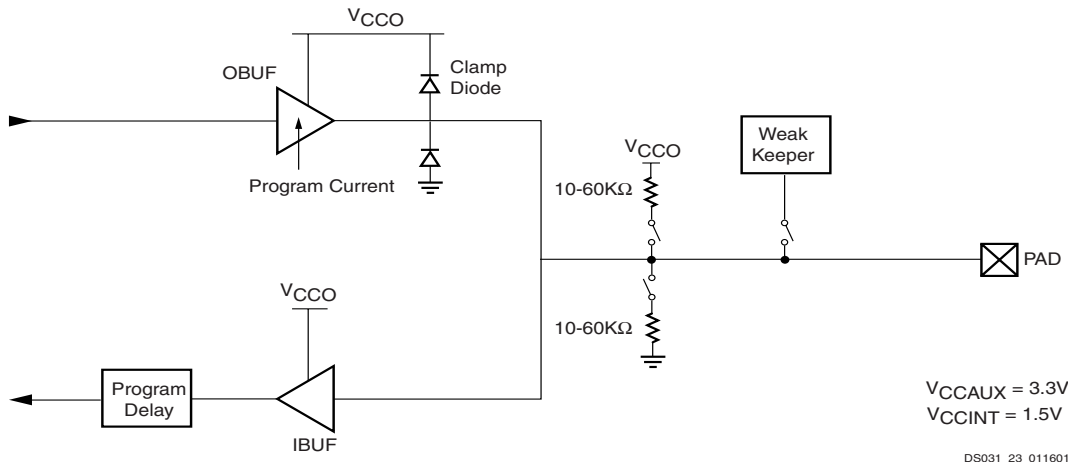


Figure 6: LVTTTL, LVCMOS, or PCI SelectI/O-Ultra Standards

The optional weak-keeper circuit is connected to each output. When selected, this circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. Pull-up or pull-down resistors override the weak-keeper circuit.

LVTTTL sinks and sources current up to 24 mA. The current is programmable for LVTTTL and LVCMOS SelectI/O-Ultra standards (see Table 10). Drive-strength and slew-rate controls for each output driver minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Table 10: LVTTTL and LVCMOS Programmable Currents (Sink and Source)

| SelectI/O-Ultra | Programmable Current (Worst-Case Guaranteed Minimum) | | | | | | |
|-----------------|--|------|------|------|-------|-------|-------|
| LVTTTL | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS33 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS25 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | 24 mA |
| LVCMOS18 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | n/a |
| LVCMOS15 | 2 mA | 4 mA | 6 mA | 8 mA | 12 mA | 16 mA | n/a |

Figure 7 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

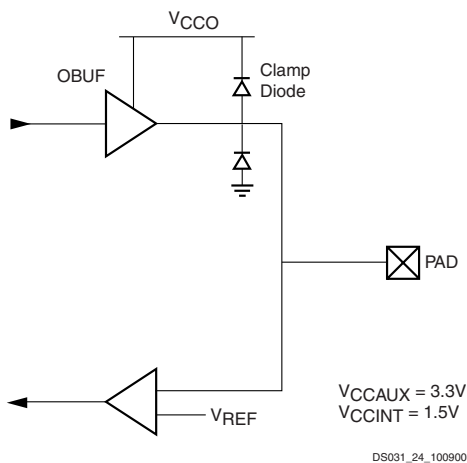


Figure 7: SSTL or HSTL SelectI/O-Ultra Standards

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II devices use two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is driven High, which disables the pull-up resistors on user I/O

pins. When HSWAP_EN is driven Low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible boundary-scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and/or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, ensures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, VREF. The need to supply VREF imposes constraints on which standards can be used in the same bank. See I/O Banking description below.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and/or the 3-state signal can be routed to the buffer directly from the internal logic or through an output/3-state flip-flop or latch, or through the DDR output/3-state registers.

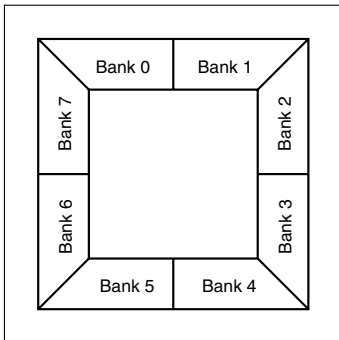
Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied VCCO voltage. The need to supply VCCO imposes constraints on which standards can be used in the same bank. See I/O Banking description below.

I/O Banking

Some of the I/O standards described above require VCCO and VREF voltages. These voltages are externally supplied

and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

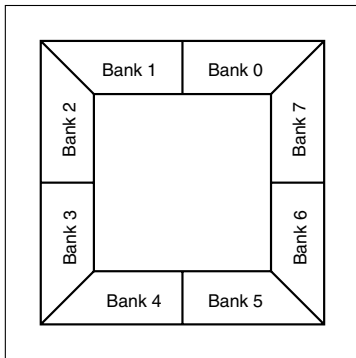
Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 8 and Figure 9. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.



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Figure 8: Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS, FG, & BG)

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user-I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.



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Figure 9: Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)

V_{REF} pins within a bank are interconnected internally, and consequently only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of

V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and are not used for I/O. In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bidirectional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.

Compatible example:

SSTL2_I and LVDS_25_DCI outputs

Incompatible example:

SSTL2_I (output $V_{CCO} = 2.5V$) and LVCOS33 (output $V_{CCO} = 3.3V$) outputs

2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.

Compatible example:

LVCOS15 and HSTL_IV inputs

Incompatible example:

LVCOS15 (input $V_{CCO} = 1.5V$) and LVCOS18 (input $V_{CCO} = 1.8V$) inputs

Incompatible example:

HSTL_I_DCI_18 ($V_{REF} = 0.9V$) and HSTL_IV_DCI_18 ($V_{REF} = 1.1V$) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.

Compatible example:

LVDS_25 output and HSTL_I input

Incompatible example:

LVDS_25 output (output $V_{CCO} = 2.5V$) and HSTL_I_DCI_18 input (input $V_{CCO} = 1.8V$)

4. **Combining bidirectional standards with input or output standards.** When combining bidirectional I/O with other standards, make sure the bidirectional standard can meet rules 1 through 3 above.

5. **Additional rules for combining DCI I/O standards.**

- a. No more than one Single Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_IV_DCI input and HSTL_III_DCI input

- b. No more than one Split Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_I_DCI input and HSTL_II_DCI input

Table 11 summarizes all standards and voltage supplies.

Table 11: Summary of Voltage Supply Requirements for All Input and Output Standards

| I/O Standard | V _{CCO} | | V _{REF} | | | Termination Type | | | | |
|--------------|------------------|-------|--------------------|--------|--------|------------------|-------|-------|--|--|
| | Output | Input | Input | Output | Input | Output | Input | Input | | |
| LVDS_33 | 3.3 | N/R | N/R ⁽¹⁾ | N/R | N/R | | | | | |
| LVDS_33 | | | N/R | N/R | N/R | | | | | |
| LVPECL_33 | | | N/R | N/R | N/R | | | | | |
| SSTL3_I | | | 1.5 | N/R | N/R | | | | | |
| SSTL3_II | | | 1.5 | N/R | N/R | | | | | |
| AGP | | | 1.32 | N/R | N/R | | | | | |
| LVTTTL | | 3.3 | N/R | N/R | N/R | N/R | | | | |
| LVCOS33 | | | | N/R | N/R | N/R | | | | |
| LVDCI_33 | | | | N/R | Series | N/R | | | | |
| LVDCI_DV2_33 | | | | N/R | Series | N/R | | | | |
| PCI33_3 | | | 3.3 | N/R | N/R | N/R | N/R | | | |
| PCI66_3 | | | | | N/R | N/R | N/R | | | |
| PCIX | | | | | N/R | N/R | N/R | | | |
| LVDS_33_DCI | | | | | N/R | N/R | Split | | | |
| LVDS_33_DCI | | | | | N/R | N/R | Split | | | |
| SSTL3_I_DCI | | | | | 1.5 | N/R | Split | | | |
| SSTL3_II_DCI | 1.5 | Split | Split | | | | | | | |
| LVDS_25 | 2.5 | N/R | N/R | N/R | N/R | | | | | |
| LVDS_25 | | | N/R | N/R | N/R | | | | | |
| LDT_25 | | | N/R | N/R | N/R | | | | | |
| ULVDS_25 | | | N/R | N/R | N/R | | | | | |
| BLVDS_25 | | | N/R | N/R | N/R | | | | | |
| SSTL2_I | | | 1.25 | N/R | N/R | | | | | |
| SSTL2_II | | 1.25 | N/R | N/R | | | | | | |
| LVCOS25 | | 2.5 | N/R | N/R | N/R | N/R | | | | |
| LVDCI_25 | | | | N/R | Series | N/R | | | | |
| LVDCI_DV2_25 | | | | N/R | Series | N/R | | | | |
| LVDS_25_DCI | | | | N/R | N/R | Split | | | | |
| LVDS_25_DCI | | | 2.5 | N/R | N/R | N/R | Split | | | |
| SSTL2_I_DCI | | | | | 1.25 | N/R | Split | | | |
| SSTL2_II_DCI | | | | | 1.25 | Split | Split | | | |

The implementation tools will enforce these design rules.

Table 11: Summary of Voltage Supply Requirements for All Input and Output Standards (Continued)

| I/O Standard | V _{CCO} | | V _{REF} | | | Termination Type | | | | |
|-----------------|------------------|-------|------------------|--------|--------|------------------|--------|-------|--|--|
| | Output | Input | Input | Output | Input | Output | Input | Input | | |
| HSTL_III_18 | 1.8 | N/R | 1.1 | N/R | N/R | | | | | |
| HSTL_IV_18 | | | 1.1 | N/R | N/R | | | | | |
| HSTL_I_18 | | | 0.9 | N/R | N/R | | | | | |
| HSTL_II_18 | | | 0.9 | N/R | N/R | | | | | |
| SSTL18_I | | | 0.9 | N/R | N/R | | | | | |
| SSTL18_II | | | 0.9 | N/R | N/R | | | | | |
| LVCOS18 | | 1.8 | N/R | N/R | N/R | N/R | | | | |
| LVDCI_18 | | | | N/R | Series | N/R | | | | |
| LVDCI_DV2_18 | | | | N/R | Series | N/R | | | | |
| HSTL_III_DCI_18 | | | | 1.1 | N/R | Single | | | | |
| HSTL_IV_DCI_18 | | | 1.1 | Single | Single | | | | | |
| HSTL_I_DCI_18 | | | 0.9 | N/R | Split | | | | | |
| HSTL_II_DCI_18 | | | 0.9 | Split | Split | | | | | |
| SSTL18_I_DCI | | | 0.9 | N/R | Split | | | | | |
| SSTL18_II_DCI | | | 0.9 | Split | Split | | | | | |
| HSTL_III | | | 1.5 | N/R | 0.9 | N/R | N/R | | | |
| HSTL_IV | 0.9 | N/R | | | N/R | | | | | |
| HSTL_I | 0.75 | N/R | | | N/R | | | | | |
| HSTL_II | 0.75 | N/R | | | N/R | | | | | |
| LVCOS15 | 1.5 | N/R | | N/R | N/R | N/R | | | | |
| LVDCI_15 | | | | N/R | Series | N/R | | | | |
| LVDCI_DV2_15 | | | | N/R | Series | N/R | | | | |
| GTLP_DCI | | | | 1 | Single | Single | | | | |
| HSTL_III_DCI | | 0.9 | | N/R | Single | | | | | |
| HSTL_IV_DCI | | 0.9 | | Single | Single | | | | | |
| HSTL_I_DCI | | 0.75 | | N/R | Split | | | | | |
| HSTL_II_DCI | | 0.75 | | Split | Split | | | | | |
| GTLP_DCI | | 1.2 | | 1.2 | 0.8 | Single | Single | | | |
| GTLP | | N/R | | N/R | 1 | N/R | N/R | | | |
| GTL | 0.8 | | | | N/R | N/R | | | | |

Notes:

- 1. N/R = no requirement.

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity.

High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, the voltage reference of the N transistor (VRN), and the voltage reference of the P transistor (VRP) are shown in Figure 10.

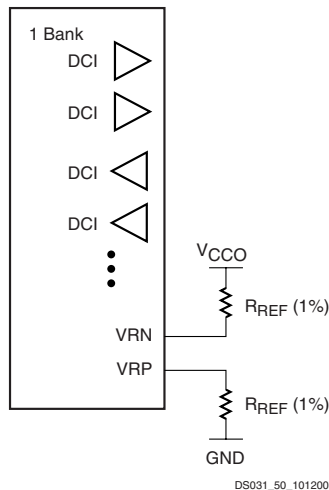


Figure 10: DCI in a Virtex-II Bank

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50 Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25 Ω to 100 Ω). For all series and parallel terminations listed in Table 12 and Table 13, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Termination)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

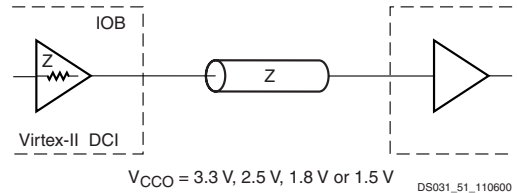


Figure 11: Internal Series Termination

Table 12: SelectI/O-Ultra Controlled Impedance Buffers

| V _{CCO} | DCI | DCI Half Impedance |
|------------------|----------|--------------------|
| 3.3 V | LVDCI_33 | LVDCI_DV2_33 |
| 2.5 V | LVDCI_25 | LVDCI_DV2_25 |
| 1.8 V | LVDCI_18 | LVDCI_DV2_18 |
| 1.5 V | LVDCI_15 | LVDCI_DV2_15 |

Controlled Impedance Drivers (Parallel Termination)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 13 lists the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 9. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 13: SelectI/O-Ultra Buffers with On-Chip Parallel Termination

| I/O Standard | External Termination | On-Chip Termination |
|----------------|----------------------|-----------------------------|
| SSTL3 Class I | SSTL3_I | SSTL3_I_DCI ⁽¹⁾ |
| SSTL3 Class II | SSTL3_II | SSTL3_II_DCI ⁽¹⁾ |
| SSTL2 Class I | SSTL2_I | SSTL2_I_DCI ⁽¹⁾ |
| SSTL2 Class II | SSTL2_II | SSTL2_II_DCI ⁽¹⁾ |
| HSTL Class I | HSTL_I | HSTL_I_DCI |
| HSTL Class II | HSTL_II | HSTL_II_DCI |
| HSTL Class III | HSTL_III | HSTL_III_DCI |
| HSTL Class IV | HSTL_IV | HSTL_IV_DCI |

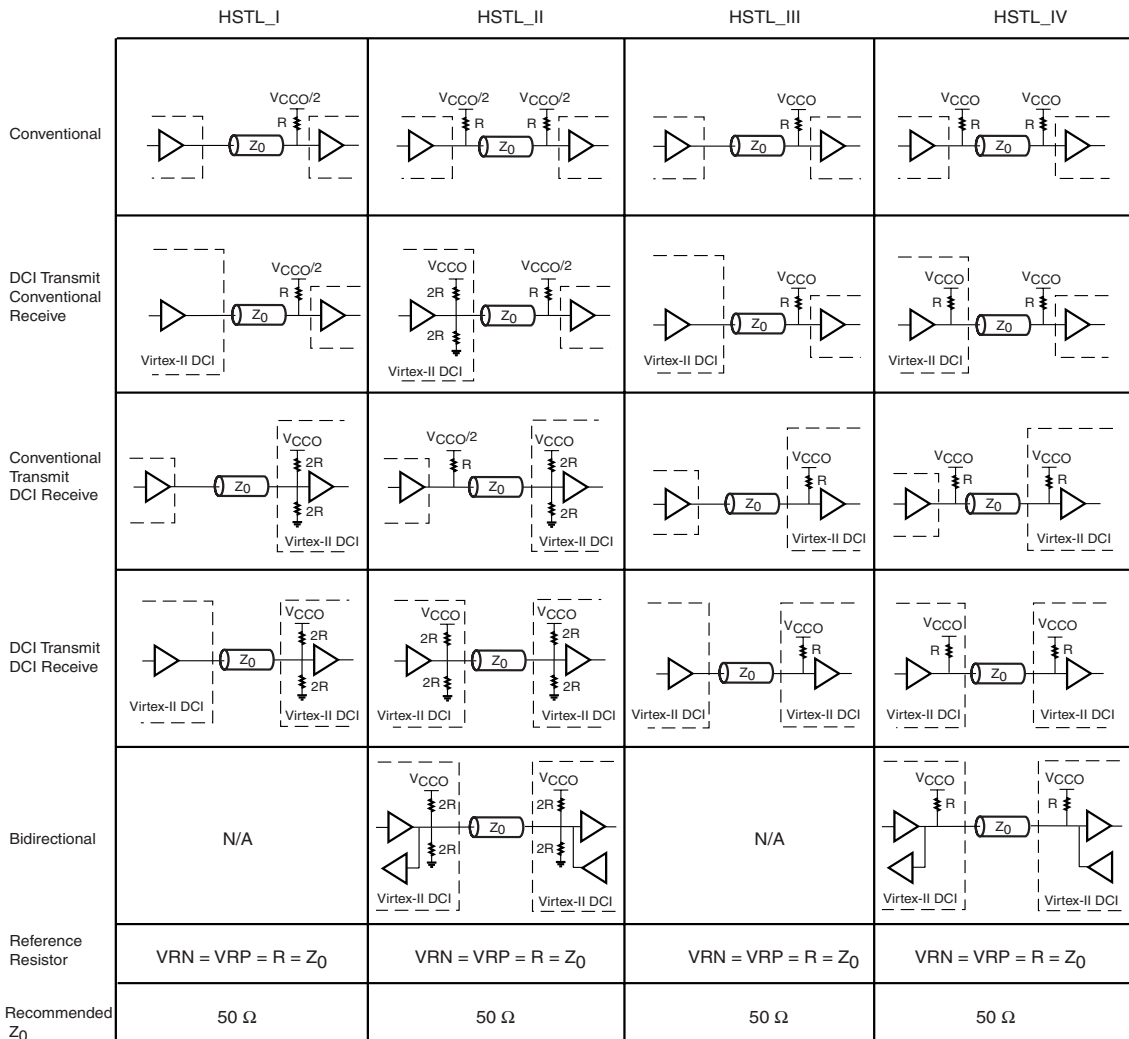
Table 13: Select I/O-Ultra Buffers with On-Chip Parallel Termination (Continued)

| I/O Standard | External Termination | On-Chip Termination |
|--------------|----------------------|---------------------|
| GTL | GTL | GTL_DCI |
| GTLP | GTLP | GTLP_DCI |

Notes:

- SSTL Compatible

Figure 12 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the Virtex-II User Guide (UG002).



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Figure 12: HSTL DCI Usage Examples

Figure 13 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL3_I_DCI, and SSTL3_II_DCI I/O standards. For a complete list, see the *Virtex-II User Guide* (UG002).

| | SSTL2_I | SSTL2_II | SSTL3_I | SSTL3_II |
|--------------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| Conventional | | | | |
| DCI Transmit Conventional Receive | | | | |
| Conventional Transmit DCI Receive | | | | |
| DCI Transmit DCI Receive | | | | |
| Bidirectional | N/A | | N/A | |
| Reference Resistor | $VRN = VRP = R = Z_0$ | $VRN = VRP = R = Z_0$ | $VRN = VRP = R = Z_0$ | $VRN = VRP = R = Z_0$ |
| Recommended $Z_0^{(2)}$ | 50 Ω | 50 Ω | 50 Ω | 50 Ω |

Notes:

1. The SSTL-compatible 25 Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

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Figure 13: SSTL DCI Usage Examples

Figure 14 provides examples illustrating the use of the LVDS_DCI and LVDS_EXT_DCI I/O standards. For a complete list, see the *Virtex-II User Guide* (UG002).

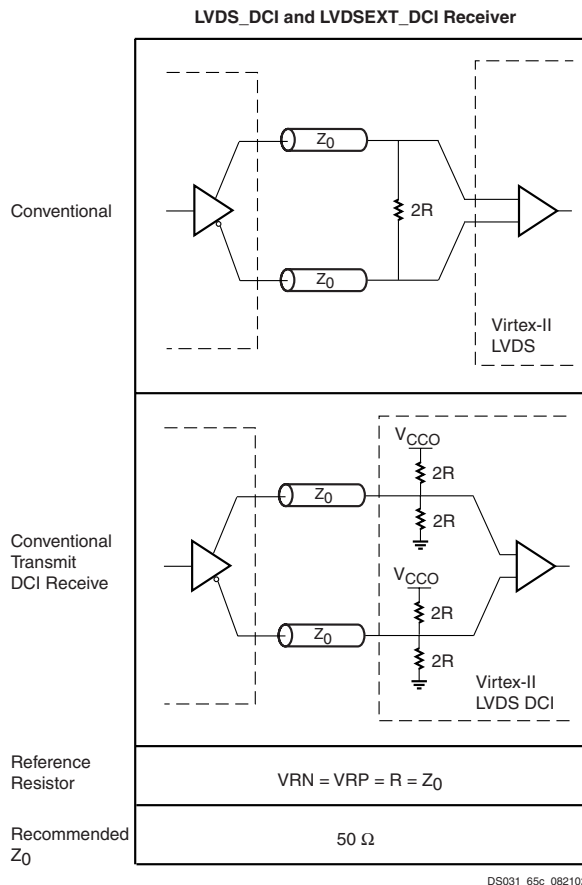


Figure 14: LVDS DCI Usage Examples

Configurable Logic Blocks (CLBs)

The Virtex-II configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in **Figure 15**. A CLB element comprises four similar slices with fast local feedback within the CLB. The four slices are split into two columns of two slices with two independent carry chains and one common shift chain.

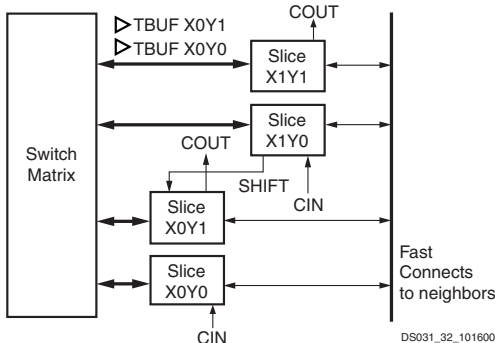


Figure 15: Virtex-II CLB Element

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in **Figure 16**, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

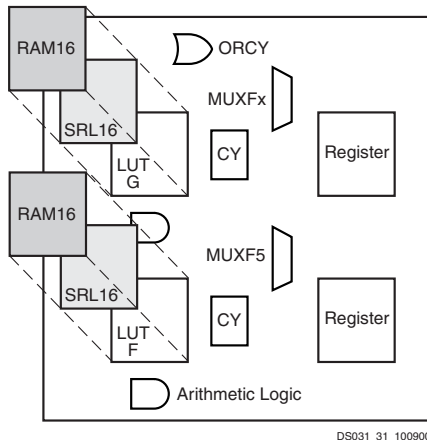


Figure 16: Virtex-II Slice Configuration

The output from the function generator in each slice drives both the slice output and the D input of the storage element. **Figure 17** shows a more detailed view of a single slice.

Configurations

Look-Up Table

Virtex-II function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined Boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in **Figure 17**).

In addition to the basic LUTs, the Virtex-II slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFXs are either MUXF6, MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any functions of six, seven, or eight inputs and selected wide logic functions.

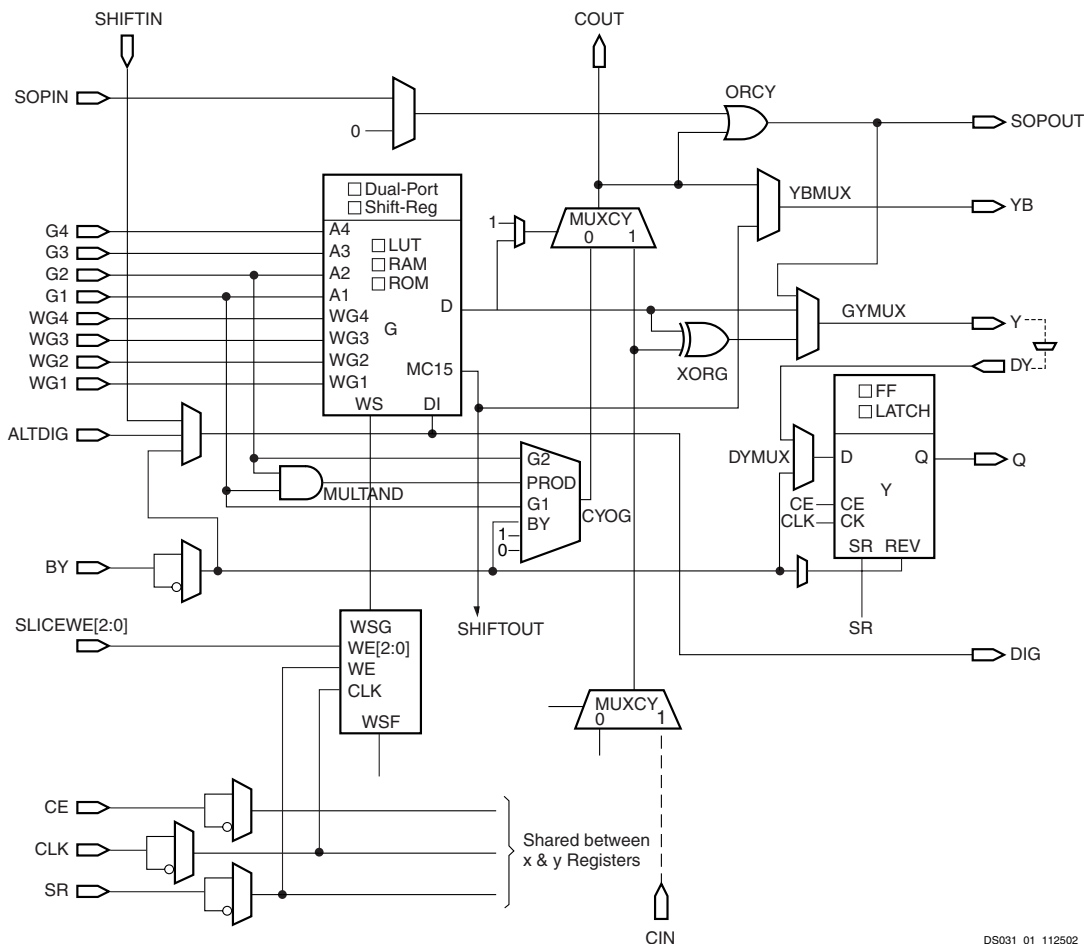
Register/Latch

The storage elements in a Virtex-II slice can be configured as either edge-triggered D-type flip-flops or level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLLOW. SRHIGH forces a logic "1" when SR is asserted. SRLLOW forces a logic "0". When SR is used, a second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition. (See **Figure 18**.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLLOW. Control signals CLK, CE, and SR are common to both storage elements in one slice. All control signals have independent polarities. Any inverter placed on a control input is automatically absorbed.



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Figure 17: Virtex-II Slice (Top Half)

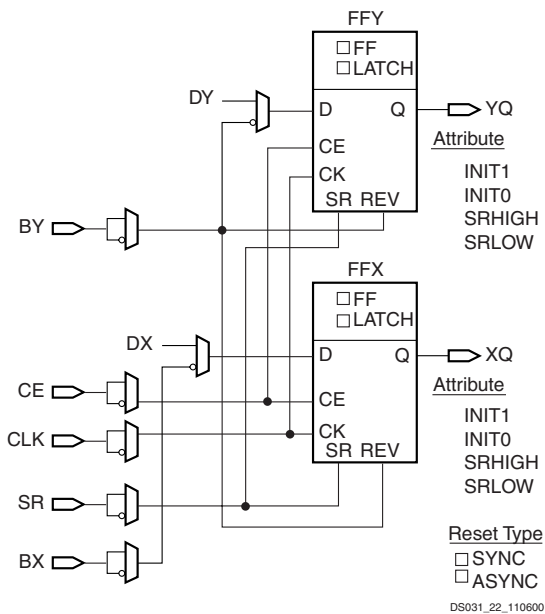


Figure 18: Register/Latch Configuration in a Slice

The set and reset functionality of a register or a latch can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset has precedence over a set, and an asynchronous clear has precedence over a preset.

Distributed SelectRAM Memory

Each function generator (LUT) can implement a 16 x 1-bit synchronous RAM resource called a distributed SelectRAM element. The SelectRAM elements are configurable within a CLB to implement the following:

- Single-Port 16 x 8 bit RAM
- Single-Port 32 x 4 bit RAM
- Single-Port 64 x 2 bit RAM

- Single-Port 128 x 1 bit RAM
- Dual-Port 16 x 4 bit RAM
- Dual-Port 32 x 2 bit RAM
- Dual-Port 64 x 1 bit RAM

Distributed SelectRAM memory modules are synchronous (write) resources. The combinatorial read access time is extremely fast, while the synchronous write simplifies high-speed designs. A synchronous read can be implemented with a storage element in the same slice. The distributed SelectRAM memory and the storage element share the same clock input. A Write Enable (WE) input is active High, and is driven by the SR input.

Table 14 shows the number of LUTs (2 per slice) occupied by each distributed SelectRAM configuration.

Table 14: Distributed SelectRAM Configurations

| RAM | Number of LUTs |
|----------|----------------|
| 16 x 1S | 1 |
| 16 x 1D | 2 |
| 32 x 1S | 2 |
| 32 x 1D | 4 |
| 64 x 1S | 4 |
| 64 x 1D | 8 |
| 128 x 1S | 8 |

Notes:

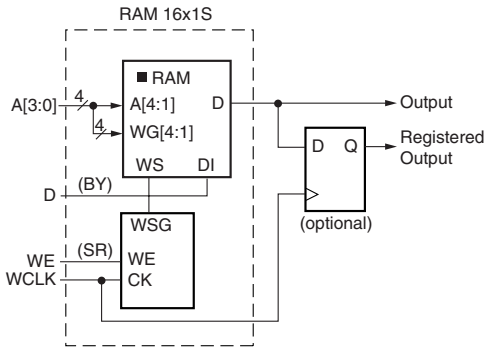
1. S = single-port configuration, and D = dual-port configuration.

For single-port configurations, distributed SelectRAM memory has one address port for synchronous writes and asynchronous reads.

For dual-port configurations, distributed SelectRAM memory has one port for synchronous writes and asynchronous reads and another port for asynchronous reads. The function generator (LUT) has separated read address inputs (A1, A2, A3, A4) and write address inputs (WG1/WF1, WG2/WF2, WG3/WF3, WG4/WF4).

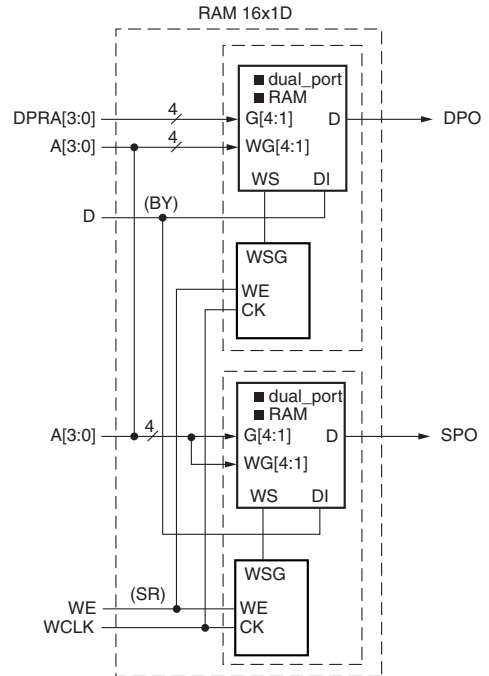
In single-port mode, read and write addresses share the same address bus. In dual-port mode, one function generator (R/W port) is connected with shared read and write addresses. The second function generator has the A inputs (read) connected to the second read-only port address and the W inputs (write) shared with the first read/write port address.

Figure 19, Figure 20, and Figure 21 illustrate various example configurations.



DS031_02_110303

Figure 19: Distributed SelectRAM (RAM16x1S)



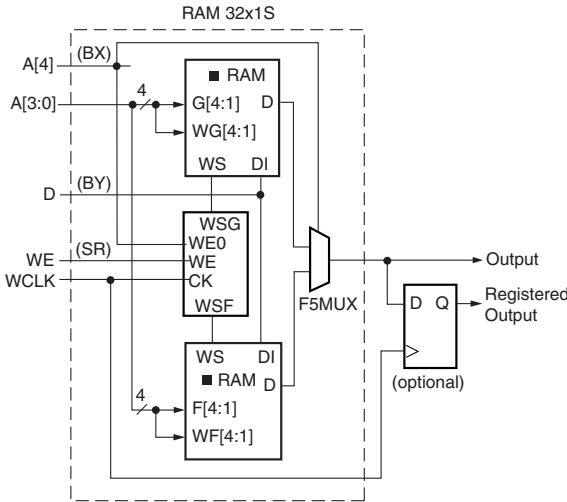
DS031_04_110100

Figure 21: Dual-Port Distributed SelectRAM (RAM16x1D)

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 15 shows the number of LUTs occupied by each configuration.

Table 15: ROM Configuration

| ROM | Number of LUTs |
|---------|----------------|
| 16 x 1 | 1 |
| 32 x 1 | 2 |
| 64 x 1 | 4 |
| 128 x 1 | 8 (1 CLB) |
| 256 x 1 | 16 (2 CLBs) |



DS031_03_110100

Figure 20: Single-Port Distributed SelectRAM (RAM32x1S)

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 22. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however, the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the seventh bit, the eighth bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

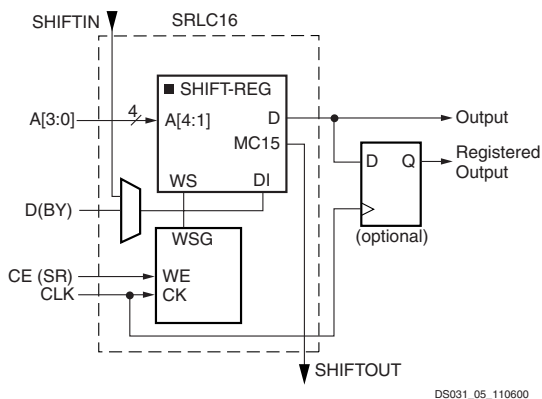


Figure 22: Shift Register Configurations

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 23.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

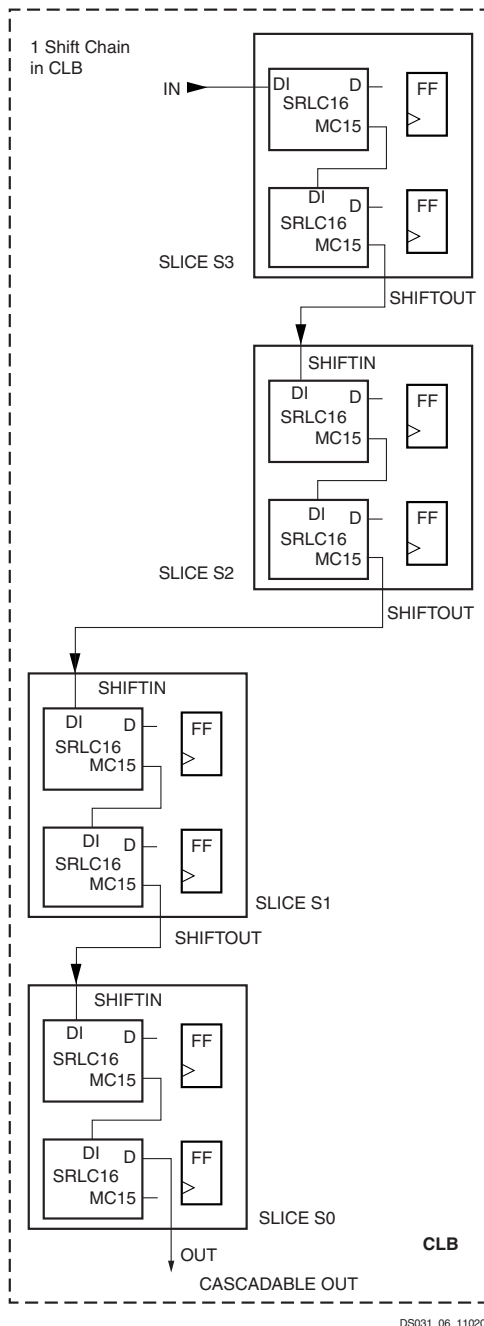


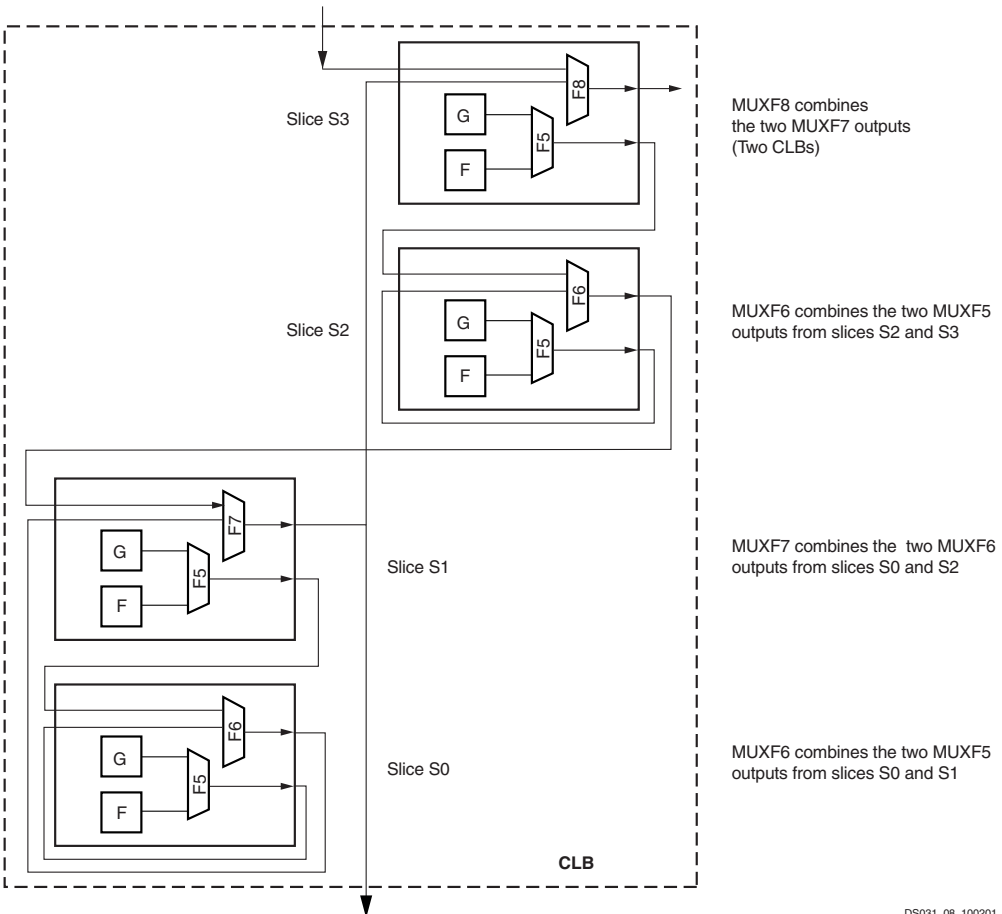
Figure 23: Cascadable Shift Register

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in **Figure 24**. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II User Guide* ([UG002](#)). Any LUT can implement a 2:1 multiplexer.



DS031_08_100201

Figure 24: MUXF5 and MUXFX multiplexers

Fast Lookahead Carry Logic

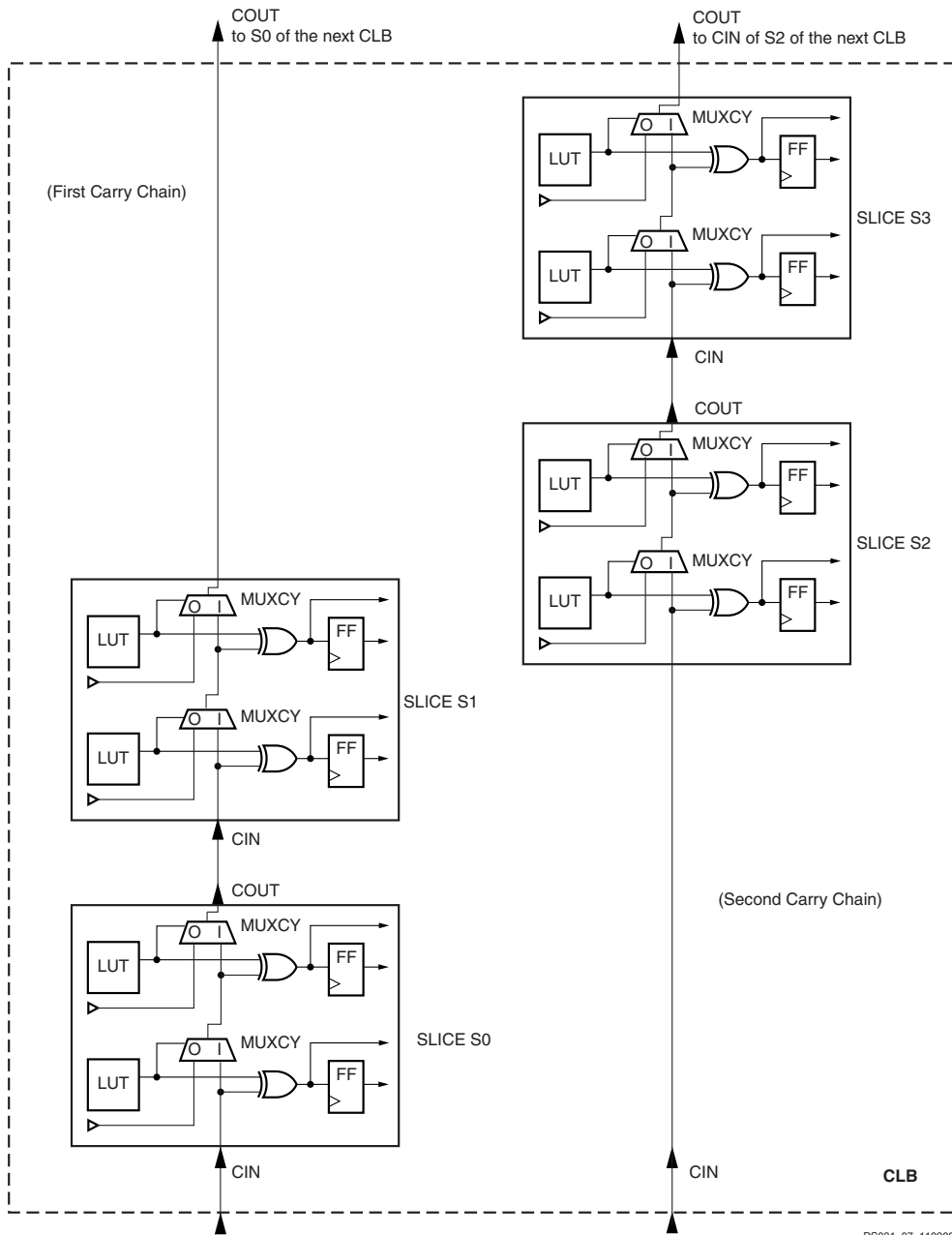
Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the **Figure 25**.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also

be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in **Figure 17**) improves the efficiency of multiplier implementation.



DS031_07_110200

Figure 25: Fast Carry Logic Path

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to

the output of the top MUXCY in the same slice, as shown in Figure 26.

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 27 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

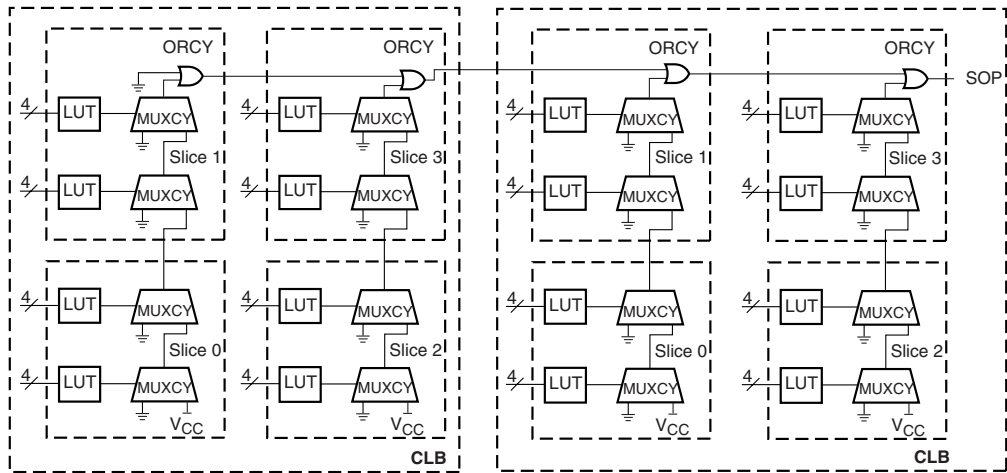


Figure 26: Horizontal Cascade Chain

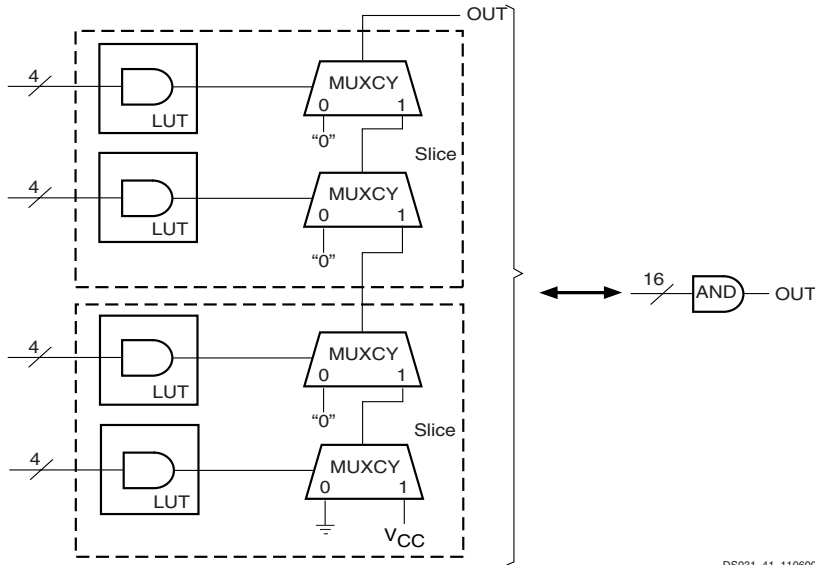


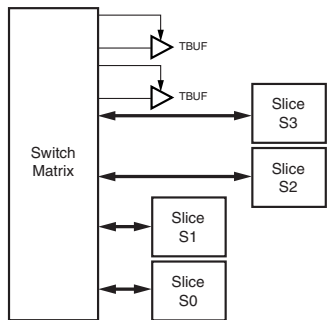
Figure 27: Wide-Input AND Gate (16 Inputs)

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip buses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 28. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state buses.



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Figure 28: Virtex-II 3-State Buffers

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependent especially with larger devices.

Locations/Organization

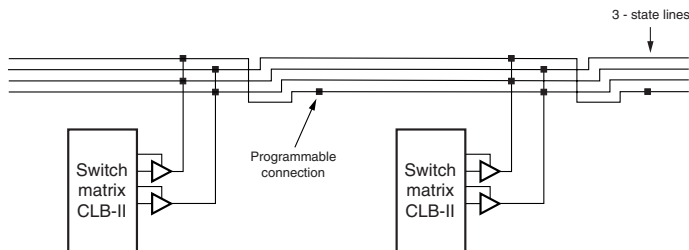
Four horizontal routing resources per CLB are provided for on-chip 3-state buses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 29. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 16 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 16: Virtex-II 3-State Buffers

| Device | 3-State Buffers per Row | Total Number of 3-State Buffers |
|-----------|-------------------------|---------------------------------|
| XQR2V1000 | 64 | 2,560 |
| XQR2V3000 | 112 | 7,168 |
| XQR2V6000 | 176 | 16,896 |



DS031_09_032700

Figure 29: 3-State Buffer Connection to Horizontal Lines

CLB/Slice Configurations

Table 17 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be imple-

mented in one of the configurations listed. Table 18 shows the available resources in all CLBs.

Table 17: Logic Resources in One CLB

| Slices | LUTs | Flip-Flops | MULT_ANDs | Arithmetic & Carry Chains | SOP Chains | Distributed SelectRAM | Shift Registers | TBUF |
|--------|------|------------|-----------|---------------------------|------------|-----------------------|-----------------|------|
| 4 | 8 | 8 | 8 | 2 | 2 | 128 bits | 128 bits | 2 |

Table 18: Virtex-II Logic Resources Available in All CLBs

| Device | CLB Array: Row x Column | Number of Slices | Number of LUTs | Max Distributed SelectRAM or Shift Register (bits) | Number of Flip-Flops | Number of Carry Chains ⁽¹⁾ | Number of SOP Chains ⁽¹⁾ |
|-----------|-------------------------|------------------|----------------|--|----------------------|---------------------------------------|-------------------------------------|
| XQR2V1000 | 40 x 32 | 5,120 | 10,240 | 163,840 | 10,240 | 64 | 80 |
| XQR2V3000 | 64 x 56 | 14,336 | 28,672 | 458,752 | 28,672 | 112 | 128 |
| XQR2V6000 | 96 x 88 | 33,792 | 67,584 | 1,081,344 | 67,584 | 176 | 192 |

Notes:

1. The carry chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for writes) and Data/parity data outputs (for reads).

Operation is synchronous. The block SelectRAM behaves like a register. Control, address, and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, as a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 19.

Table 19: Dual- and Single-Port Configurations

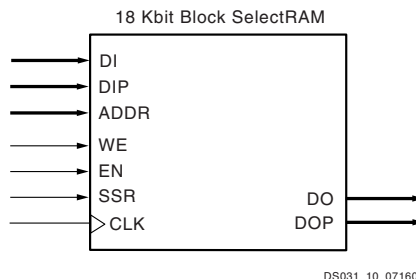
| | |
|-------------|---------------|
| 16K x 1 bit | 2K x 9 bits |
| 8K x 2 bits | 1K x 18 bits |
| 4K x 4 bits | 512 x 36 bits |

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit,

1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of 9-bit, 18-bit, and 36-bit widths is the ability to store a parity bit for every eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 30. Input data bus and output data bus widths are identical.



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Figure 30: 18 Kbit Block SelectRAM Memory in Single-Port Mode

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 20 illustrates the different configurations available on Ports A and B.

Table 20: Dual-Port Mode Configurations

| | | | | | | |
|--------|----------|----------|----------|----------|----------|----------|
| Port A | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 | 16K x 1 |
| Port B | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 |
| Port A | 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 | 8K x 2 | |
| Port B | 8K x 2 | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 | |
| Port A | 4K x 4 | 4K x 4 | 4K x 4 | 4K x 4 | | |
| Port B | 4K x 4 | 2K x 9 | 1K x 18 | 512 x 36 | | |
| Port A | 2K x 9 | 2K x 9 | 2K x 9 | | | |
| Port B | 2K x 9 | 1K x 18 | 512 x 36 | | | |
| Port A | 1K x 18 | 1K x 18 | | | | |
| Port B | 1K x 18 | 512 x 36 | | | | |
| Port A | 512 x 36 | | | | | |
| Port B | 512 x 36 | | | | | |

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from Port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations, the 16 Kbit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 Kbit subset of the memory block equal to 16 Kbits.

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 31. The two ports have independent inputs and outputs and are independently clocked.

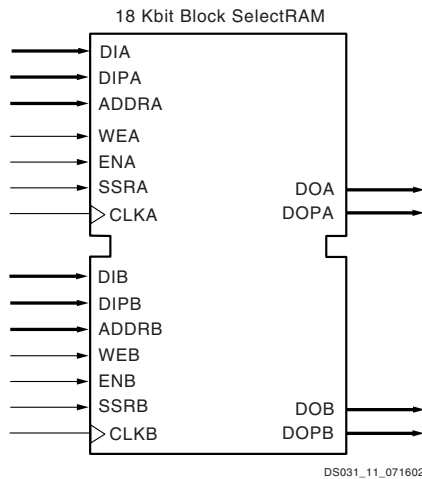


Figure 31: 18 Kbit Block SelectRAM in Dual-Port Mode

Port Aspect Ratios

Table 21 shows the depth and the width aspect ratios for the 18 Kbit block SelectRAM. Virtex-II block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 21: 18 Kbit Block SelectRAM Port Aspect Ratio

| Width | Depth | Address Bus | Data Bus | Parity Bus |
|-------|--------|-------------|------------|-------------|
| 1 | 16,384 | ADDR[13:0] | DATA[0] | N/A |
| 2 | 8,192 | ADDR[12:0] | DATA[1:0] | N/A |
| 4 | 4,096 | ADDR[11:0] | DATA[3:0] | N/A |
| 9 | 2,048 | ADDR[10:0] | DATA[7:0] | Parity[0] |
| 18 | 1,024 | ADDR[9:0] | DATA[15:0] | Parity[1:0] |
| 36 | 512 | ADDR[8:0] | DATA[31:0] | Parity[3:0] |

Read/Write Operations

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. "WRITE_FIRST"

The "WRITE_FIRST" option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 32.

2. "READ_FIRST"

The "READ_FIRST" option is a read-before-write mode. The same clock edge that writes data input (DI) into the

memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 33.

3. "NO_CHANGE"

The "NO_CHANGE" option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as "NO_CHANGE", only a read operation loads a new value in the output register DO, as shown in Figure 34.

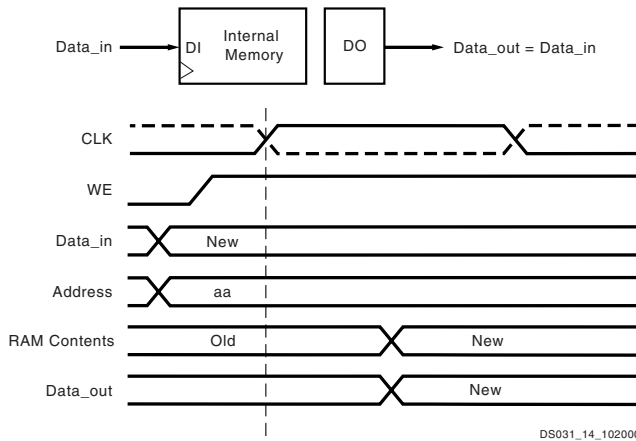


Figure 32: WRITE_FIRST Mode

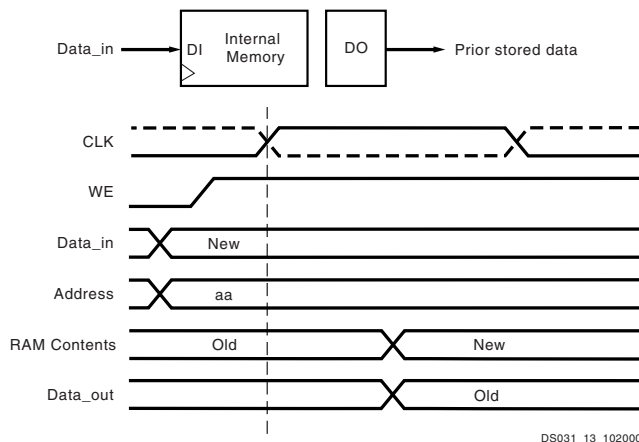


Figure 33: READ_FIRST Mode

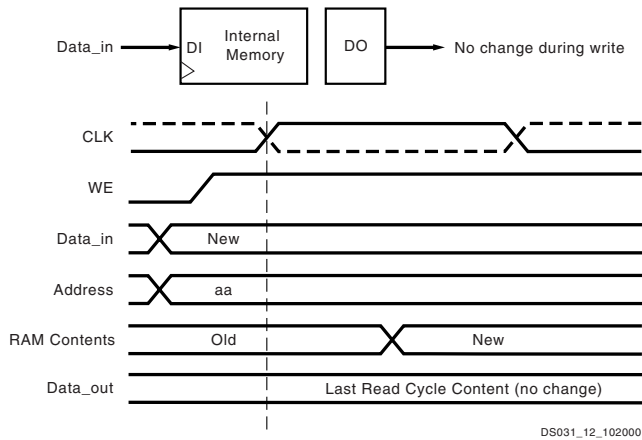


Figure 34: NO_CHANGE Mode

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 22. All control inputs including the clock have an optional inversion.

Table 22: Control Functions

| Control Signal | Function |
|----------------|--|
| CLK | Read and Write Clock |
| EN | Enable affects Read, Write, Set, Reset |
| WE | Write Enable |
| SSR | Set DO register to SRVAL (attribute) |

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available

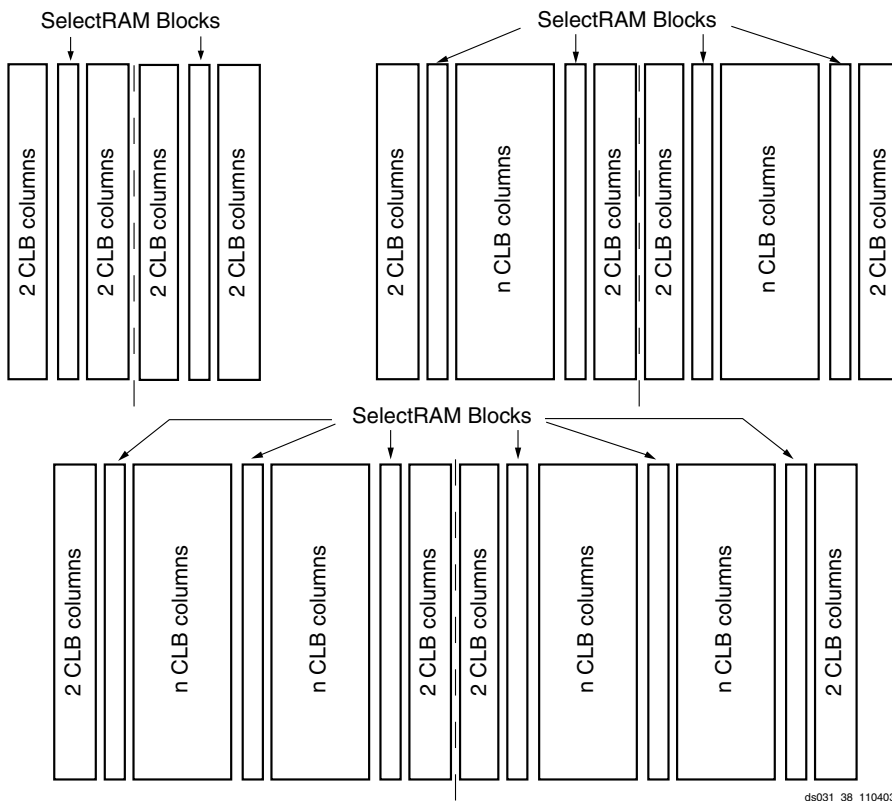
for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are located in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 23.

Table 23: SelectRAM Memory Floor Plan

| Device | Columns | SelectRAM Blocks | |
|-----------|---------|------------------|-------|
| | | Per Column | Total |
| XQR2V1000 | 4 | 10 | 40 |
| XQR2V3000 | 6 | 16 | 96 |
| XQR2V6000 | 6 | 24 | 144 |



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Figure 35: Block SelectRAM (2-column, 4-column, and 6-column)

Total Amount of SelectRAM Memory

Table 24 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18 Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 24: Virtex-II SelectRAM Memory Available

| Device | Total SelectRAM Memory | | |
|-----------|------------------------|----------|-----------|
| | Blocks | in Kbits | in Bits |
| XQR2V1000 | 40 | 720 | 737,280 |
| XQR2V3000 | 96 | 1,728 | 1,769,472 |
| XQR2V6000 | 144 | 2,592 | 2,654,208 |

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 36.

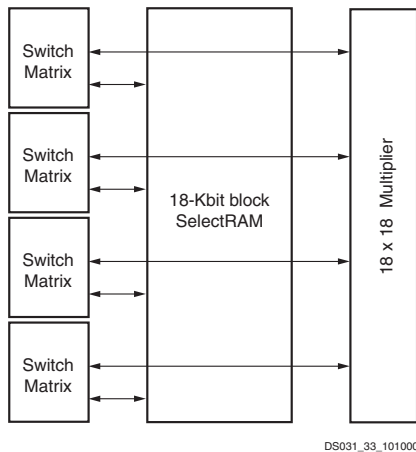


Figure 36: SelectRAM and Multiplier Blocks

Association with Block SelectRAM Memory

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 37 shows a multiplier block.

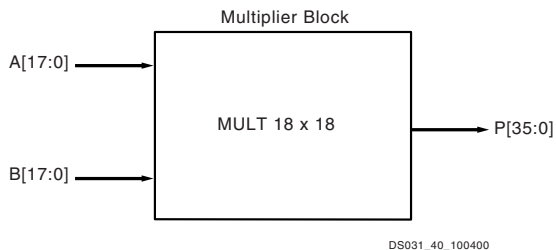


Figure 37: Multiplier Block

Locations/Organization

Multiplier organization is identical to the 18 Kbit SelectRAM organization, because each multiplier is associated with an 18 Kbit block SelectRAM resource.

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to **Configurable Logic Blocks (CLBs)**).

Table 25: Multiplier Floor Plan

| Device | Columns | Multipliers | |
|-----------|---------|-------------|-------|
| | | Per Column | Total |
| XQR2V1000 | 4 | 10 | 40 |
| XQR2V3000 | 6 | 16 | 96 |
| XQR2V6000 | 6 | 24 | 144 |

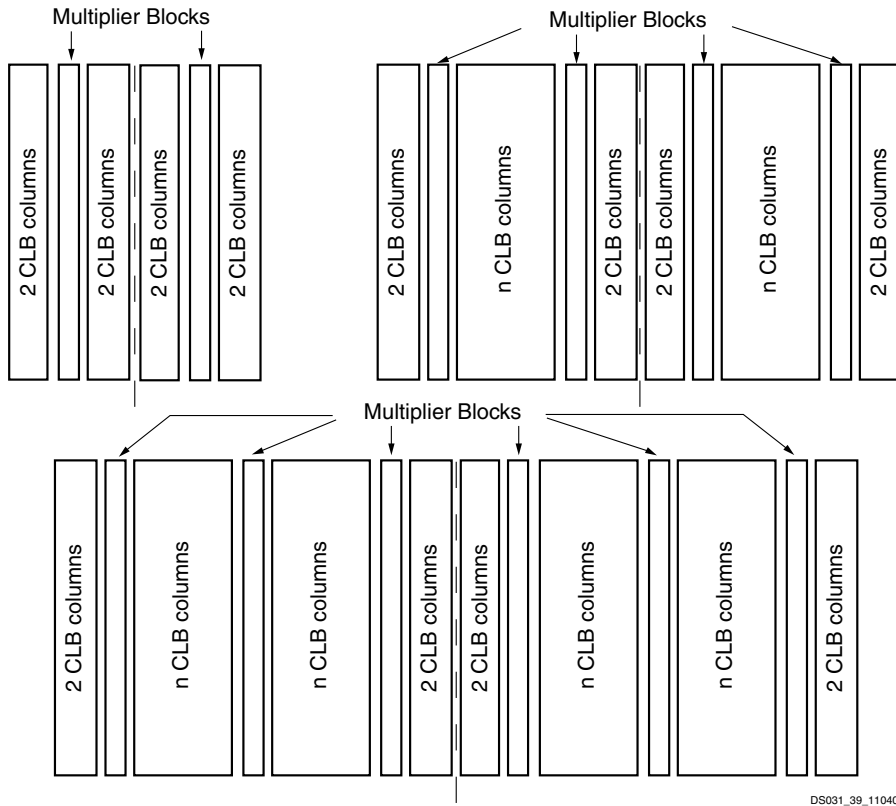


Figure 38: Multipliers (2-column, 4-column, and 6-column)

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 39.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

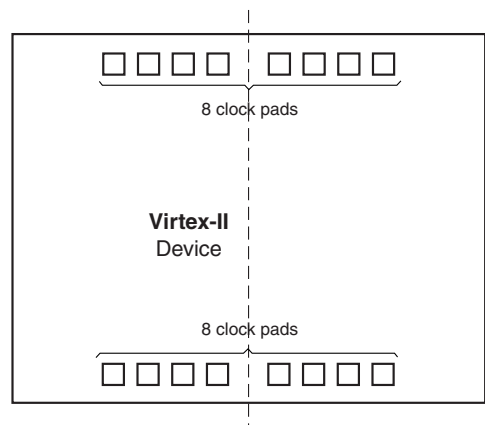


Figure 39: Virtex-II Clock Pads

Each global clock buffer can be driven by either the clock pad to distribute a clock directly to the device, or the Digital Clock Manager (DCM), discussed in **Digital Clock Manager (DCM)**, page 36. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in **Figure 40**.

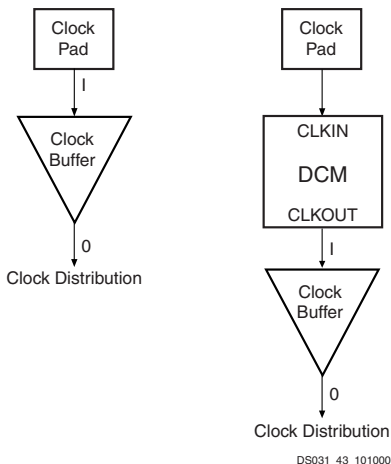


Figure 40: Virtex-II Clock Distribution Configurations

Global clock buffers are used to distribute the clock to some or all synchronous logic elements (such as registers in CLBs and IOBs, and SelectRAM blocks).

Eight global clocks can be used in each quadrant of the Virtex-II device. Designers should consider the clock distri-

bution detail of the device prior to pin-locking and floorplanning (see the *Virtex-II User Guide*, **UG002**).

Figure 42 shows clock distribution in Virtex-II devices.

In each quadrant, up to eight clocks are organized in clock rows. A clock row supports up to 16 CLB rows (eight up and eight down). For the largest devices a new clock row is added, as necessary.

To reduce power consumption, any unused clock branches remain static.

Global clocks are driven by dedicated clock buffers (BUFG), which can also be used to gate the clock (BUFGCE) or to multiplex between two independent clock inputs (BUFGMUX).

The most common configuration option of this element is as a buffer. A BUFG function in this (global buffer) mode, is shown in **Figure 41**.

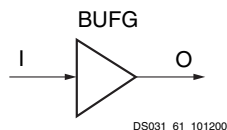


Figure 41: Virtex-II BUFG Function

The Virtex-II global clock buffer BUFG can also be configured as a clock enable/disable circuit (**Figure 43**), as well as a two-input clock multiplexer (**Figure 44**). A functional description of these two options is provided below. Each of them can be used in either of two modes, selected by configuration: rising clock edge or falling clock edge.

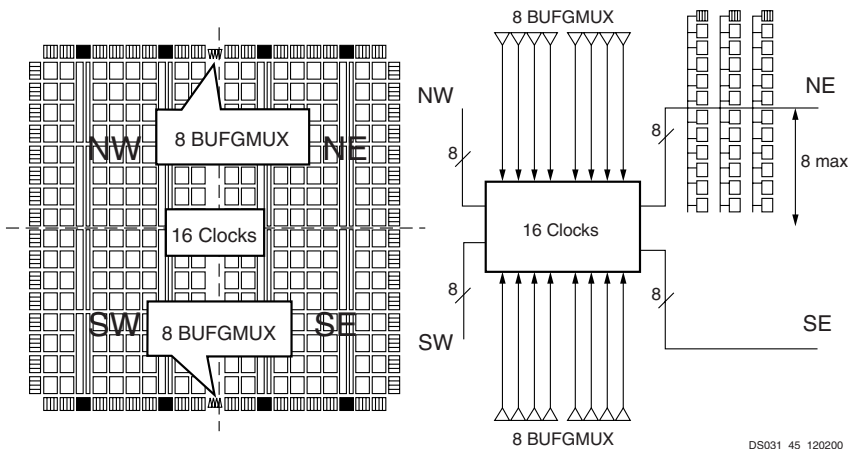


Figure 42: Virtex-II Clock Distribution

This section describes the rising clock edge option. For the opposite option, falling clock edge, just change all "rising" references to "falling" and all "High" references to "Low", except for the description of the CE or S levels. The rising clock edge option uses the BUFGCE and BUFGMUX primitives. The falling clock edge option uses the BUFGCE_1 and BUFGMUX_1 primitives.

BUFGCE

If the CE input is active (High) prior to the incoming rising clock edge, this Low-to-High-to-Low clock pulse passes through the clock buffer. Any level change of CE during the incoming clock High time has no effect.

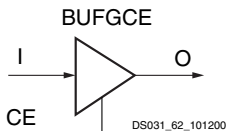


Figure 43: Virtex-II BUFGCE Function

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, and a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect.

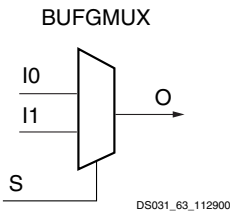


Figure 44: Virtex-II BUFGMUX Function

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock, that is, prior to the rising edge of the BUFGMUX output O. Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 45 shows a switchover from CLK0 to CLK1.

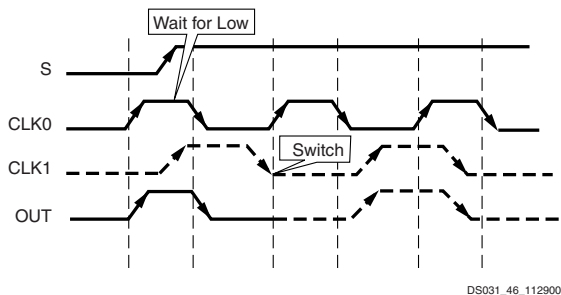


Figure 45: Clock Multiplexer Waveform Diagram

In Figure 45:

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features:

- **Clock De-skew:** The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis:** The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting:** The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 46). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

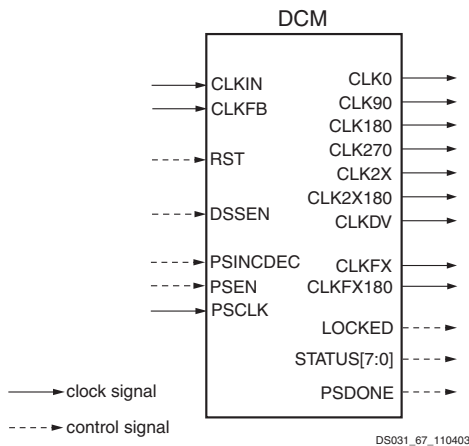


Figure 46: Digital Clock Manager

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM.
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 26.

Table 26: DCM Status Pins

| Status Pin | Function |
|------------|----------------------|
| 0 | Phase Shift Overflow |
| 1 | CLKIN Stopped |
| 2 | CLKFX Stopped |
| 3 | N/A |
| 4 | N/A |
| 5 | N/A |
| 6 | N/A |
| 7 | N/A |

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers. Specifications for M and D are provided under **DCM Timing Parameters**. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Phase Shifting

The DCM provides additional control over clock skew through either coarse- or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 47 illustrates the effects of fine-phase

shifting. For more information on DCM features, see the *Virtex-II User Guide* (UG002).

Table 27 lists fine-phase shifting control pins, when used in variable mode.

Table 27: Fine-Phase Shifting Control Pins

| Control Pin | Direction | Function |
|-------------|-----------|------------------------|
| PSINCDEC | in | Increment or decrement |
| PSEN | in | Enable ± phase shift |
| PSCLK | in | Clock for phase shift |
| PSDONE | out | Active when completed |

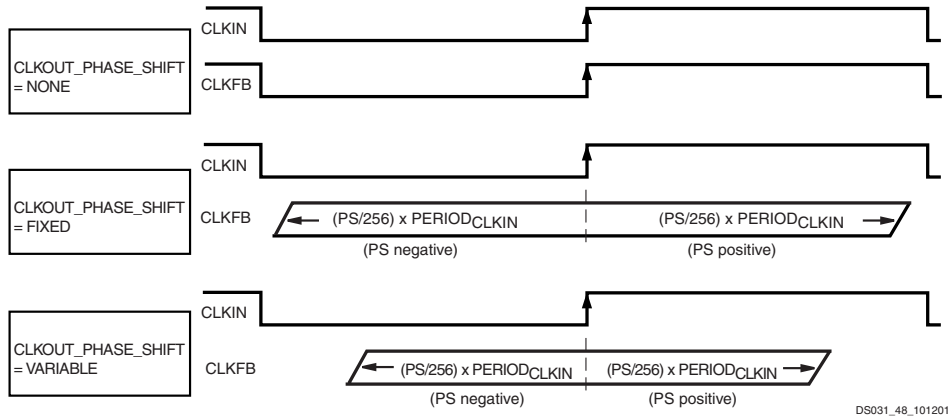


Figure 47: Fine-Phase Shifting Effects

Two separate components of the phase shift range must be understood:

- PHASE_SHIFT attribute range
- FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

$$\text{Phase Shift (ns)} = (\text{PHASE_SHIFT}/256) * \text{PERIOD}_{\text{CLKIN}}$$

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit. Across process, voltage, and temperature, this absolute range is guaranteed to be as specified under **DCM Timing Parameters**.

$$\text{Absolute range (fixed mode)} = \pm \text{FINE_SHIFT_RANGE}$$

$$\text{Absolute range (variable mode)} = \pm \text{FINE_SHIFT_RANGE}/2$$

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric, dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line, thus dividing the total delay line range in half. In fixed mode, since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertion into either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If $\text{PERIOD}_{\text{CLKIN}} = 2 * \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 128, and in variable mode it is limited to ± 64.
- If $\text{PERIOD}_{\text{CLKIN}} = \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT in fixed mode is limited to ± 255, and in variable mode it is limited to ± 128.
- If $\text{PERIOD}_{\text{CLKIN}} \leq 0.5 * \text{FINE_SHIFT_RANGE}$, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to [Table 28](#). (For actual values, see [QPro Virtex-II Switching](#)

Characteristics.) The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high-frequency mode. High or low-frequency mode is selected by an attribute.

Table 28: DCM Frequency Ranges

| Output Clock | Low-Frequency Mode | | High-Frequency Mode | |
|-----------------|--------------------|-------------------|---------------------|-------------------|
| | CLKIN Input | CLK Output | CLKIN Input | CLK Output |
| CLK0, CLK180 | CLKIN_FREQ_DLL_LF | CLKOUT_FREQ_1X_LF | CLKIN_FREQ_DLL_HF | CLKOUT_FREQ_1X_HF |
| CLK90, CLK270 | CLKIN_FREQ_DLL_LF | CLKOUT_FREQ_1X_LF | NA | NA |
| CLK2X, CLK2X180 | CLKIN_FREQ_DLL_LF | CLKOUT_FREQ_2X_LF | NA | NA |
| CLKDV | CLKIN_FREQ_DLL_LF | CLKOUT_FREQ_DV_LF | CLKIN_FREQ_DLL_HF | CLKOUT_FREQ_DV_HF |
| CLKFX, CLKFX180 | CLKIN_FREQ_FX_LF | CLKOUT_FREQ_FX_LF | CLKIN_FREQ_FX_HF | CLKOUT_FREQ_FX_HF |

Locations/Organization

Virtex-II DCMs are placed on the top and the bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in [Table 29](#).

Table 29: DCM Organization

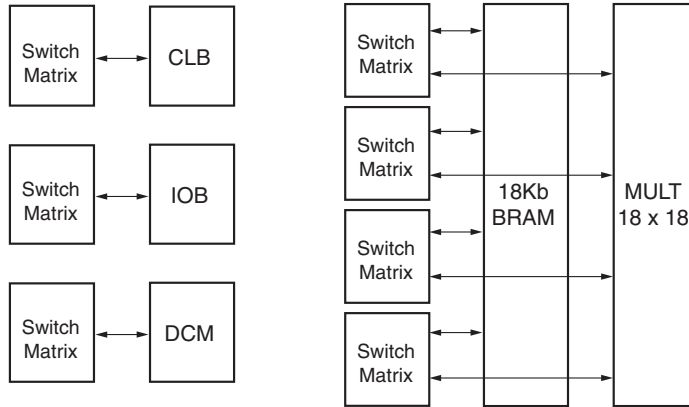
| Device | Columns | DCMs |
|-----------|---------|------|
| XQR2V1000 | 4 | 8 |
| XQR2V3000 | 6 | 12 |
| XQR2V6000 | 6 | 12 |

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected

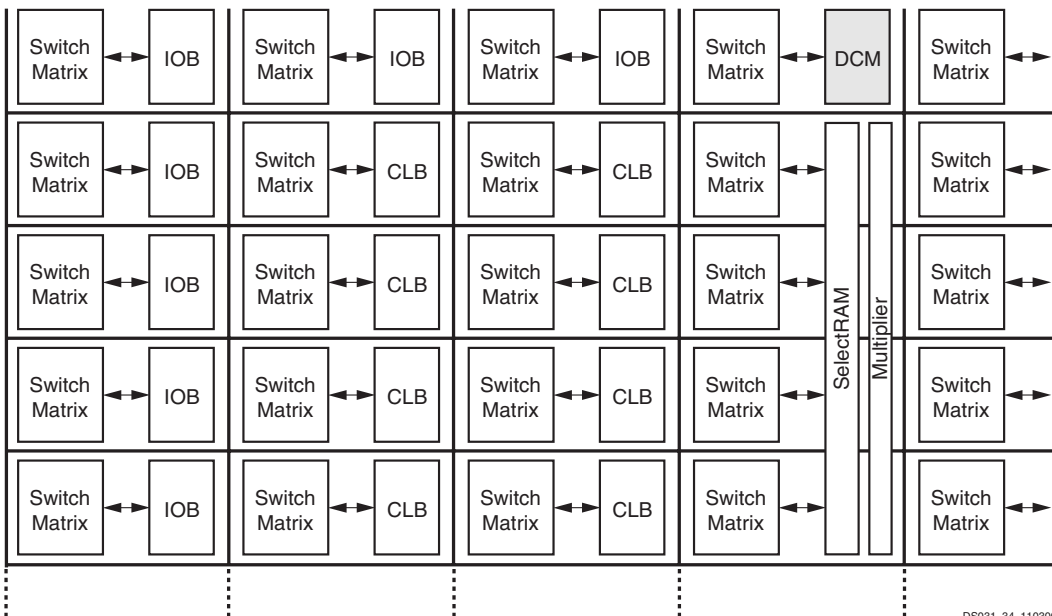
to an identical switch matrix for access to global routing resources, as shown in Figure 48.

Each Virtex-II device can be represented as an array of switch matrices with logic blocks attached, as illustrated in Figure 49.



DS031_55_101000

Figure 48: Active Interconnect Technology



DS031_34_110300

Figure 49: Routing Resources

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an

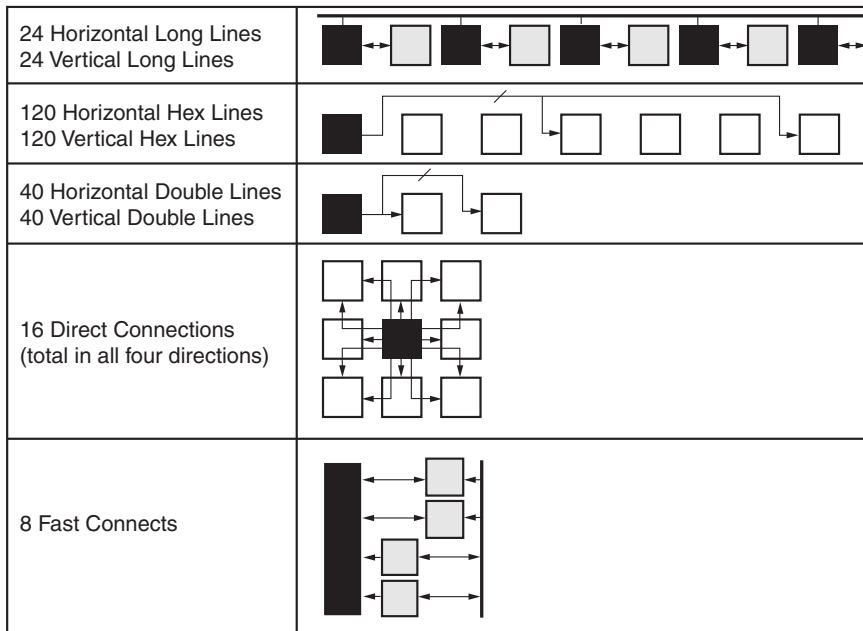
incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

As shown in **Figure 50**, Virtex-II devices have fully buffered programmable interconnections, with a number of



DS031_60_110403

Figure 50: Hierarchical Routing Resources

In **Figure 50**:

- Long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- Hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).
- Double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).

- Direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- Fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available:

- There are eight global clock nets per quadrant (see **Global Clock Multiplexer Buffers**).
- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row. (See **3-State Buffers**.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY

output signals vertically to the adjacent slice. (See **CLB/Slice Configurations**.)

- One dedicated SOP chain per slice row (two per CLB row) propagates ORCY output logic signals horizontally to the adjacent slice. (See **Sum of Products**.)
- One dedicated shift chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See **Shift Registers**, page 22.)

Creating a Design

Creating Virtex-II designs is easy with Xilinx Integrated Synthesis Environment (ISE) development systems, which support advanced design capabilities, including ProActive Timing Closure, integrated logic analysis, and the fastest place and route runtimes in the industry. ISE solutions enable designers to get the performance they need, quickly and easily.

As a result of the ongoing cooperative development efforts between Xilinx and EDA Alliance partners, designers can take advantage of the benefits provided by EDA technologies in the programmable logic design process. Xilinx development systems are available in a number of easy to use configurations, collectively known as the ISE Series.

ISE Alliance

The ISE Alliance solution is designed to plug and play within an existing design environment. Built using industry standard data formats and netlists, these stable, flexible products enable Alliance EDA partners to deliver their best design automation capabilities to Xilinx customers, along with the time to market benefits of ProActive Timing Closure.

ISE Foundation

The ISE Foundation solution delivers the benefits of true HDL-based design in a seamlessly integrated design environment. An intuitive project navigator, as well as powerful HDL design and two HDL synthesis tools, ensure that high-quality results are achieved quickly and easily. The ISE Foundation product includes:

- State Diagram entry using Xilinx StateCAD
- Automatic HDL Testbench generation using Xilinx HDLBencher
- HDL Simulation using ModelSim XE

Design Flow

Virtex-II design flow proceeds as follows:

- Design Entry
- Synthesis
- Implementation
- Verification

Most programmable logic designers iterate through these steps several times in the process of completing a design.

Design Entry

All Xilinx ISE development systems support the mainstream EDA design entry capabilities, ranging from schematic design to advanced HDL design methodologies. Given the high densities of the Virtex-II family, designs are created most efficiently using HDLs. To further improve their time to market, many Xilinx customers employ incremental, modular, and Intellectual Property (IP) design techniques. When properly used, these techniques further accelerate the logic design process.

To enable designers to leverage existing investments in EDA tools and to ensure high-performance design flows, Xilinx jointly develops tools with leading EDA vendors, including:

- Aldec
- Cadence
- Exemplar
- Mentor Graphics
- Model Technology
- Synopsys
- Synplicity

Complete information on Alliance Series partners and their associated design flows is available at <http://www.xilinx.com> on the Xilinx Alliance Series web page.

The ISE Foundation product offers schematic entry and HDL design capabilities as part of an integrated design solution, enabling one-stop shopping. These capabilities are powerful, easy to use, and they support the full portfolio of Xilinx programmable logic devices. HDL design capabilities include a color-coded HDL editor with integrated language templates, state diagram entry, and Core generation capabilities.

Synthesis

The ISE Alliance product is engineered to support advanced design flows with the industry's best synthesis tools. Advanced design methodologies include:

- Physical Synthesis
- Incremental synthesis
- RTL floorplanning
- Direct physical mapping

The ISE Foundation product seamlessly integrates synthesis capabilities purchased directly from Exemplar, Synopsys, and Synplicity. In addition, it includes the capabilities of Xilinx Synthesis Technology.

A benefit of having two seamlessly integrated synthesis engines within an ISE design flow is the ability to apply alternative sets of optimization techniques on designs, helping to ensure that designers can meet even the toughest timing requirements.

Design Implementation

The ISE Series development systems include Xilinx timing-driven implementation tools, frequently called “place and route” or “fitting” software. This robust suite of tools enables the creation of an intuitive, flexible, tightly integrated design flow that efficiently bridges “logical” and “physical” design domains. This simplifies the task of defining a design, including its behavior, timing requirements, and optional layout (or floorplanning), as well as simplifying the task of analyzing reports generated during the implementation process.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry’s most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows,

which are robust capabilities enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is “Modular Design”, part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical “logic block”, and perform synthesis, verification, and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx website for a list of supported EDA partners). When used in conjunction with one of the EDA partners’ floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical “logic block” to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from “my module works in simulation” to “my module works in the FPGA”. This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Configuration

Virtex-II devices are configured by loading application-specific configuration data into the internal configuration memory. Configuration is carried out using a subset of the device pins, some of which are dedicated, while others can be re-used as general purpose inputs and outputs once configuration is complete.

Depending on the system design, several configuration modes are supported, selectable via mode pins. The mode pins M2, M1, and M0 are dedicated pins. An additional pin, HSWAP_EN, is used in conjunction with the mode pins to select whether user I/O pins have pull-ups during configura-

tion. By default, HSWAP_EN is tied High (internal pull-up), which shuts off the pull-ups on the user I/O pins during configuration. When HSWAP_EN is tied Low, user I/Os have pull-ups during configuration. Other dedicated pins are CCLK (the configuration clock pin), DONE, PROG_B, and the boundary-scan pins: TDI, TDO, TMS, and TCK. Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or an input accepting an externally generated clock. The configuration pins and boundary-scan pins are independent of the V_{CCO} . The auxiliary power supply (V_{CCAUX}) of 3.3V is used for these pins. All configuration pins are LVTTL 12 mA. (See **QPro Virtex-II DC Characteristics**.)

A persist option is available which can be used to force the configuration pins to retain their configuration function even after device configuration is complete. If the persist option is not selected, then the configuration pins with the exception of CCLK, PROG_B, and DONE can be used as user I/O in normal operation. The persist option does not apply to the boundary-scan related pins. The persist feature is valuable in applications which employ partial reconfiguration or reconfiguration on the fly.

Configuration Modes

Virtex-II supports the following five configuration modes:

- Slave-serial mode
- Master-serial mode
- Slave SelectMAP mode
- Master SelectMAP mode
- Boundary-Scan mode (IEEE 1532/IEEE 1149)

A detailed description of configuration modes is provided in the *Virtex-II User Guide* ([UG002](#)).

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other serial source of configuration data. The CCLK pin on the FPGA is an input in this mode. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of the externally generated CCLK.

Multiple FPGAs can be daisy chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected.

Master-Serial Mode

In master-serial mode, the CCLK pin is an output pin. It is the Virtex-II FPGA device that drives the configuration clock on the CCLK pin to a Xilinx Serial PROM, which in turn

feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration.

Slave SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the Virtex-II FPGA device with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, an active-Low Chip Select (CS_B) signal, and a Write signal (RDWR_B). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If RDWR_B is asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback using the persist option.

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and can be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, RDWR_B, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by deasserting the CS_B pin of each device in turn and writing the appropriate data.

Master SelectMAP Mode

This mode is a master version of the SelectMAP mode. The device is configured byte-wide on a CCLK supplied by the Virtex-II FPGA. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In boundary-scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using boundary scan is compliant with IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes.

Table 30: Virtex-II Configuration Mode Pin Settings

| Configuration Mode ⁽¹⁾ | M2 | M1 | M0 | CCLK Direction | Data Width | Serial D _{OUT} ⁽²⁾ |
|-----------------------------------|----|----|----|----------------|------------|--|
| Master Serial | 0 | 0 | 0 | Out | 1 | Yes |
| Slave Serial | 1 | 1 | 1 | In | 1 | Yes |
| Master SelectMAP | 0 | 1 | 1 | Out | 8 | No |
| Slave SelectMAP | 1 | 1 | 0 | In | 8 | No |
| Boundary Scan | 1 | 0 | 1 | N/A | 1 | No |

Notes:

1. The HSWAP_EN pin controls the pullups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pullups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 31 lists the total number of bits required to configure each device.

Table 31: Virtex-II Bitstream Lengths

| Device | # of Configuration Bits |
|-----------|-------------------------|
| XQR2V1000 | 3,753,432 |
| XQR2V3000 | 9,595,304 |
| XQR2V6000 | 19,760,560 |

Notes:

1. These values are only valid for STEPPING LEVEL 1.
2. Only STEPPING LEVEL 1 should be used with QPro devices.

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the

start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary Scan modes.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II User Guide* ([UG002](#)).

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II User Guide*. Your local FAE can also provide specific information on this feature.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip,

while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration "frame" of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

QPro Virtex-II Electrical Characteristics

QPro Virtex-II devices are only available with the –4 speed grade. QPro Virtex-II DC and AC characteristics are specified for military grade. Except for the operating temperature range, or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a –4 speed grade military device are the same as for a –4 speed grade commer-

cial device). All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

QPro Virtex-II DC Characteristics

Table 32: Absolute Maximum Ratings

| Symbol | Description ⁽¹⁾ | | Units |
|--------------------------------|---|--------------------------------|-------|
| V _{CCINT} | Internal supply voltage relative to GND | –0.5 to 1.65 | V |
| V _{CCAUX} | Auxiliary supply voltage relative to GND | –0.5 to 4.0 | V |
| V _{CCO} | Output drivers supply voltage relative to GND | –0.5 to 4.0 | V |
| V _{BATT} | Key memory battery backup supply | –0.5 to 4.0 | V |
| V _{REF} | Input reference voltage | –0.5 to V _{CCO} + 0.5 | V |
| V _{IN} ⁽³⁾ | Input voltage relative to GND (user and dedicated I/Os) | –0.5 to V _{CCO} + 0.5 | V |
| V _{TS} | Voltage applied to 3-state output (user and dedicated I/Os) | –0.5 to 4.0 | V |
| T _{STG} | Storage temperature (ambient) | –65 to +150 | °C |
| T _{SOL} | Maximum soldering temperature | +220 | °C |
| T _J | Operating junction temperature ⁽²⁾ | +125 | °C |

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the [Device Packaging](#) information on the Xilinx website.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Table 33: Recommended Operating Conditions

| Symbol | Description | Package | Min | Max | Units |
|--------------------|--|---------|-------|-------|-------|
| V _{CCINT} | Internal supply voltage relative to GND, T _C = -55° C to +125° C | Ceramic | 1.425 | 1.575 | V |
| | Internal supply voltage relative to GND, T _J = -55° C to +125° C | Plastic | 1.425 | 1.575 | V |
| V _{CCAUX} | Auxiliary supply voltage relative to GND, T _C = -55° C to +125° C | Ceramic | 3.135 | 3.465 | V |
| | Auxiliary supply voltage relative to GND, T _J = -55° C to +125° C | Plastic | 3.135 | 3.465 | V |
| V _{CCO} | Supply voltage relative to GND, T _C = -55° C to +125° C | Ceramic | 1.2 | 3.6 | V |
| | Supply voltage relative to GND, T _J = -55° C to +125° C | Plastic | 1.2 | 3.6 | V |
| V _{BATT} | Battery voltage relative to GND, T _C = -55° C to +125° C | Ceramic | 1.0 | 3.6 | V |
| | Battery voltage relative to GND, T _J = -55° C to +125° C | Plastic | 1.0 | 3.6 | V |

Notes:

1. If battery is not used, do not connect V_{BATT}.
2. Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5 V.
4. Limit the noise at the power supply to be within 200 mV peak-to-peak.
5. For power bypassing guidelines, see Xilinx Application Note [XAPP623](#).

Table 34: DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Device | Min | Max | Units |
|--------------------|---|--------|--------|-----|-------|
| V _{DRINT} | Data retention V _{CCINT} voltage | All | 1.2 | | V |
| V _{DRI} | Data retention V _{CCAUX} voltage | All | 2.5 | | V |
| I _{REF} | V _{REF} current per bank | All | -10 | +10 | μA |
| I _L | Input leakage current | All | -10 | +10 | μA |
| C _{IN} | Input capacitance | All | | 10 | pF |
| I _{RPU} | Pad pull-up (when selected) @ V _{IN} = 0 V, V _{CCO} = 3.3 V (sample tested) | All | Note 1 | 250 | μA |
| I _{RPD} | Pad pull-down (when selected) @ V _{IN} = 3.6 V (sample tested) | All | Note 1 | 250 | μA |
| I _{BATT} | Battery supply current | All | | 100 | nA |

Notes:

1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 35: Quiescent Supply Current

| Symbol | Description | Device | Min | Typical | Max | Units |
|--------------|---|-----------|-----|---------|------|-------|
| I_{CCINTQ} | Quiescent V_{CCINT} supply current | XQR2V1000 | | 100 | 0.50 | A |
| | | XQR2V3000 | - | 200 | 1.30 | |
| | | XQR2V6000 | | 250 | 1.50 | |
| I_{CCOQ} | Quiescent V_{CCO} supply current ^(1,2) | XQR2V1000 | | 1.0 | 6.25 | mA |
| | | XQR2V3000 | - | 2.0 | 6.25 | |
| | | XQR2V6000 | | 2.0 | 6.25 | |
| I_{CCAUXQ} | Quiescent V_{CCAUX} supply current ^(1,2) | XQR2V1000 | | 10 | 30 | mA |
| | | XQR2V3000 | - | 20 | 95 | |
| | | XQR2V6000 | | 25 | 95 | |

Notes:

1. With no output current loads and no active input pull-up resistors. All I/O pins are 3-stated and floating.
2. If DCI or differential signaling is used, more accurate values can be obtained by using the Power Estimator or XPOWER.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Military Grade.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to ensure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT} , V_{CCAUX} , and V_{CCO} power supplies shall each ramp on no faster than 200 μ s and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

Table 36 shows the minimum current required by QPro Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence.

If any V_{CCO} bank powers up before V_{CCAUX} , then each bank draws up to 300 mA, worst case, until the V_{CCAUX} powers on¹. This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power on reset threshold voltages.

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is essential. Consult Xilinx Application Note [XAPP623](#) for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion

are provided in Xilinx Answer Record 13756, available at www.support.xilinx.com.

Table 36: Maximum Power On Current Required for QPro Virtex-II Devices

| Current | Device (mA) | | |
|----------------|-------------|-----------|-----------|
| | XQR2V1000 | XQR2V3000 | XQR2V6000 |
| $I_{CCINTMAX}$ | 500 | 1300 | 1500 |
| $I_{CCAUXMAX}$ | 30 | 95 | 95 |
| I_{CCOMAX} | 6.25 | 6.25 | 6.25 |

Notes:

1. Values specified for power on current parameters are Military Grade.
2. I_{CCOMAX} values listed here apply to the entire device (all banks).

1. The 300 mA is transient current (peak). It eventually disappears even if V_{CCAUX} does not power up.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are cho-

sen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 37: DC Input and Output Levels

| Input/Output Standard | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|-----------------------|----------|------------------|------------------|-----------------|------------------|------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL ⁽¹⁾ | -0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | -24 |
| LVC MOS33 | -0.5 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCO} - 0.4$ | 24 | -24 |
| LVC MOS25 | -0.5 | 0.7 | 1.7 | 2.7 | 0.4 | $V_{CCO} - 0.4$ | 24 | -24 |
| LVC MOS18 | -0.5 | 35% V_{CCO} | 65% V_{CCO} | 1.95 | 0.4 | $V_{CCO} - 0.4$ | 16 | -16 |
| LVC MOS15 | -0.5 | 35% V_{CCO} | 65% V_{CCO} | 1.7 | 0.4 | $V_{CCO} - 0.4$ | 16 | -16 |
| PCI33_3 | -0.5 | 30% V_{CCO} | 50% V_{CCO} | $V_{CCO} + 0.5$ | 10% V_{CCO} | 90% V_{CCO} | Note 2 | Note 2 |
| PCI66_3 | -0.5 | 30% V_{CCO} | 50% V_{CCO} | $V_{CCO} + 0.5$ | 10% V_{CCO} | 90% V_{CCO} | Note 2 | Note 2 |
| PCI-X | -0.5 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 | Note 2 |
| GTLP | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.5$ | 0.6 | n/a | 36 | n/a |
| GTL | -0.5 | $V_{REF} - 0.05$ | $V_{REF} + 0.05$ | $V_{CCO} + 0.5$ | 0.4 | n/a | 40 | n/a |
| HSTL I | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.5$ | 0.4 | $V_{CCO} - 0.4$ | 8 | -8 |
| HSTL II | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.5$ | 0.4 | $V_{CCO} - 0.4$ | 16 | -16 |
| HSTL III | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.5$ | 0.4 | $V_{CCO} - 0.4$ | 24 | -8 |
| HSTL IV | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | $V_{CCO} + 0.5$ | 0.4 | $V_{CCO} - 0.4$ | 48 | -8 |
| SSTL3 I | -0.5 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{CCO} + 0.5$ | $V_{REF} - 0.6$ | $V_{REF} + 0.6$ | 8 | -8 |
| SSTL3 II | -0.5 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{CCO} + 0.5$ | $V_{REF} - 0.8$ | $V_{REF} + 0.8$ | 16 | -16 |
| SSTL2 I | -0.5 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCO} + 0.5$ | $V_{REF} - 0.65$ | $V_{REF} + 0.65$ | 7.6 | -7.6 |
| SSTL2 II | -0.5 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCO} + 0.5$ | $V_{REF} - 0.80$ | $V_{REF} + 0.80$ | 15.2 | -15.2 |
| AGP | -0.5 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{CCO} + 0.5$ | 10% V_{CCO} | 90% V_{CCO} | Note 2 | Note 2 |

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.
3. LVTTL and LVC MOS inputs have approximately 100 mV of hysteresis.

LDT Differential Signal DC Specifications (LDT_25)

Table 38: LDT DC Specifications

| DC Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-------------------------------|------------------|---|-----|-----|------|-------|
| Differential Output Voltage | V_{OD} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 500 | 600 | 700 | mV |
| Change in V_{OD} Magnitude | ΔV_{OD} | | -15 | | 15 | mV |
| Output Common Mode Voltage | V_{OCM} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 560 | 600 | 640 | mV |
| Change in V_{OS} Magnitude | ΔV_{OCM} | | -15 | | 15 | mV |
| Input Differential Voltage | V_{ID} | | 200 | 600 | 1000 | mV |
| Change in V_{ID} Magnitude | ΔV_{ID} | | -15 | | 15 | mV |
| Input Common Mode Voltage | V_{ICM} | | 500 | 600 | 700 | mV |
| Change in V_{ICM} Magnitude | ΔV_{ICM} | | -15 | | 15 | mV |

LVDS DC Specifications (LVDS_33 and LVDS_25)

Table 39: LVDS DC Specifications

| DC Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|-------------|---|-------|------------|-----------------|-------|
| Supply Voltage | V_{CCO} | | | 3.3 or 2.5 | | V |
| Output High Voltage for Q and \bar{Q} | V_{OH} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | | | 1.575 | V |
| Output Low Voltage for Q and \bar{Q} | V_{OL} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 0.925 | | | V |
| Differential Output Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | V_{ODIFF} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 250 | 350 | 400 | mV |
| Output Common-Mode Voltage | V_{OCM} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 1.125 | 1.2 | 1.375 | V |
| Differential Input Voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | V_{IDIFF} | Common-mode input voltage = 1.25 V | 100 | 350 | N/A | mV |
| Input Common-Mode Voltage | V_{ICM} | Differential input voltage = ± 350 mV | 0.2 | 1.25 | $V_{CCO} - 0.5$ | V |

Extended LVDS DC Specifications (LVDS_EXT_33 and LVDS_EXT_25)

Table 40: Extended LVDS DC Specifications

| DC Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|-------------|---|-------|------------|-----------------|-------|
| Supply Voltage | V_{CCO} | | | 3.3 or 2.5 | | V |
| Output High voltage for Q and \bar{Q} | V_{OH} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | | | 1.785 | V |
| Output Low voltage for Q and \bar{Q} | V_{OL} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 0.705 | | | V |
| Differential output voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | V_{ODIFF} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 440 | | 820 | mV |
| Output common-mode voltage | V_{OCM} | $R_T = 100 \Omega$ across Q and \bar{Q} signals | 1.125 | 1.200 | 1.375 | V |
| Differential input voltage (Q - \bar{Q}), Q = High ($\bar{Q} - Q$), \bar{Q} = High | V_{IDIFF} | Common-mode input voltage = 1.25 V | 100 | 350 | N/A | mV |
| Input common-mode voltage | V_{ICM} | Differential input voltage = ± 350 mV | 0.2 | 1.25 | $V_{CCO} - 0.5$ | V |

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower

common-mode ranges. [Table 41](#) summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 41: LVPECL DC Specifications

| DC Parameter | Min | Max | Min | Max | Min | Max | Units |
|----------------------------|------|-------|------|-------|------|-------|-------|
| V_{CCO} | 3.0 | | 3.3 | | 3.6 | | V |
| V_{OH} | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| V_{OL} | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| V_{IH} | 1.49 | 2.72 | 1.49 | 2.72 | 1.49 | 2.72 | V |
| V_{IL} | 0.86 | 2.125 | 0.86 | 2.125 | 0.86 | 2.125 | V |
| Differential Input Voltage | 0.3 | – | 0.3 | – | 0.3 | – | V |

QPro Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typ-

ically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 42](#) correlates the current status of each QPro Virtex-II device with a corresponding speed grade designation.

Table 42: QPro Virtex-II Device Speed Grade Designations

| Device | Speed Grade Designations | | |
|-----------|--------------------------|-------------|------------|
| | Advance | Preliminary | Production |
| XQR2V1000 | | | –4 |
| XQR2V3000 | | | –4 |
| XQR2V6000 | | | –4 |

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data,

use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all QPro Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with

the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 53.

Table 43: IOB Input Switching Characteristics

| Description | Symbol | Device | Min | Max | Units |
|---|----------------------------|-----------|------------|------|-------|
| Propagation Delays | | | | | |
| Pad to I output, no delay | T_{IOPI} | All | - | 0.88 | ns |
| Pad to I output, with delay | T_{IOPID} | XQR2V1000 | - | 2.43 | ns |
| | | XQR2V3000 | - | 2.49 | ns |
| | | XQR2V6000 | - | 2.66 | ns |
| Propagation Delays | | | | | |
| Pad to output IQ via transparent latch, no delay | T_{IOPLI} | All | - | 1.05 | ns |
| Pad to output IQ via transparent latch, with delay | T_{IOPLID} | XQR2V1000 | - | 4.09 | ns |
| | | XQR2V3000 | - | 4.20 | ns |
| | | XQR2V6000 | - | 4.55 | ns |
| Clock CLK to output IQ | T_{IOCKIQ} | All | - | 0.77 | ns |
| Setup and Hold Times with Respect to Clock at IOB Input Register | | | | | |
| Pad, no delay | T_{IOPICK}/T_{IOICKP} | All | 1.06/-0.45 | - | ns |
| Pad, with delay | $T_{IOPICKD}/T_{IOICKPD}$ | XQR2V1000 | 4.10/-2.58 | - | ns |
| | | XQR2V3000 | 4.22/-2.66 | - | ns |
| | | XQR2V6000 | 4.56/-2.90 | - | ns |
| ICE input | $T_{IOICECK}/T_{IOICKICE}$ | All | 0.24/ 0.04 | - | ns |
| SR input (IFF, synchronous) | $T_{IOSRCKI}$ | All | 0.34 | - | ns |
| Set/Reset Delays | | | | | |
| SR input to IQ (asynchronous) | T_{IOSRIQ} | All | | 1.40 | ns |
| GSR to output IQ | T_{GSRQ} | All | | 6.88 | ns |

Notes:

- Input timing for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 47](#).

IOB Input Switching Characteristics Standard Adjustments

Table 44: IOB Input Switching Characteristics Standard Adjustments

| Description | Symbol | Standard | Value | Units |
|--|-----------------------|-----------------------|-------|-------|
| Data Input Delay Adjustments | | | | |
| Standard-specific data input delay adjustments | T_{ILVTTL} | LVTTL | 0.00 | ns |
| | $T_{ILVCMOS33}$ | LVCMOS33 | 0.00 | ns |
| | $T_{ILVCMOS25}$ | LVCMOS25 | 0.12 | ns |
| | $T_{ILVCMOS18}$ | LVCMOS18 | 0.49 | ns |
| | $T_{ILVCMOS15}$ | LVCMOS15 | 1.15 | ns |
| | T_{ILVDS_25} | LVDS_25 | 0.69 | ns |
| | T_{ILVDS_33} | LVDS_33 | 0.69 | ns |
| | $T_{ILVPECL_33}$ | LVPECL | 0.69 | ns |
| | T_{IPCI33_3} | PCI, 33 MHz, 3.3 V | 0.00 | ns |
| | T_{IPCI66_3} | PCI, 66 MHz, 3.3 V | 0.00 | ns |
| | T_{IPCIX} | PCI-X, 133 MHz, 3.3 V | 0.00 | ns |
| | T_{IGTL} | GTL | 0.48 | ns |
| | T_{IGTLP} | GTLP | 0.48 | ns |
| | T_{IHSTL_I} | HSTL I | 0.48 | ns |
| | T_{IHSTL_II} | HSTL II | 0.48 | ns |
| | T_{IHSTL_III} | HSTL III | 0.48 | ns |
| | T_{IHSTL_IV} | HSTL IV | 0.48 | ns |
| | $T_{IHSTL_I_18}$ | HSTL I_18 | 0.48 | ns |
| | $T_{IHSTL_II_18}$ | HSTL II_18 | 0.48 | ns |
| | $T_{IHSTL_III_18}$ | HSTL III_18 | 0.48 | ns |
| | $T_{IHSTL_IV_18}$ | HSTL IV_18 | 0.48 | ns |
| | T_{ISSTL2_I} | SSTL2 I | 0.48 | ns |
| | T_{ISSTL2_II} | SSTL2 II | 0.48 | ns |
| | T_{ISSTL3_I} | SSTL3 I | 0.40 | ns |
| | T_{ISSTL3_II} | SSTL3 II | 0.40 | ns |
| | T_{IAGP} | AGP | 0.40 | ns |
| | T_{ILVDCI_33} | LVDCI_33 | 0.00 | ns |
| | T_{ILVDCI_25} | LVDCI_25 | 0.12 | ns |
| | T_{ILVDCI_18} | LVDCI_18 | 0.49 | ns |
| | T_{ILVDCI_15} | LVDCI_15 | 1.14 | ns |
| | $T_{ILVDCI_DV2_33}$ | LVDCI_DV2_33 | 0.00 | ns |
| | $T_{ILVDCI_DV2_25}$ | LVDCI_DV2_25 | 0.12 | ns |
| | $T_{ILVDCI_DV2_18}$ | LVDCI_DV2_18 | 0.49 | ns |

Table 44: IOB Input Switching Characteristics Standard Adjustments (Continued)

| Description | Symbol | Standard | Value | Units |
|--|---------------------------|-----------------|-------|-------|
| Standard-specific data input delay adjustments | $T_{ILVDCI_DV2_15}$ | LVDCI_DV2_15 | 1.14 | ns |
| | T_{IGTL_DCI} | GTL_DCI | 0.48 | ns |
| | T_{IGTLP_DCI} | GTL_P_DCI | 0.48 | ns |
| | $T_{IHSTL_I_DCI}$ | HSTL_I_DCI | 0.48 | ns |
| | $T_{IHSTL_II_DCI}$ | HSTL_II_DCI | 0.48 | ns |
| | $T_{IHSTL_III_DCI}$ | HSTL_III_DCI | 0.48 | ns |
| | $T_{IHSTL_IV_DCI}$ | HSTL_IV_DCI | 0.48 | ns |
| | $T_{IHSTL_I_DCI_18}$ | HSTL_I_DCI_18 | 0.48 | ns |
| | $T_{IHSTL_II_DCI_18}$ | HSTL_II_DCI_18 | 0.48 | ns |
| | $T_{IHSTL_III_DCI_18}$ | HSTL_III_DCI_18 | 0.48 | ns |
| | $T_{IHSTL_IV_DCI_18}$ | HSTL_IV_DCI_18 | 0.48 | ns |
| | $T_{ISSTL2_I_DCI}$ | SSTL2_I_DCI | 0.48 | ns |
| | $T_{ISSTL2_II_DCI}$ | SSTL2_II_DCI | 0.48 | ns |
| | $T_{ISSTL3_I_DCI}$ | SSTL3_I_DCI | 0.40 | ns |
| | $T_{ISSTL3_II_DCI}$ | SSTL3_II_DCI | 0.40 | ns |
| | $T_{ILD T_25}$ | LDT_25 | 0.56 | ns |
| | T_{IULVDS_25} | ULVDS_25 | 0.56 | ns |

Notes:

1. Input timing for LVTTTL is measured at 1.4 V. For other I/O standards, see [Table 47](#).

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 56.

Table 45: IOB Output Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|---------------------------|------------|------|-------|
| Propagation Delays | | | | |
| O input to Pad | T_{IOOP} | | 1.74 | ns |
| O input to Pad via transparent latch | T_{IOOLP} | | 2.11 | ns |
| 3-State Delays | | | | |
| T input to Pad high-impedance ⁽¹⁾ | T_{IOTHZ} | | 0.64 | ns |
| T input to valid data on Pad | T_{IOTON} | | 1.67 | ns |
| T input to Pad high-impedance via transparent latch ⁽¹⁾ | $T_{IOTLPHZ}$ | | 1.01 | ns |
| T input to valid data on Pad via transparent latch | $T_{IOTLPON}$ | | 2.04 | ns |
| GTS to Pad high-impedance ⁽¹⁾ | T_{GTS} | | 5.98 | ns |
| Sequential Delays | | | | |
| Clock CLK to Pad | T_{IOCKP} | | 2.15 | ns |
| Clock CLK to Pad high-impedance (synchronous) ⁽¹⁾ | T_{IOCKHZ} | | 1.20 | ns |
| Clock CLK to valid data on Pad (synchronous) | T_{IOCKON} | | 2.22 | ns |
| Setup and Hold Times Before/After Clock CLK | | | | |
| O input | T_{IOOCK}/T_{IOCKO} | 0.39/-0.11 | | ns |
| OCE input | $T_{IOOCECK}/T_{IOCKOCE}$ | 0.24/-0.08 | | ns |
| SR input (OFF) | $T_{IOSRCKO}/T_{IOCKOSR}$ | 0.34/-0.07 | | ns |
| 3-State Setup Times, T input | T_{IOTCK}/T_{IOCKT} | 0.35/-0.08 | | ns |
| 3-State Setup Times, TCE input | $T_{IOTCECK}/T_{IOCKTCE}$ | 0.24/-0.08 | | ns |
| 3-State Setup Times, SR input (TFF) | $T_{IOSRCKT}/T_{IOCKTSR}$ | 0.34/-0.07 | | ns |
| Set/Reset Delays | | | | |
| SR input to Pad (asynchronous) | T_{IOSRP} | | 2.98 | ns |
| SR input to Pad high-impedance (asynchronous) ⁽¹⁾ | T_{IOSRHZ} | | 1.92 | ns |
| SR input to valid data on Pad (asynchronous) | T_{IOSRON} | | 2.95 | ns |
| GSR to Pad | T_{IOGSRQ} | | 6.88 | ns |

Notes:

- The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 46: IOB Output Switching Characteristics Standard Adjustments

| Description | Symbol | Standard | Value | Units |
|--|--------------------------|-----------------------|-------|-------|
| Output Delay Adjustments | | | | |
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | T _{OLVTTTL_S2} | LVTTTL, Slow, 2 mA | 10.68 | ns |
| | T _{OLVTTTL_S4} | 4 mA | 6.55 | ns |
| | T _{OLVTTTL_S6} | 6 mA | 4.66 | ns |
| | T _{OLVTTTL_S8} | 8 mA | 3.26 | ns |
| | T _{OLVTTTL_S12} | 12 mA | 2.63 | ns |
| | T _{OLVTTTL_S16} | 16 mA | 1.93 | ns |
| | T _{OLVTTTL_S24} | 24 mA | 1.43 | ns |
| | T _{OLVTTTL_F2} | LVTTTL, Fast, 2 mA | 7.39 | ns |
| | T _{OLVTTTL_F4} | 4 mA | 3.17 | ns |
| | T _{OLVTTTL_F6} | 6 mA | 1.78 | ns |
| | T _{OLVTTTL_F8} | 8 mA | 0.52 | ns |
| | T _{OLVTTTL_F12} | 12 mA | 0.00 | ns |
| | T _{OLVTTTL_F16} | 16 mA | -0.15 | ns |
| | T _{OLVTTTL_F24} | 24 mA | -0.26 | ns |
| | T _{OLVDS_25} | LVDS | -0.36 | ns |
| | T _{OLVDS_33} | LVDS | -0.29 | ns |
| | T _{OLVDSEXT_25} | LVDS | -0.21 | ns |
| | T _{OLVDSEXT_33} | LVDS | -0.19 | ns |
| | T _{OLDT_25} | LDT | -0.23 | ns |
| | T _{OBLVDS_25} | BLVDS | 0.76 | ns |
| | T _{OULVDS_25} | ULVDS | -0.23 | ns |
| | T _{OLVPECL_33} | LVPECL | 0.33 | ns |
| | T _{OPCI33_3} | PCI, 33 MHz, 3.3 V | 1.31 | ns |
| | T _{OPCI66_3} | PCI, 66 MHz, 3.3 V | -0.01 | ns |
| | T _{OPCIX} | PCI-X, 133 MHz, 3.3 V | -0.01 | ns |
| | T _{OGTL} | GTL | -0.36 | ns |
| | T _{OGTLP} | GTLP | -0.20 | ns |
| | T _{OHSTL_I} | HSTL I | 0.29 | ns |
| | T _{OHSTL_II} | HSTL II | -0.17 | ns |
| | T _{OHSTL_III} | HSTL III | -0.19 | ns |
| | T _{OHSTL_IV} | HSTL IV | -0.45 | ns |
| | T _{OHSTL_I_18} | HSTL I_18 | -0.04 | ns |
| T _{OHSTL_II_18} | HSTL II_18 | -0.20 | ns | |
| T _{OHSTL_III_18} | HSTL III_18 | -0.18 | ns | |

Table 46: IOB Output Switching Characteristics Standard Adjustments (Continued)

| Description | Symbol | Standard | Value | Units |
|--|----------------------|-----------------------|-------|-------|
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | $T_{OHSTL_IV_18}$ | HSTL IV_18 | -0.44 | ns |
| | T_{OSSTL2_I} | SSTL2 I | 0.24 | ns |
| | T_{OSSTL2_II} | SSTL2 II | -0.18 | ns |
| | T_{OSSTL3_I} | SSTL3 I | 0.33 | ns |
| | T_{OSSTL3_II} | SSTL3 II | -0.05 | ns |
| | T_{OAGP} | AGP | -0.31 | ns |
| | $T_{OLVCMOS33_S2}$ | LVC MOS33, Slow, 2 mA | 8.70 | ns |
| | $T_{OLVCMOS33_S4}$ | 4 mA | 4.95 | ns |
| | $T_{OLVCMOS33_S6}$ | 6 mA | 3.78 | ns |
| | $T_{OLVCMOS33_S8}$ | 8 mA | 2.60 | ns |
| | $T_{OLVCMOS33_S12}$ | 12 mA | 2.16 | ns |
| | $T_{OLVCMOS33_S16}$ | 16 mA | 1.40 | ns |
| | $T_{OLVCMOS33_S24}$ | 24 mA | 1.34 | ns |
| | $T_{OLVCMOS33_F2}$ | LVC MOS33, Fast, 2 mA | 6.60 | ns |
| | $T_{OLVCMOS33_F4}$ | 4 mA | 2.81 | ns |
| | $T_{OLVCMOS33_F6}$ | 6 mA | 1.45 | ns |
| | $T_{OLVCMOS33_F8}$ | 8 mA | 0.54 | ns |
| | $T_{OLVCMOS33_F12}$ | 12 mA | 0.31 | ns |
| | $T_{OLVCMOS33_F16}$ | 16 mA | -0.15 | ns |
| | $T_{OLVCMOS33_F24}$ | 24 mA | -0.23 | ns |
| | $T_{OLVCMOS25_S2}$ | LVC MOS25, Slow, 2 mA | 10.33 | ns |
| | $T_{OLVCMOS25_S4}$ | 4 mA | 5.67 | ns |
| | $T_{OLVCMOS25_S6}$ | 6 mA | 5.13 | ns |
| | $T_{OLVCMOS25_S8}$ | 8 mA | 4.38 | ns |
| | $T_{OLVCMOS25_S12}$ | 12 mA | 3.22 | ns |
| | $T_{OLVCMOS25_S16}$ | 16 mA | 2.67 | ns |
| | $T_{OLVCMOS25_S24}$ | 24 mA | 2.27 | ns |
| | $T_{OLVCMOS25_F2}$ | LVC MOS25, Fast, 2 mA | 4.60 | ns |
| | $T_{OLVCMOS25_F4}$ | 4 mA | 1.30 | ns |
| | $T_{OLVCMOS25_F6}$ | 6 mA | 0.81 | ns |
| | $T_{OLVCMOS25_F8}$ | 8 mA | 0.37 | ns |
| | $T_{OLVCMOS25_F12}$ | 12 mA | 0.03 | ns |
| | $T_{OLVCMOS25_F16}$ | 16 mA | -0.21 | ns |
| | $T_{OLVCMOS25_F24}$ | 24 mA | -0.40 | ns |
| | $T_{OLVCMOS18_S2}$ | LVC MOS18, Slow, 2 mA | 17.71 | ns |
| | $T_{OLVCMOS18_S4}$ | 4 mA | 11.57 | ns |
| | $T_{OLVCMOS18_S6}$ | 6 mA | 8.53 | ns |
| | $T_{OLVCMOS18_S8}$ | 8 mA | 7.78 | ns |

Table 46: IOB Output Switching Characteristics Standard Adjustments (Continued)

| Description | Symbol | Standard | Value | Units |
|--|-------------------------------|-----------------------|-------|-------|
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | T _{OLVCMOS18_S12} | 12 mA | 6.28 | ns |
| | T _{OLVCMOS18_S16} | 16 mA | 6.02 | ns |
| | T _{OLVCMOS18_F2} | LVC MOS18, Fast, 2 mA | 6.30 | ns |
| | T _{OLVCMOS18_F4} | 4 mA | 2.15 | ns |
| | T _{OLVCMOS18_F6} | 6 mA | 0.94 | ns |
| | T _{OLVCMOS18_F8} | 8 mA | 0.80 | ns |
| | T _{OLVCMOS18_F12} | 12 mA | 0.30 | ns |
| | T _{OLVCMOS18_F16} | 16 mA | 0.26 | ns |
| | T _{OLVCMOS15_S2} | LVC MOS15, Slow, 2 mA | 21.50 | ns |
| | T _{OLVCMOS15_S4} | 4 mA | 14.48 | ns |
| | T _{OLVCMOS15_S6} | 6 mA | 13.66 | ns |
| | T _{OLVCMOS15_S8} | 8 mA | 11.06 | ns |
| | T _{OLVCMOS15_S12} | 12 mA | 10.25 | ns |
| | T _{OLVCMOS15_S16} | 16 mA | 9.31 | ns |
| | T _{OLVCMOS15_F2} | LVC MOS15, Fast, 2 mA | 5.78 | ns |
| | T _{OLVCMOS15_F4} | 4 mA | 2.27 | ns |
| | T _{OLVCMOS15_F6} | 6 mA | 1.66 | ns |
| | T _{OLVCMOS15_F8} | 8 mA | 1.05 | ns |
| | T _{OLVCMOS15_F12} | 12 mA | 0.84 | ns |
| | T _{OLVCMOS15_F16} | 16 mA | 0.75 | ns |
| | T _{OLVDCI_33} | LVDCI_33 | 0.84 | ns |
| | T _{OLVDCI_25} | LVDCI_25 | 0.88 | ns |
| | T _{OLVDCI_18} | LVDCI_18 | 0.95 | ns |
| | T _{OLVDCI_15} | LVDCI_15 | 2.06 | ns |
| | T _{OLVDCI_DV2_33} | LVDCI_DV2_33 | 0.13 | ns |
| | T _{OLVDCI_DV2_25} | LVDCI_DV2_25 | 0.03 | ns |
| | T _{OLVDCI_DV2_18} | LVDCI_DV2_18 | 0.48 | ns |
| | T _{OLVDCI_DV2_15} | LVDCI_DV2_15 | 1.36 | ns |
| | T _{OGTL_DCI} | GTL_DCI | -0.35 | ns |
| | T _{OGTLP_DCI} | GTL_P_DCI | -0.17 | ns |
| | T _{OHSTL_I_DCI} | HSTL_I_DCI | 0.26 | ns |
| | T _{OHSTL_II_DCI} | HSTL_II_DCI | 0.07 | ns |
| | T _{OHSTL_III_DCI} | HSTL_III_DCI | -0.20 | ns |
| | T _{OHSTL_IV_DCI} | HSTL_IV_DCI | -0.52 | ns |
| | T _{OHSTL_I_DCI_18} | HSTL_I_DCI_18 | 0.06 | ns |
| | T _{OHSTL_II_DCI_18} | HSTL_II_DCI_18 | -0.03 | ns |
| | T _{OHSTL_III_DCI_18} | HSTL_III_DCI_18 | -0.16 | ns |
| | T _{OHSTL_IV_DCI_18} | HSTL_IV_DCI_18 | -0.47 | ns |

Table 46: IOB Output Switching Characteristics Standard Adjustments (Continued)

| Description | Symbol | Standard | Value | Units |
|--|-----------------------|--------------|-------|-------|
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | $T_{OSSTL2_I_DCI}$ | SSTL2_I_DCI | 0.14 | ns |
| | $T_{OSSTL2_II_DCI}$ | SSTL2_II_DCI | -0.11 | ns |
| | $T_{OSSTL3_I_DCI}$ | SSTL3_I_DCI | 0.17 | ns |
| | $T_{OSSTL3_II_DCI}$ | SSTL3_II_DCI | 0.09 | ns |

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring Input standard adjustments (see Table 44, page 53).

Table 47: Input Delay Measurement Methodology

| Standard | $V_L^{(1)}$ | $V_H^{(1)}$ | $V_{MEAS}^{(3,4)}$ | $V_{REF}^{(2,4)}$ |
|--------------------|----------------------------------|----------------------------------|--------------------|-------------------|
| LVTTTL | 0 | 3.0 | 1.4 | – |
| LVCOS33 | 0 | 3.3 | 1.65 | – |
| LVCOS25 | 0 | 2.5 | 1.25 | – |
| LVCOS18 | 0 | 1.8 | 0.9 | – |
| LVCOS15 | 0 | 1.5 | 0.75 | – |
| PCI33_3 | Per PCI Specification | | | – |
| PCI66_3 | Per PCI Specification | | | – |
| PCI-X | Per PCI-X Specification | | | – |
| GTL | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | V_{REF} | 0.80 |
| GTL P | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | V_{REF} | 1.0 |
| HSTL Class I | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.75 |
| HSTL Class II | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.75 |
| HSTL Class III | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| HSTL Class IV | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| SSTL3 Class I & II | $V_{REF} - 1.00$ | $V_{REF} + 1.00$ | V_{REF} | 1.5 |
| SSTL2 Class I & II | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | V_{REF} | 1.25 |
| AGP-2X | $V_{REF} - (0.2 \times V_{CC0})$ | $V_{REF} + (0.2 \times V_{CC0})$ | V_{REF} | Per AGP Spec |
| LVDS25 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDS33 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDS25EXT | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| LVDS25EXT33 | 1.2 – 0.125 | 1.2 + 0.125 | 1.2 | |
| ULVDS25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LDT25 | 0.6 – 0.125 | 0.6 + 0.125 | 0.6 | |
| LVPECL | 1.6 – 0.3 | 1.6 + 0.3 | 1.6 | |

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See [Virtex-II Platform FPGA User Guide](#) for min/max specifications.
- Input voltage level from which measurement starts.
- Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 51.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pf) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See [Virtex-II Platform FPGA User Guide](#) for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 51.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at http://support.xilinx.com/support/sw_ibis.htm.) Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 46) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

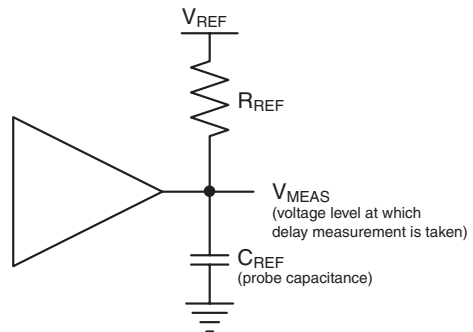


Figure 51: Generalized Test Setup

Table 48: Output Delay Measurement Methodology

| Standard | R _{REF} (ohms) | C _{REF} ⁽¹⁾ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|------------------------|----------------------------|---|--------------------------|-------------------------|
| LVTTTL (all) | 1M | 0 | 1.4 | 0 |
| LVCOS33 | 1M | 0 | 1.65 | 0 |
| LVCOS25 | 1M | 0 | 1.25 | 0 |
| LVCOS18 | 1M | 0 | 0.9 | 0 |
| LVCOS15 | 1M | 0 | 0.75 | 0 |
| PCI33_3 - rising edge | 25 | 0 | 0.94 | 0 |
| PCI33_3 - falling edge | 25 | 0 | 2.03 | 3.3 |
| PCI66_3 - rising edge | 25 | 0 | 0.94 | 0 |
| PCI66_3 - falling edge | 25 | 0 | 2.03 | 3.3 |
| PCI-X - rising edge | 25 | 0 | 0.94 | |
| PCI-X - falling edge | 25 | 0 | 2.03 | 3.3 |
| GTL | 25 | 0 | 0.8 | 1.2 |
| GTL P | 25 | 0 | 1.0 | 1.5 |
| HSTL Class I | 50 | 0 | V _{REF} | 0.75 |
| HSTL Class II | 25 | 0 | V _{REF} | 0.75 |
| HSTL Class III | 50 | 0 | 0.9 | 1.5 |
| HSTL Class IV | 25 | 0 | 0.9 | 1.5 |
| HSTL18 Class I | 50 | 0 | V _{REF} | 0.9 |
| HSTL18 Class II | 25 | 0 | V _{REF} | 0.9 |
| HSTL18 Class III | 50 | 0 | 1.1 | 1.8 |
| HSTL18 Class IV | 25 | 0 | 1.1 | 1.8 |
| SSTL3 Class I | 50 | 0 | V _{REF} | 1.5 |
| SSTL3 Class II | 25 | 0 | V _{REF} | 1.5 |
| SSTL2 Class I | 50 | 0 | V _{REF} | 1.25 |
| SSTL2 Class II | 25 | 0 | V _{REF} | 1.25 |
| SSTL18 Class I | 50 | 0 | V _{REF} | 0.9 |
| SSTL18 Class II | 25 | 0 | V _{REF} | 0.9 |
| AGP-2X - rising edge | 50 | 0 | 0.94 | 0 |
| AGP-2X - falling edge | 50 | 0 | 2.03 | 3.3 |

Table 48: Output Delay Measurement Methodology

| Standard | R _{REF} (ohms) | C _{REF} ⁽¹⁾ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|----------------------|----------------------------|---|--------------------------|-------------------------|
| LVDS25 | 50 | 0 | V _{REF} | 1.2 |
| LVDS25EXT25 | 50 | 0 | V _{REF} | 1.2 |
| LVDS33 | 50 | 0 | V _{REF} | 1.2 |
| LVDS25EXT33 | 50 | 0 | V _{REF} | 1.2 |
| BLVDS | 1M | 0 | 1.2 | 0 |
| LDT_25 | 50 | 0 | V _{REF} | 0.6 |
| LVPECL25 | 1M | 0 | 1.23 | 0 |
| LVDCI33 | 1M | 0 | 1.65 | 0 |
| LVDCI25 | 1M | 0 | 1.25 | 0 |
| LVDCI18 | 1M | 0 | 0.9 | 0 |
| LVDCI15 | 1M | 0 | 0.75 | 0 |
| HSTL DCI Class I | 50 | 0 | V _{REF} | 0.75 |
| HSTL DCI Class II | 50 | 0 | V _{REF} | 0.75 |
| HSTL DCI Class III | 50 | 0 | 0.9 | 1.5 |
| HSTL DCI Class IV | 50 | 0 | 0.9 | 1.5 |
| HSTL18 DCI Class I | 50 | 0 | V _{REF} | 0.9 |
| HSTL18 DCI Class II | 50 | 0 | V _{REF} | 0.9 |
| HSTL18 DCI Class III | 50 | 0 | 1.1 | 1.8 |
| HSTL18 DCI Class IV | 50 | 0 | 1.1 | 1.8 |
| SSTL3 DCI Class I | 50 | 0 | V _{REF} | 1.5 |
| SSTL3 DCI Class II | 50 | 0 | V _{REF} | 1.5 |
| SSTL2 DCI Class I | 50 | 0 | V _{REF} | 1.25 |
| SSTL2 DCI Class II | 50 | 0 | V _{REF} | 1.25 |
| SSTL18 DCI Class I | 50 | 0 | V _{REF} | 0.9 |
| SSTL18 DCI Class II | 50 | 0 | V _{REF} | 0.9 |
| GTL DCI | 50 | 0 | 0.8 | 1.2 |
| GTL P DCI | 50 | 0 | 1.0 | 1.5 |

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.

Clock Distribution Switching Characteristics

Table 49: Clock Distribution Switching Characteristics

| Description | Symbol | Value | Units |
|---|-----------|-------|-------|
| Global Clock Buffer I input to O output | T_{GIO} | 0.59 | ns |

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 50). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 50: CLB Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|---------------------|------------|------|-------|
| Combinatorial Delays | | | | |
| 4-input function: F/G inputs to X/Y outputs | T_{ILO} | - | 0.44 | ns |
| 5-input function: F/G inputs to F5 output | T_{IF5} | - | 0.72 | ns |
| 5-input function: F/G inputs to X output | T_{IF5X} | - | 0.95 | ns |
| FXINA or FXINB inputs to Y output via MUXFX | T_{IFXY} | - | 0.45 | ns |
| FXINA input to FX output via MUXFX | T_{INAFX} | - | 0.32 | ns |
| FXINB input to FX output via MUXFX | T_{INBFX} | - | 0.32 | ns |
| SOPIN input to SOPOUT output via ORCY | T_{SOPSOP} | - | 0.44 | ns |
| Incremental delay routing through transparent latch to XQ/YQ outputs | T_{IFNCTL} | - | 0.51 | ns |
| Sequential Delays | | | | |
| FF Clock CLK to XQ/YQ outputs | T_{CKO} | - | 0.57 | ns |
| Latch Clock CLK to XQ/YQ outputs | T_{CKLO} | - | 0.68 | ns |
| Setup and Hold Times Before/After Clock CLK | | | | |
| BX/BY inputs | T_{DICK}/T_{CKDI} | 0.37/-0.09 | - | ns |
| DY inputs | T_{DYCK}/T_{CKDY} | 0.37/-0.09 | - | ns |
| DX inputs | T_{DXQK}/T_{CKDX} | 0.37/-0.09 | - | ns |
| CE input | T_{CECK}/T_{CKCE} | 0.24/-0.08 | - | ns |
| SR/BY inputs (synchronous) | T_{SRCK}/T_{SCKR} | 0.26/-0.03 | - | ns |
| Clock CLK | | | | |
| Minimum Pulse Width, High | T_{CH} | 0.77 | - | ns |
| Minimum Pulse Width, Low | T_{CL} | 0.77 | - | ns |
| Set/Reset | | | | |
| Minimum Pulse Width, SR/BY inputs | T_{RPW} | 0.77 | - | ns |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | T_{RQ} | - | 1.34 | ns |
| Toggle Frequency (MHz) (for export control) | F_{TOG} | - | 650 | MHz |

CLB Distributed RAM Switching Characteristics

Table 51: CLB Distributed RAM Switching Characteristics

| Description | Symbol | Min | Max | Units |
|---|-------------------|------------|------|-------|
| Sequential Delays | | | | |
| Clock CLK to X/Y outputs (WE active) in 16 x 1 mode | $T_{SHCKO16}$ | - | 2.05 | ns |
| Clock CLK to X/Y outputs (WE active) in 32 x 1 mode | $T_{SHCKO32}$ | - | 2.49 | ns |
| Clock CLK to F5 output | $T_{SHCKOF5}$ | - | 2.23 | ns |
| Setup and Hold Times Before/After Clock CLK | | | | |
| BX/BY data inputs (DIN) | T_{DS}/T_{DH} | 0.67/-0.11 | - | ns |
| F/G address inputs | T_{AS}/T_{AH} | 0.50/ 0.00 | - | ns |
| SR input (WS) | T_{WES}/T_{WEH} | 0.53/-0.01 | - | ns |
| Clock CLK | | | | |
| Minimum Pulse Width, High | T_{WPH} | 0.72 | - | ns |
| Minimum Pulse Width, Low | T_{WPL} | 0.72 | - | ns |
| Minimum clock period to meet address write cycle time | T_{WC} | 1.44 | - | ns |

CLB Shift Register Switching Characteristics

Table 52: CLB Shift Register Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|-----------------------|------------|------|-------|
| Sequential Delays | | | | |
| Clock CLK to X/Y outputs | T_{REG} | - | 2.92 | ns |
| Clock CLK to X/Y outputs | T_{REG32} | - | 3.35 | ns |
| Clock CLK to XB output via MC15 LUT output | T_{REGXB} | - | 2.82 | ns |
| Clock CLK to YB output via MC15 LUT output | T_{REGYB} | - | 2.75 | ns |
| Clock CLK to Shiftout | T_{CKSH} | - | 2.43 | ns |
| Clock CLK to F5 output | T_{REGF5} | - | 3.09 | ns |
| Setup and Hold Times Before/After Clock CLK | | | | |
| BX/BY data inputs (DIN) | T_{SRLDS}/T_{SRLDH} | 0.67/-0.09 | - | ns |
| SR input (WS) | T_{WSS}/T_{WSH} | 0.24/-0.08 | - | ns |
| Clock CLK | | | | |
| Minimum Pulse Width, High | T_{SRPH} | 0.72 | - | ns |
| Minimum Pulse Width, Low | T_{SRPL} | 0.72 | - | ns |

Multiplier Switching Characteristics

Table 53 and Table 54 provide timing information for QPro Virtex-II multiplier blocks, available in stepping revisions of QPro Virtex-II devices. For more information on stepping revisions, availability, and ordering instructions, see your local sales representative.

Table 53: Enhanced Multiplier Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|-----------------|-----|------|-------|
| Propagation Delay to Output Pin | | | | |
| Input to Pin 35 | T_{MULT_P35} | - | 5.91 | ns |
| Input to Pin 34 | T_{MULT_P34} | - | 5.79 | ns |
| Input to Pin 33 | T_{MULT_P33} | - | 5.66 | ns |
| Input to Pin 32 | T_{MULT_P32} | - | 5.54 | ns |
| Input to Pin 31 | T_{MULT_P31} | - | 5.42 | ns |
| Input to Pin 30 | T_{MULT_P30} | - | 5.29 | ns |
| Input to Pin 29 | T_{MULT_P29} | - | 5.17 | ns |
| Input to Pin 28 | T_{MULT_P28} | - | 5.05 | ns |
| Input to Pin 27 | T_{MULT_P27} | - | 4.92 | ns |
| Input to Pin 26 | T_{MULT_P26} | - | 4.80 | ns |
| Input to Pin 25 | T_{MULT_P25} | - | 4.68 | ns |
| Input to Pin 24 | T_{MULT_P24} | - | 4.56 | ns |
| Input to Pin 23 | T_{MULT_P23} | - | 4.43 | ns |
| Input to Pin 22 | T_{MULT_P22} | - | 4.31 | ns |
| Input to Pin 21 | T_{MULT_P21} | - | 4.19 | ns |
| Input to Pin 20 | T_{MULT_P20} | - | 4.06 | ns |
| Input to Pin 19 | T_{MULT_P19} | - | 3.94 | ns |
| Input to Pin 18 | T_{MULT_P18} | - | 3.82 | ns |
| Input to Pin 17 | T_{MULT_P17} | - | 3.69 | ns |
| Input to Pin 16 | T_{MULT_P16} | - | 3.57 | ns |
| Input to Pin 15 | T_{MULT_P15} | - | 3.45 | ns |
| Input to Pin 14 | T_{MULT_P14} | - | 3.33 | ns |
| Input to Pin 13 | T_{MULT_P13} | - | 3.20 | ns |
| Input to Pin 12 | T_{MULT_P12} | - | 3.08 | ns |
| Input to Pin 11 | T_{MULT_P11} | - | 2.96 | ns |
| Input to Pin 10 | T_{MULT_P10} | - | 2.83 | ns |
| Input to Pin 9 | T_{MULT_P9} | - | 2.71 | ns |
| Input to Pin 8 | T_{MULT_P8} | - | 2.59 | ns |
| Input to Pin 7 | T_{MULT_P7} | - | 2.46 | ns |
| Input to Pin 6 | T_{MULT_P6} | - | 2.34 | ns |
| Input to Pin 5 | T_{MULT_P5} | - | 2.22 | ns |
| Input to Pin 4 | T_{MULT_P4} | - | 2.10 | ns |
| Input to Pin 3 | T_{MULT_P3} | - | 1.97 | ns |
| Input to Pin 2 | T_{MULT_P2} | - | 1.85 | ns |
| Input to Pin 1 | T_{MULT_P1} | - | 1.73 | ns |
| Input to Pin 0 | T_{MULT_P0} | - | 1.60 | ns |

Table 54: Pipelined Multiplier Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|-------------------------------------|-----|-----------|-------|
| Setup and Hold Times Before/After Clock | | | | |
| Data Inputs | $T_{MULIDCK}/T_{MULCKID}$ | - | 3.89/0.00 | ns |
| Clock Enable | $T_{MULIDCK_CE}/T_{MULCKID_CE}$ | - | 0.86/0.00 | ns |
| Reset | $T_{MULIDCK_RST}/T_{MULCKID_RST}$ | - | 0.86/0.00 | ns |
| Clock to Output Pin | | | | |
| Clock to Pin 35 | T_{MULTCK_P35} | - | 3.74 | ns |
| Clock to Pin 34 | T_{MULTCK_P34} | - | 3.61 | ns |
| Clock to Pin 33 | T_{MULTCK_P33} | - | 3.49 | ns |
| Clock to Pin 32 | T_{MULTCK_P32} | - | 3.37 | ns |
| Clock to Pin 31 | T_{MULTCK_P31} | - | 3.25 | ns |
| Clock to Pin 30 | T_{MULTCK_P30} | - | 3.12 | ns |
| Clock to Pin 29 | T_{MULTCK_P29} | - | 3.00 | ns |
| Clock to Pin 28 | T_{MULTCK_P28} | - | 2.88 | ns |
| Clock to Pin 27 | T_{MULTCK_P27} | - | 2.75 | ns |
| Clock to Pin 26 | T_{MULTCK_P26} | - | 2.63 | ns |
| Clock to Pin 25 | T_{MULTCK_P25} | - | 2.51 | ns |
| Clock to Pin 24 | T_{MULTCK_P24} | - | 2.38 | ns |
| Clock to Pin 23 | T_{MULTCK_P23} | - | 2.26 | ns |
| Clock to Pin 22 | T_{MULTCK_P22} | - | 2.14 | ns |
| Clock to Pin 21 | T_{MULTCK_P21} | - | 2.02 | ns |
| Clock to Pin 20 | T_{MULTCK_P20} | - | 1.89 | ns |
| Clock to Pin 19 | T_{MULTCK_P19} | - | 1.77 | ns |
| Clock to Pin 18 | T_{MULTCK_P18} | - | 1.65 | ns |
| Clock to Pin 17 | T_{MULTCK_P17} | - | 1.52 | ns |
| Clock to Pin 16 | T_{MULTCK_P16} | - | 1.40 | ns |
| Clock to Pin 15 | T_{MULTCK_P15} | - | 1.28 | ns |
| Clock to Pin 14 | T_{MULTCK_P14} | - | 1.15 | ns |
| Clock to Pin 13 | T_{MULTCK_P13} | - | 1.15 | ns |
| Clock to Pin 12 | T_{MULTCK_P12} | - | 1.15 | ns |
| Clock to Pin 11 | T_{MULTCK_P11} | - | 1.15 | ns |
| Clock to Pin 10 | T_{MULTCK_P10} | - | 1.15 | ns |
| Clock to Pin 9 | T_{MULTCK_P9} | - | 1.15 | ns |
| Clock to Pin 8 | T_{MULTCK_P8} | - | 1.15 | ns |
| Clock to Pin 7 | T_{MULTCK_P7} | - | 1.15 | ns |
| Clock to Pin 6 | T_{MULTCK_P6} | - | 1.15 | ns |
| Clock to Pin 5 | T_{MULTCK_P5} | - | 1.15 | ns |
| Clock to Pin 4 | T_{MULTCK_P4} | - | 1.15 | ns |
| Clock to Pin 3 | T_{MULTCK_P3} | - | 1.15 | ns |
| Clock to Pin 2 | T_{MULTCK_P2} | - | 1.15 | ns |
| Clock to Pin 1 | T_{MULTCK_P1} | - | 1.15 | ns |
| Clock to Pin 0 | T_{MULTCK_P0} | - | 1.15 | ns |

Block SelectRAM Switching Characteristics

Table 55: Block SelectRAM Switching Characteristics

| Description | Symbol | Min | Min | Units |
|--|---------------------|------------|------|-------|
| Sequential Delays | | | | |
| Clock CLK to DOUT output | T_{BCKO} | - | 2.65 | ns |
| Setup and Hold Times Before Clock CLK | | | | |
| ADDR inputs | T_{BACK}/T_{BCKA} | 0.36/ 0.00 | - | ns |
| DIN inputs | T_{BDCK}/T_{BCKD} | 0.36/ 0.00 | - | ns |
| EN input | T_{BECK}/T_{BCKE} | 1.20/-0.58 | - | ns |
| RST input | T_{BRCK}/T_{BCKR} | 1.65/-0.90 | - | ns |
| WEN input | T_{BWCK}/T_{BCKW} | 0.72/-0.25 | - | ns |
| Clock CLK | | | | |
| Minimum Pulse Width, High | T_{BPWH} | 1.48 | - | ns |
| Minimum Pulse Width, Low | T_{BPWL} | 1.48 | - | ns |

TBUF Switching Characteristics

Table 56: TBUF Switching Characteristics

| Description | Symbol | Min | Max | Units |
|--|-----------|-----|------|-------|
| Combinatorial Delays | | | | |
| IN input to OUT output | T_{IO} | - | 0.58 | ns |
| TRI input to OUT output high-impedance | T_{OFF} | - | 0.55 | ns |
| TRI input to valid data on OUT output | T_{ON} | - | 0.55 | ns |

JTAG Test Access Port Switching Characteristics

Table 57: JTAG Test Access Port Switching Characteristics

| Description | Symbol | Min | Max | Units |
|---|--------------|-----|------|-------|
| TMS and TDI Setup times before TCK | T_{TAPTK} | 5.5 | - | ns |
| TMS and TDI Hold times after TCK | T_{TCKTAP} | 0.0 | - | ns |
| Output delay from clock TCK to output TDO | T_{TCKTDO} | - | 10.0 | ns |
| Maximum TCK clock frequency | F_{TCK} | - | 33 | MHz |

QPro Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *with* DCM

Table 58: Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *with* DCM

| Description | Symbol | Device | Value | Units |
|--|----------------|-----------|-------|-------|
| LVTTTL Global Clock Input to Output delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments , page 56. | | | | |
| Global Clock and OFF with DCM | $T_{ICKOFDCM}$ | XQR2V1000 | 2.76 | ns |
| | | XQR2V3000 | 2.88 | ns |
| | | XQR2V6000 | 3.45 | ns |

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- Output timing is measured with a 35 pF external capacitive load. The only time it is not 50% of V_{CC} threshold is with LVCMOS. For other I/O standards and different loads, see [Table 48](#).
- DCM output jitter is included in the measurement.

Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *without* DCM

Table 59: Global Clock Input to Output Delay for LVTTTL, 12 mA, Fast Slew Rate, *without* DCM

| Description | Symbol | Device | Value | Units |
|---|-------------|-----------|-------|-------|
| LVTTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DCM. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments , page 56. | | | | |
| Global Clock and OFF without DCM | T_{ICKOF} | XQR2V1000 | 5.90 | ns |
| | | XQR2V3000 | 6.62 | ns |
| | | XQR2V6000 | 7.22 | ns |

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 48](#).

QPro Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTTL Standard, *with* DCM

Table 60: Global Clock Setup and Hold for LVTTTL Standard, *with* DCM

| Description | Symbol | Device | Value | Units |
|--|-----------------------|---------------|------------|-------|
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments , page 53. | | | | |
| No Delay Global Clock and IFF with DCM | T_{PSDCM}/T_{PHDCM} | XQR2V100 0 | 1.84/-0.76 | ns |
| | | XQR2V300 0 | 1.96/-0.76 | ns |
| | | XQR2V600 0 | 1.96/-0.76 | ns |

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

Global Clock Setup and Hold for LVTTTL Standard, *without* DCM

Table 61: Global Clock Setup and Hold for LVTTTL Standard, *without* DCM

| Description | Symbol | Device | Value | Units |
|---|---------------------|-----------|------------|-------|
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTTL Standard. ⁽¹⁾ For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments , page 53. | | | | |
| Full Delay Global Clock and IFF ⁽²⁾ without DCM | T_{PSFD}/T_{PHFD} | XQR2V1000 | 2.21/ 0.00 | ns |
| | | XQR2V3000 | 2.21/ 0.00 | ns |
| | | XQR2V6000 | 2.21/ 0.50 | ns |

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. IFF = Input Flip-Flop or Latch
3. These values are parametrically measured.

DCM Timing Parameters

All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values

across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 62: Operating Frequency Ranges

| Description | Symbol | Constraints | Value | Units |
|---|-----------------------|-------------|--------|-------|
| Output Clocks (Low Frequency Mode) | | | | |
| CLK0, CLK90, CLK180, CLK270 | CLKOUT_FREQ_1X_LF_Min | | 24.00 | MHz |
| | CLKOUT_FREQ_1X_LF_Max | | 180.00 | MHz |
| CLK2X, CLK2X180 | CLKOUT_FREQ_2X_LF_Min | | 48.00 | MHz |
| | CLKOUT_FREQ_2X_LF_Max | | 360.00 | MHz |
| CLKDV | CLKOUT_FREQ_DV_LF_Min | | 1.50 | MHz |
| | CLKOUT_FREQ_DV_LF_Max | | 120.00 | MHz |
| CLKFX, CLKFX180 | CLKOUT_FREQ_FX_LF_Min | | 24.00 | MHz |
| | CLKOUT_FREQ_FX_LF_Max | | 210.00 | MHz |
| Input Clocks (Low Frequency Mode) | | | | |
| CLKIN (using DLL outputs) ^{(1), (3)} | CLKIN_FREQ_DLL_LF_Min | | 24.00 | MHz |
| | CLKIN_FREQ_DLL_LF_Max | | 180.00 | MHz |
| CLKIN (using CLKFX outputs) ^{(2), (3)} | CLKIN_FREQ_FX_LF_Min | | 1.00 | MHz |
| | CLKIN_FREQ_FX_LF_Max | | 210.00 | MHz |
| PSCLK | PSCLK_FREQ_LF_Min | | 0.01 | MHz |
| | PSCLK_FREQ_LF_Max | | 360.00 | MHz |
| Output Clocks (High Frequency Mode) | | | | |
| CLK0, CLK180 | CLKOUT_FREQ_1X_HF_Min | | 48.00 | MHz |
| | CLKOUT_FREQ_1X_HF_Max | | 360.00 | MHz |
| CLKDV | CLKOUT_FREQ_DV_HF_Min | | 3.00 | MHz |
| | CLKOUT_FREQ_DV_HF_Max | | 240.00 | MHz |
| CLKFX, CLKFX180 | CLKOUT_FREQ_FX_HF_Min | | 210.00 | MHz |
| | CLKOUT_FREQ_FX_HF_Max | | 270.00 | MHz |
| Input Clocks (High Frequency Mode) | | | | |
| CLKIN (using DLL outputs) ^{(1), (3)} | CLKIN_FREQ_DLL_HF_Min | | 48.00 | MHz |
| | CLKIN_FREQ_DLL_HF_Max | | 360.00 | MHz |
| CLKIN (using CLKFX outputs) ^{(2), (3)} | CLKIN_FRQ_FX_HF_Min | | 50.00 | MHz |
| | CLKIN_FRQ_FX_HF_Max | | 270.00 | MHz |
| PSCLK | PSCLK_FREQ_HF_Min | | 0.01 | MHz |
| | PSCLK_FREQ_HF_Max | | 360.00 | MHz |

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.

Input Clock Tolerances

Table 63: Input Clock Tolerances

| Description | Symbol | Constraints F _{CLKIN} | Min | Max | Units |
|---|--------------------------------|-----------------------------------|-------|------|-------|
| Input Clock Low/High Pulse Width | | | | | |
| PSCLK | PSCLK_PULSE | < 1MHz | 25.00 | | ns |
| PSCLK and CLKIN ⁽²⁾ | PSCLK_PULSE and CLKIN_PULSE | 1 – 10 MHz | 25.00 | | ns |
| | | 10 – 25 MHz | 10.00 | | ns |
| | | 25 – 50 MHz | 5.00 | | ns |
| | | 50 – 100 MHz | 3.00 | | ns |
| | | 100 – 150 MHz | 2.40 | | ns |
| | | 150 – 200 MHz | 2.00 | | ns |
| | | 200 – 250 MHz | 1.80 | | ns |
| | | 250 – 300 MHz | 1.50 | | ns |
| | | 300 – 350 MHz | 1.30 | | ns |
| | | 350 – 400 MHz | 1.15 | | ns |
| > 400 MHz | 1.05 | | ns | | |
| Input Clock Cycle-Cycle Jitter (Low Frequency Mode) | | | | | |
| CLKIN (using DLL outputs) ⁽¹⁾ | CLKIN_CYC_JITT_DLL_LF | | | ±300 | ps |
| CLKIN (using CLKFX outputs) ⁽²⁾ | CLKIN_CYC_JITT_FX_LF | | | ±300 | ps |
| Input Clock Cycle-Cycle Jitter (High Frequency Mode) | | | | | |
| CLKIN (using DLL outputs) ⁽¹⁾ | CLKIN_CYC_JITT_DLL_HF | | | ±150 | ps |
| CLKIN (using CLKFX outputs) ⁽²⁾ | CLKIN_CYC_JITT_FX_HF | | | ±150 | ps |
| Input Clock Period Jitter (Low Frequency Mode) | | | | | |
| CLKIN (using DLL outputs) ⁽¹⁾ | CLKIN_PER_JITT_DLL_LF | | | ±1 | ns |
| CLKIN (using CLKFX outputs) ⁽²⁾ | CLKIN_PER_JITT_FX_LF | | | ±1 | ns |
| Input Clock Period Jitter (High Frequency Mode) | | | | | |
| CLKIN (using DLL outputs) ⁽¹⁾ | CLKIN_PER_JITT_DLL_HF | | | ±1 | ns |
| CLKIN (using CLKFX outputs) ⁽²⁾ | CLKIN_PER_JITT_FX_HF | | | ±1 | ns |
| Feedback Clock Path Delay Variation | | | | | |
| CLKFB off-chip feedback | CLKFB_DELAY_VAR_EXT | | | ±1 | ns |

Notes:

- “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- If both DLL and CLKFX outputs are used, follow the more restrictive specification.
- If the DCM phase shift feature is used and the CLKIN frequency > 200 MHz, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Output Clock Jitter

Table 64: Output Clock Jitter

| Description | Symbol | Constraints | Value | Units |
|--------------------------------------|---------------------|-------------|--------|-------|
| Clock Synthesis Period Jitter | | | | |
| CLK0 | CLKOUT_PER_JITT_0 | | ±100 | ps |
| CLK90 | CLKOUT_PER_JITT_90 | | ±150 | ps |
| CLK180 | CLKOUT_PER_JITT_180 | | ±150 | ps |
| CLK270 | CLKOUT_PER_JITT_270 | | ±150 | ps |
| CLK2X, CLK2X180 | CLKOUT_PER_JITT_2X | | ±200 | ps |
| CLKDV (integer division) | CLKOUT_PER_JITT_DV1 | | ±150 | ps |
| CLKDV (non-integer division) | CLKOUT_PER_JITT_DV2 | | ±300 | ps |
| CLKFX, CLKFX180 | CLKOUT_PER_JITT_FX | | Note 1 | ps |

Notes:

1. Values for this parameter are available at <http://www.xilinx.com>.

Output Clock Phase Alignment

Table 65: Output Clock Phase Alignment

| Description | Symbol | Constraints | Value | Units |
|---|--------------------------------------|-------------|-------|-------|
| Phase Offset Between CLKIN and CLKFB | | | | |
| CLKIN/CLKFB | CLKIN_CLKFB_PHASE | | ±50 | ps |
| Phase Offset Between Any DCM Outputs | | | | |
| All CLK* outputs | CLKOUT_PHASE | | ±140 | ps |
| Duty Cycle Precision | | | | |
| DLL outputs ⁽¹⁾ | CLKOUT_DUTY_CYCLE_DLL ⁽²⁾ | | ±150 | ps |
| CLKFX outputs | CLKOUT_DUTY_CYCLE_FX | | ±100 | ps |

Notes:

1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
3. Specification also applies to PSCLK.

Miscellaneous Timing Parameters

Table 66: Miscellaneous Timing Parameters

| Description | Symbol | Constraints F _{CLKIN} | Value | Units |
|---|---------------------|-----------------------------------|-------|-------|
| Time Required to Achieve LOCK | | | | |
| Using DLL outputs ⁽¹⁾ | LOCK_DLL | | | |
| | LOCK_DLL_60 | > 60MHz | 20.0 | μs |
| | LOCK_DLL_50_60 | 50 - 60 MHz | 25.0 | μs |
| | LOCK_DLL_40_50 | 40 - 50 MHz | 50.0 | μs |
| | LOCK_DLL_30_40 | 30 - 40 MHz | 90.0 | μs |
| | LOCK_DLL_24_30 | 24 - 30 MHz | 120.0 | μs |
| Using CLKFX outputs | LOCK_FX_MIN | | 10.0 | ms |
| | LOCK_FX_MAX | | 10.0 | ms |
| Additional lock time with fine-phase shifting | LOCK_DLL_FINE_SHIFT | | 50.0 | μs |
| Fine-Phase Shifting | | | | |
| Absolute shifting range | FINE_SHIFT_RANGE | | 10.0 | ns |
| Delay Lines | | | | |
| Tap delay resolution | DCM_TAP_MIN | | 30.0 | ps |
| | DCM_TAP_MAX | | 60.0 | ps |

Notes:

- ⁽¹⁾ "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- Specification also applies to PSCLK.

Frequency Synthesis

Table 67: Frequency Synthesis

| Attribute | Min | Max |
|----------------|-----|-----|
| CLKFX_MULTIPLY | 2 | 32 |
| CLKFX_DIVIDE | 1 | 32 |

Parameter Cross Reference

Table 68: Parameter Cross Reference

| Libraries Guide | Data Sheet |
|-------------------------|---------------------------|
| DLL_CLKOUT_{MIN MAX}_LF | CLKOUT_FREQ_{1X 2X DV}_LF |
| DFS_CLKOUT_{MIN MAX}_LF | CLKOUT_FREQ_FX_LF |
| DLL_CLKIN_{MIN MAX}_LF | CLKIN_FREQ_DLL_LF |
| DFS_CLKIN_{MIN MAX}_LF | CLKIN_FREQ_FX_LF |
| DLL_CLKOUT_{MIN MAX}_HF | CLKOUT_FREQ_{1X DV}_HF |
| DFS_CLKOUT_{MIN MAX}_HF | CLKOUT_FREQ_FX_HF |
| DLL_CLKIN_{MIN MAX}_HF | CLKIN_FREQ_DLL_HF |
| DFS_CLKIN_{MIN MAX}_HF | CLKIN_FREQ_FX_HF |

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for QPro Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 69: Duty Cycle Distortion and Clock-Tree Skew

| Description | Symbol | Device | Value | Units |
|--------------------------------------|-------------------------|---------------|-------|-------|
| Duty Cycle Distortion ⁽¹⁾ | T _{DCD_CLK0} | All | 140 | ps |
| | T _{DCD_CLK180} | All | 50 | ps |
| Clock Tree Skew ⁽²⁾ | T _{CKSKEW} | XQR2V100 0 | 90 | ps |
| | | XQR2V300 0 | 110 | ps |
| | | XQR2V600 0 | 550 | ps |

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O. T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
- This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 70: Package Skew

| Description | Symbol | Device/Package | Value | Units |
|-----------------------------|----------------------|------------------|-------|-------|
| Package Skew ⁽¹⁾ | T _{PKGSKEW} | XQR2V6000/CF1144 | 90 | ps |

Notes:

- These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 71: Sample Window

| Description | Symbol | Device | Value | Units |
|--|------------|---------------|-------|-------|
| Sampling Error at Receiver Pins ⁽¹⁾ | T_{SAMP} | XQR2V100 0 | TBD | ps |
| | | XQR2V300 0 | TBD | ps |
| | | XQR2V600 0 | TBD | ps |

Notes:

- This parameter indicates the total sampling error of QPro Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 and CLK180 DCM jitter
 - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
 - DCM accuracy (phase offset)
 - DCM phase shift resolution.
 These measurements do not include package or clock tree skew.

Table 72: Pin-to-Pin Setup/Hold: Source-Synchronous Configuration

| Description | Symbol | Device | Value | Units |
|--|-----------------------|---------------|-------|-------|
| Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments , page 53. | | | | |
| No Delay Global Clock and IFF with DCM | T_{PSDCM}/T_{PHDCM} | XQR2V100 0 | TBD | ns |
| | | XQR2V300 0 | TBD | ns |
| | | XQR2V600 0 | TBD | ns |

Notes:

- IFF = Input Flip-Flop
- The timing values were measured using the fine-phase adjustment feature of the DCM.
- The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the **Source-Synchronous Switching Characteristics** section to develop system-specific timing budgets. The following analysis provides information necessary for deter-

mining QPro Virtex-II contributions to an overall system timing analysis. No assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

QPro Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$T_X = \text{Data Period} - [\text{Jitter}^{(1)} + \text{Duty Cycle Distortion}^{(2)} + \text{TCKSKEW}^{(3)} + \text{TPKGSKEW}^{(4)}]$$

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the **DCM Timing Parameters** section of the particular DCM output clock used to clock the IOB FF can be used for a best-case analysis.
2. This value depends on the clocking methodology used. See Note 1 for **Table 69**.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

QPro Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

$$R_X = [\text{TSAMP}^{(1)} + \text{TCKSKEW}^{(2)} + \text{TPKGSKEW}^{(3)}]$$

Notes:

1. This parameter indicates the total sampling error of QPro Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 and CLK180 DCM jitter in a quiet system
 - Worst-case duty-cycle distortion
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

QPro Virtex-II Device/Package Combinations and Maximum I/Os Available

This section provides **QPro Virtex-II Device/Package Combinations and Maximum I/Os Available** and **QPro Virtex-II Pin Definitions**, followed by pinout tables for the following packages:

- **FG456 Fine-Pitch BGA Package**
- **BG575 Standard BGA Package**
- **BG728 Standard BGA and CG717 Ceramic CGA Packages**
- **CF1144 Ceramic Flip-Chip Fine-Pitch CGA Package**

QPro Virtex-II devices are available in both wire-bond and flip-chip packages. The basic package dimensions are listed in [Table 73](#). See [Figure 52](#) through [Figure 56](#) for a more complete mechanical description of each available package. [Table 74](#) shows the maximum number of user I/Os

possible for each available package. There are four package type definitions:

- FG denotes plastic wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes plastic wire-bond ball grid array (1.27 mm pitch).
- CG denotes hermetic ceramic wire-bond column grid array (1.27 mm pitch).
- CF denotes non-hermetic ceramic flip-chip column grid array (1.00 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 73: Package Information

| Package | FG456 | BG575 | BG728 & CG717 | CF1144 |
|------------|---------|---------|---------------|---------|
| Pitch (mm) | 1.00 | 1.27 | 1.27 | 1.00 |
| Size (mm) | 23 x 23 | 31 x 31 | 35 x 35 | 35 x 35 |

Table 74: QPro Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)

| Package | Available I/Os | | |
|---------|----------------|-----------|-----------|
| | XQR2V1000 | XQR2V3000 | XQR2V6000 |
| FG456 | 324 | - | - |
| BG575 | 328 | - | - |
| BG728 | - | 516 | - |
| CG717 | - | 516 | - |
| CF1144 | - | - | 824 |

Notes:

1. The BG728 and CG717 packages are pinout (footprint) compatible.

QPro Virtex-II Pin Definitions

This section describes the pinouts for QPro Virtex-II devices in the following packages:

- FG456: wire-bond fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- CG717: wire-bond ceramic column grid of 1.27 mm pitch
- CF1144: Ceramic flip-chip fine-pitch column grid of 1.00 mm pitch

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the *QPro Virtex-II Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. [Table 75](#) provides definitions for all pin types.

All QPro Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at <http://www.xilinx.com>).

Pin Definitions

Table 75 provides a description of each pin type listed in QPro Virtex-II pinout tables.

Table 75: QPro Virtex-II Pin Definitions

| Pin Name | Direction | Description |
|-------------------------------------|----------------------------|---|
| User I/O Pins | | |
| IO_LXXY_# | Input/Output | All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "IO_LXXY_#", where: <ul style="list-style-type: none"> IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = P/N for the positive and negative sides of the differential pair. # indicates the bank number (0 through 7). |
| Dual-Function Pins | | |
| IO_LXXY_#/ZZZ | | The dual-function pins are labelled "IO_LXXY_#/ZZZ", where ZZZ can be one of the following pins: Per Bank - VRP, VRN, or VREF Globally - GCLKX(S/P), BUSY/DOUT, INIT_B, DIN/D0 – D7, RDWR_B, or CS_B |
| With /ZZZ | | |
| DIN/D0, D1, D2, D3, D4, D5, D6, D7 | Input/Output | In SelectMAP mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. In bit-serial modes, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration. |
| CS_B | Input | In SelectMAP mode, this is the active-Low Chip Select signal. This pin becomes a user I/O after configuration, unless the SelectMAP port is retained. |
| RDWR_B | Input | In SelectMAP mode, this is the active-Low Write Enable signal. This pin becomes a user I/O after configuration, unless the SelectMAP port is retained. |
| BUSY/DOUT | Output | In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration, unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy chain. This pin becomes a user I/O after configuration. |
| INIT_B | Bidirectional (open-drain) | When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. This pin becomes a user I/O after configuration. |
| GCLKx (S/P) | Input/Output | These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. |
| VRP | Input | This pin is for the DCI voltage reference resistor of the P transistor (per bank). |
| VRN | Input | This pin is for the DCI voltage reference resistor of the N transistor (per bank). |
| ALT_VRP | Input | This is the alternative pin for the DCI voltage reference resistor of the P transistor. |
| ALT_VRN | Input | This is the alternative pin for the DCI voltage reference resistor of the N transistor. |
| VREF | Input | These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank). |
| Dedicated Pins⁽¹⁾ | | |
| CCLK | Input/Output | Configuration clock. Output in Master mode or Input in Slave mode. |

Table 75: QPro Virtex-II Pin Definitions (Continued)

| Pin Name | Direction | Description |
|--------------------|------------------------|---|
| PROG_B | Input | Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor. |
| DONE | Input/Output | DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence. |
| M2, M1, M0 | Input | Configuration mode selection. |
| HSWAP_EN | Input | Enable I/O pullups during configuration. |
| TCK | Input | Boundary Scan Clock. |
| TDI | Input | Boundary Scan Data Input. |
| TDO | Output | Boundary Scan Data Output. |
| TMS | Input | Boundary Scan Mode Select. |
| PWRDWN_B | Input (unsupported) | Active Low power-down pin (unsupported). <i>Driving this pin Low can adversely affect device operation and configuration.</i> PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up. |
| Other Pins | | |
| DXN, DXP | N/A | Temperature-sensing diode pins (Anode: DXP, Cathode: DXN). |
| V _{BATT} | Input | Decryptor key memory backup supply. (Do not connect if battery is not used.) |
| RSVD | N/A | Reserved pin - do not connect. |
| V _{CCO} | Input | Power-supply pins for the output drivers (per bank). |
| V _{CCAUX} | Input | Power-supply pins for auxiliary circuits. |
| V _{CCINT} | Input | Power-supply pins for the internal core logic. |
| GND | Input | Ground. |

Notes:

- All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).

FG456 Fine-Pitch BGA Package

As shown in [Table 76](#), the XQR2V1000 QPro Virtex-II device is available in the FG456 fine-pitch BGA package. Pins definitions are identical to the commercial grade

XC2V1000-FG456. Following this table are the **FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L01N_0 | B4 |
| 0 | IO_L01P_0 | A4 |
| 0 | IO_L02N_0 | C4 |
| 0 | IO_L02P_0 | C5 |
| 0 | IO_L03N_0/VRP_0 | B5 |
| 0 | IO_L03P_0/VRN_0 | A5 |
| 0 | IO_L04N_0/VREF_0 | D6 |
| 0 | IO_L04P_0 | C6 |
| 0 | IO_L05N_0 | B6 |
| 0 | IO_L05P_0 | A6 |
| 0 | IO_L06N_0 | E7 |
| 0 | IO_L06P_0 | E8 |
| 0 | IO_L21N_0 | D7 |
| 0 | IO_L21P_0/VREF_0 | C7 |
| 0 | IO_L22N_0 | B7 |
| 0 | IO_L22P_0 | A7 |
| 0 | IO_L24N_0 | D8 |
| 0 | IO_L24P_0 | C8 |
| 0 | IO_L49N_0 | B8 |
| 0 | IO_L49P_0 | A8 |
| 0 | IO_L51N_0 | E9 |
| 0 | IO_L51P_0/VREF_0 | F9 |
| 0 | IO_L52N_0 | D9 |
| 0 | IO_L52P_0 | C9 |
| 0 | IO_L54N_0 | B9 |
| 0 | IO_L54P_0 | A9 |
| 0 | IO_L91N_0/VREF_0 | E10 |
| 0 | IO_L91P_0 | F10 |
| 0 | IO_L92N_0 | D10 |
| 0 | IO_L92P_0 | C10 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L93N_0 | B10 |
| 0 | IO_L93P_0 | A10 |
| 0 | IO_L94N_0/VREF_0 | E11 |
| 0 | IO_L94P_0 | F11 |
| 0 | IO_L95N_0/GCLK7P | D11 |
| 0 | IO_L95P_0/GCLK6S | C11 |
| 0 | IO_L96N_0/GCLK5P | B11 |
| 0 | IO_L96P_0/GCLK4S | A11 |
| | | |
| 1 | IO_L96N_1/GCLK3P | F12 |
| 1 | IO_L96P_1/GCLK2S | F13 |
| 1 | IO_L95N_1/GCLK1P | E12 |
| 1 | IO_L95P_1/GCLK0S | D12 |
| 1 | IO_L94N_1 | C12 |
| 1 | IO_L94P_1/VREF_1 | B12 |
| 1 | IO_L93N_1 | A13 |
| 1 | IO_L93P_1 | B13 |
| 1 | IO_L92N_1 | C13 |
| 1 | IO_L92P_1 | D13 |
| 1 | IO_L91N_1 | E13 |
| 1 | IO_L91P_1/VREF_1 | E14 |
| 1 | IO_L54N_1 | A14 |
| 1 | IO_L54P_1 | B14 |
| 1 | IO_L52N_1 | C14 |
| 1 | IO_L52P_1 | D14 |
| 1 | IO_L51N_1/VREF_1 | A15 |
| 1 | IO_L51P_1 | B15 |
| 1 | IO_L49N_1 | C15 |
| 1 | IO_L49P_1 | D15 |
| 1 | IO_L24N_1 | F14 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L24P_1 | E15 |
| 1 | IO_L22N_1 | A16 |
| 1 | IO_L22P_1 | B16 |
| 1 | IO_L21N_1/VREF_1 | C16 |
| 1 | IO_L21P_1 | D16 |
| 1 | IO_L06N_1 | E16 |
| 1 | IO_L06P_1 | E17 |
| 1 | IO_L05N_1 | A17 |
| 1 | IO_L05P_1 | B17 |
| 1 | IO_L04N_1 | C17 |
| 1 | IO_L04P_1/VREF_1 | D17 |
| 1 | IO_L03N_1/VRP_1 | A18 |
| 1 | IO_L03P_1/VRN_1 | B18 |
| 1 | IO_L02N_1 | C18 |
| 1 | IO_L02P_1 | D18 |
| 1 | IO_L01N_1 | A19 |
| 1 | IO_L01P_1 | B19 |
| | | |
| 2 | IO_L01N_2 | C21 |
| 2 | IO_L01P_2 | C22 |
| 2 | IO_L02N_2/VRP_2 | E18 |
| 2 | IO_L02P_2/VRN_2 | F18 |
| 2 | IO_L03N_2 | D21 |
| 2 | IO_L03P_2/VREF_2 | D22 |
| 2 | IO_L04N_2 | E19 |
| 2 | IO_L04P_2 | E20 |
| 2 | IO_L06N_2 | E21 |
| 2 | IO_L06P_2 | E22 |
| 2 | IO_L19N_2 | F19 |
| 2 | IO_L19P_2 | F20 |
| 2 | IO_L21N_2 | F21 |
| 2 | IO_L21P_2/VREF_2 | F22 |
| 2 | IO_L22N_2 | G18 |
| 2 | IO_L22P_2 | H18 |
| 2 | IO_L24N_2 | G19 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L24P_2 | G20 |
| 2 | IO_L43N_2 | G21 |
| 2 | IO_L43P_2 | G22 |
| 2 | IO_L45N_2 | H19 |
| 2 | IO_L45P_2/VREF_2 | H20 |
| 2 | IO_L46N_2 | H21 |
| 2 | IO_L46P_2 | H22 |
| 2 | IO_L48N_2 | J17 |
| 2 | IO_L48P_2 | J18 |
| 2 | IO_L49N_2 | J19 |
| 2 | IO_L49P_2 | J20 |
| 2 | IO_L51N_2 | J21 |
| 2 | IO_L51P_2/VREF_2 | J22 |
| 2 | IO_L52N_2 | K17 |
| 2 | IO_L52P_2 | K18 |
| 2 | IO_L54N_2 | K19 |
| 2 | IO_L54P_2 | K20 |
| 2 | IO_L91N_2 | K21 |
| 2 | IO_L91P_2 | K22 |
| 2 | IO_L93N_2 | L17 |
| 2 | IO_L93P_2/VREF_2 | L18 |
| 2 | IO_L94N_2 | L19 |
| 2 | IO_L94P_2 | L20 |
| 2 | IO_L96N_2 | L21 |
| 2 | IO_L96P_2 | L22 |
| | | |
| 3 | IO_L96N_3 | M21 |
| 3 | IO_L96P_3 | M20 |
| 3 | IO_L94N_3 | M19 |
| 3 | IO_L94P_3 | M18 |
| 3 | IO_L93N_3/VREF_3 | M17 |
| 3 | IO_L93P_3 | N17 |
| 3 | IO_L91N_3 | N22 |
| 3 | IO_L91P_3 | N21 |
| 3 | IO_L54N_3 | N20 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 3 | IO_L54P_3 | N19 |
| 3 | IO_L52N_3 | N18 |
| 3 | IO_L52P_3 | P18 |
| 3 | IO_L51N_3/VREF_3 | P22 |
| 3 | IO_L51P_3 | P21 |
| 3 | IO_L49N_3 | P20 |
| 3 | IO_L49P_3 | P19 |
| 3 | IO_L48N_3 | R22 |
| 3 | IO_L48P_3 | R21 |
| 3 | IO_L46N_3 | R20 |
| 3 | IO_L46P_3 | R19 |
| 3 | IO_L45N_3/VREF_3 | R18 |
| 3 | IO_L45P_3 | P17 |
| 3 | IO_L43N_3 | T22 |
| 3 | IO_L43P_3 | T21 |
| 3 | IO_L24N_3 | T20 |
| 3 | IO_L24P_3 | T19 |
| 3 | IO_L22N_3 | U22 |
| 3 | IO_L22P_3 | U21 |
| 3 | IO_L21N_3/VREF_3 | U20 |
| 3 | IO_L21P_3 | U19 |
| 3 | IO_L19N_3 | T18 |
| 3 | IO_L19P_3 | U18 |
| 3 | IO_L06N_3 | V22 |
| 3 | IO_L06P_3 | V21 |
| 3 | IO_L04N_3 | V20 |
| 3 | IO_L04P_3 | V19 |
| 3 | IO_L03N_3/VREF_3 | W22 |
| 3 | IO_L03P_3 | W21 |
| 3 | IO_L02N_3/VRP_3 | Y22 |
| 3 | IO_L02P_3/VRN_3 | Y21 |
| 3 | IO_L01N_3 | W20 |
| 3 | IO_L01P_3 | AA20 |
| | | |
| 4 | IO_L01N_4/DOUT | AB19 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 4 | IO_L01P_4/INIT_B | AA19 |
| 4 | IO_L02N_4/D0 | V18 |
| 4 | IO_L02P_4/D1 | V17 |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | W18 |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | Y18 |
| 4 | IO_L04N_4/VREF_4 | AA18 |
| 4 | IO_L04P_4 | AB18 |
| 4 | IO_L05N_4/VRP_4 | W17 |
| 4 | IO_L05P_4/VRN_4 | Y17 |
| 4 | IO_L06N_4 | AA17 |
| 4 | IO_L06P_4 | AB17 |
| 4 | IO_L19N_4 | V16 |
| 4 | IO_L19P_4 | V15 |
| 4 | IO_L21N_4 | W16 |
| 4 | IO_L21P_4/VREF_4 | Y16 |
| 4 | IO_L22N_4 | AA16 |
| 4 | IO_L22P_4 | AB16 |
| 4 | IO_L24N_4 | W15 |
| 4 | IO_L24P_4 | Y15 |
| 4 | IO_L49N_4 | AA15 |
| 4 | IO_L49P_4 | AB15 |
| 4 | IO_L51N_4 | U14 |
| 4 | IO_L51P_4/VREF_4 | V14 |
| 4 | IO_L52N_4 | W14 |
| 4 | IO_L52P_4 | Y14 |
| 4 | IO_L54N_4 | AA14 |
| 4 | IO_L54P_4 | AB14 |
| 4 | IO_L91N_4/VREF_4 | U13 |
| 4 | IO_L91P_4 | V13 |
| 4 | IO_L92N_4 | W13 |
| 4 | IO_L92P_4 | Y13 |
| 4 | IO_L93N_4 | AA13 |
| 4 | IO_L93P_4 | AB13 |
| 4 | IO_L94N_4/VREF_4 | U12 |
| 4 | IO_L94P_4 | V12 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L95N_4/GCLK3S | W12 |
| 4 | IO_L95P_4/GCLK2P | Y12 |
| 4 | IO_L96N_4/GCLK1S | AA12 |
| 4 | IO_L96P_4/GCLK0P | AB12 |
| | | |
| 5 | IO_L96N_5/GCLK7S | AA11 |
| 5 | IO_L96P_5/GCLK6P | Y11 |
| 5 | IO_L95N_5/GCLK5S | W11 |
| 5 | IO_L95P_5/GCLK4P | V11 |
| 5 | IO_L94N_5 | U11 |
| 5 | IO_L94P_5/VREF_5 | U10 |
| 5 | IO_L93N_5 | AB10 |
| 5 | IO_L93P_5 | AA10 |
| 5 | IO_L92N_5 | Y10 |
| 5 | IO_L92P_5 | W10 |
| 5 | IO_L91N_5 | V10 |
| 5 | IO_L91P_5/VREF_5 | V9 |
| 5 | IO_L54N_5 | AB9 |
| 5 | IO_L54P_5 | AA9 |
| 5 | IO_L52N_5 | Y9 |
| 5 | IO_L52P_5 | W9 |
| 5 | IO_L51N_5/VREF_5 | AB8 |
| 5 | IO_L51P_5 | AA8 |
| 5 | IO_L49N_5 | Y8 |
| 5 | IO_L49P_5 | W8 |
| 5 | IO_L24N_5 | U9 |
| 5 | IO_L24P_5 | V8 |
| 5 | IO_L22N_5 | AB7 |
| 5 | IO_L22P_5 | AA7 |
| 5 | IO_L21N_5/VREF_5 | Y7 |
| 5 | IO_L21P_5 | W7 |
| 5 | IO_L19N_5 | AB6 |
| 5 | IO_L19P_5 | AA6 |
| 5 | IO_L06N_5 | Y6 |
| 5 | IO_L06P_5 | W6 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 5 | IO_L05N_5/VRP_5 | V7 |
| 5 | IO_L05P_5/VRN_5 | V6 |
| 5 | IO_L04N_5 | AB5 |
| 5 | IO_L04P_5/VREF_5 | AA5 |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | Y5 |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | W5 |
| 5 | IO_L02N_5/D6 | AB4 |
| 5 | IO_L02P_5/D7 | AA4 |
| 5 | IO_L01N_5/RDWR_B | Y4 |
| 5 | IO_L01P_5/CS_B | AA3 |
| | | |
| 6 | IO_L01P_6 | V5 |
| 6 | IO_L01N_6 | U5 |
| 6 | IO_L02P_6/VRN_6 | Y2 |
| 6 | IO_L02N_6/VRP_6 | Y1 |
| 6 | IO_L03P_6 | V4 |
| 6 | IO_L03N_6/VREF_6 | V3 |
| 6 | IO_L04P_6 | W2 |
| 6 | IO_L04N_6 | W1 |
| 6 | IO_L06P_6 | U4 |
| 6 | IO_L06N_6 | U3 |
| 6 | IO_L19P_6 | V2 |
| 6 | IO_L19N_6 | V1 |
| 6 | IO_L21P_6 | U2 |
| 6 | IO_L21N_6/VREF_6 | U1 |
| 6 | IO_L22P_6 | T5 |
| 6 | IO_L22N_6 | R5 |
| 6 | IO_L24P_6 | T4 |
| 6 | IO_L24N_6 | T3 |
| 6 | IO_L43P_6 | T2 |
| 6 | IO_L43N_6 | T1 |
| 6 | IO_L45P_6 | R4 |
| 6 | IO_L45N_6/VREF_6 | R3 |
| 6 | IO_L46P_6 | R2 |
| 6 | IO_L46N_6 | R1 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L48P_6 | P6 |
| 6 | IO_L48N_6 | P5 |
| 6 | IO_L49P_6 | P4 |
| 6 | IO_L49N_6 | P3 |
| 6 | IO_L51P_6 | P2 |
| 6 | IO_L51N_6/VREF_6 | P1 |
| 6 | IO_L52P_6 | N6 |
| 6 | IO_L52N_6 | N5 |
| 6 | IO_L54P_6 | N4 |
| 6 | IO_L54N_6 | N3 |
| 6 | IO_L91P_6 | N2 |
| 6 | IO_L91N_6 | N1 |
| 6 | IO_L93P_6 | M6 |
| 6 | IO_L93N_6/VREF_6 | M5 |
| 6 | IO_L94P_6 | M4 |
| 6 | IO_L94N_6 | M3 |
| 6 | IO_L96P_6 | M2 |
| 6 | IO_L96N_6 | M1 |
| | | |
| 7 | IO_L96P_7 | L2 |
| 7 | IO_L96N_7 | L3 |
| 7 | IO_L94P_7 | L4 |
| 7 | IO_L94N_7 | L5 |
| 7 | IO_L93P_7/VREF_7 | K1 |
| 7 | IO_L93N_7 | K2 |
| 7 | IO_L91P_7 | K3 |
| 7 | IO_L91N_7 | K4 |
| 7 | IO_L54P_7 | L6 |
| 7 | IO_L54N_7 | K6 |
| 7 | IO_L52P_7 | K5 |
| 7 | IO_L52N_7 | J5 |
| 7 | IO_L51P_7/VREF_7 | J1 |
| 7 | IO_L51N_7 | J2 |
| 7 | IO_L49P_7 | J3 |
| 7 | IO_L49N_7 | J4 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L48P_7 | H1 |
| 7 | IO_L48N_7 | H2 |
| 7 | IO_L46P_7 | H3 |
| 7 | IO_L46N_7 | H4 |
| 7 | IO_L45P_7/VREF_7 | J6 |
| 7 | IO_L45N_7 | H5 |
| 7 | IO_L43P_7 | G1 |
| 7 | IO_L43N_7 | G2 |
| 7 | IO_L24P_7 | G3 |
| 7 | IO_L24N_7 | G4 |
| 7 | IO_L22P_7 | F1 |
| 7 | IO_L22N_7 | F2 |
| 7 | IO_L21P_7/VREF_7 | F3 |
| 7 | IO_L21N_7 | F4 |
| 7 | IO_L19P_7 | G5 |
| 7 | IO_L19N_7 | F5 |
| 7 | IO_L06P_7 | E1 |
| 7 | IO_L06N_7 | E2 |
| 7 | IO_L04P_7 | E3 |
| 7 | IO_L04N_7 | E4 |
| 7 | IO_L03P_7/VREF_7 | D1 |
| 7 | IO_L03N_7 | D2 |
| 7 | IO_L02P_7/VRN_7 | C1 |
| 7 | IO_L02N_7/VRP_7 | C2 |
| 7 | IO_L01P_7 | E5 |
| 7 | IO_L01N_7 | E6 |
| | | |
| 0 | VCCO_0 | G11 |
| 0 | VCCO_0 | G10 |
| 0 | VCCO_0 | G9 |
| 0 | VCCO_0 | F8 |
| 0 | VCCO_0 | F7 |
| 1 | VCCO_1 | G14 |
| 1 | VCCO_1 | G13 |
| 1 | VCCO_1 | G12 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 1 | VCCO_1 | F16 |
| 1 | VCCO_1 | F15 |
| 2 | VCCO_2 | L16 |
| 2 | VCCO_2 | K16 |
| 2 | VCCO_2 | J16 |
| 2 | VCCO_2 | H17 |
| 2 | VCCO_2 | G17 |
| 3 | VCCO_3 | T17 |
| 3 | VCCO_3 | R17 |
| 3 | VCCO_3 | P16 |
| 3 | VCCO_3 | N16 |
| 3 | VCCO_3 | M16 |
| 4 | VCCO_4 | U16 |
| 4 | VCCO_4 | U15 |
| 4 | VCCO_4 | T14 |
| 4 | VCCO_4 | T13 |
| 4 | VCCO_4 | T12 |
| 5 | VCCO_5 | U8 |
| 5 | VCCO_5 | U7 |
| 5 | VCCO_5 | T11 |
| 5 | VCCO_5 | T10 |
| 5 | VCCO_5 | T9 |
| 6 | VCCO_6 | T6 |
| 6 | VCCO_6 | R6 |
| 6 | VCCO_6 | P7 |
| 6 | VCCO_6 | N7 |
| 6 | VCCO_6 | M7 |
| 7 | VCCO_7 | L7 |
| 7 | VCCO_7 | K7 |
| 7 | VCCO_7 | J7 |
| 7 | VCCO_7 | H6 |
| 7 | VCCO_7 | G6 |
| | | |
| NA | CCLK | Y19 |
| NA | PROG_B | A2 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | DONE | AB20 |
| NA | M0 | AB2 |
| NA | M1 | W3 |
| NA | M2 | AB3 |
| NA | HSWAP_EN | B3 |
| NA | TCK | C19 |
| NA | TDI | D3 |
| NA | TDO | D20 |
| NA | TMS | B20 |
| NA | PWRDWN_B | AB21 |
| NA | DXN | D5 |
| NA | DXP | A3 |
| NA | VBATT | A21 |
| NA | RSVD | A20 |
| | | |
| NA | VCCAUX | AB11 |
| NA | VCCAUX | AA22 |
| NA | VCCAUX | AA1 |
| NA | VCCAUX | M22 |
| NA | VCCAUX | L1 |
| NA | VCCAUX | B22 |
| NA | VCCAUX | B1 |
| NA | VCCAUX | A12 |
| NA | VCCINT | U17 |
| NA | VCCINT | U6 |
| NA | VCCINT | T16 |
| NA | VCCINT | T15 |
| NA | VCCINT | T8 |
| NA | VCCINT | T7 |
| NA | VCCINT | R16 |
| NA | VCCINT | R7 |
| NA | VCCINT | H16 |
| NA | VCCINT | H7 |
| NA | VCCINT | G16 |
| NA | VCCINT | G15 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCINT | G8 |
| NA | VCCINT | G7 |
| NA | VCCINT | F17 |
| NA | VCCINT | F6 |
| NA | GND | AB22 |
| NA | GND | AB1 |
| NA | GND | AA21 |
| NA | GND | AA2 |
| NA | GND | Y20 |
| NA | GND | Y3 |
| NA | GND | W19 |
| NA | GND | W4 |
| NA | GND | P14 |
| NA | GND | P13 |
| NA | GND | P12 |
| NA | GND | P11 |
| NA | GND | P10 |
| NA | GND | P9 |
| NA | GND | N14 |
| NA | GND | N13 |
| NA | GND | N12 |
| NA | GND | N11 |
| NA | GND | N10 |
| NA | GND | N9 |
| NA | GND | M14 |
| NA | GND | M13 |
| NA | GND | M12 |
| NA | GND | M11 |
| NA | GND | M10 |
| NA | GND | M9 |
| NA | GND | L14 |
| NA | GND | L13 |
| NA | GND | L12 |
| NA | GND | L11 |
| NA | GND | L10 |

Table 76: FG456 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | L9 |
| NA | GND | K14 |
| NA | GND | K13 |
| NA | GND | K12 |
| NA | GND | K11 |
| NA | GND | K10 |
| NA | GND | K9 |
| NA | GND | J14 |
| NA | GND | J13 |
| NA | GND | J12 |
| NA | GND | J11 |
| NA | GND | J10 |
| NA | GND | J9 |
| NA | GND | D19 |
| NA | GND | D4 |
| NA | GND | C20 |
| NA | GND | C3 |
| NA | GND | B21 |
| NA | GND | B2 |
| NA | GND | A22 |
| NA | GND | A1 |

FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)

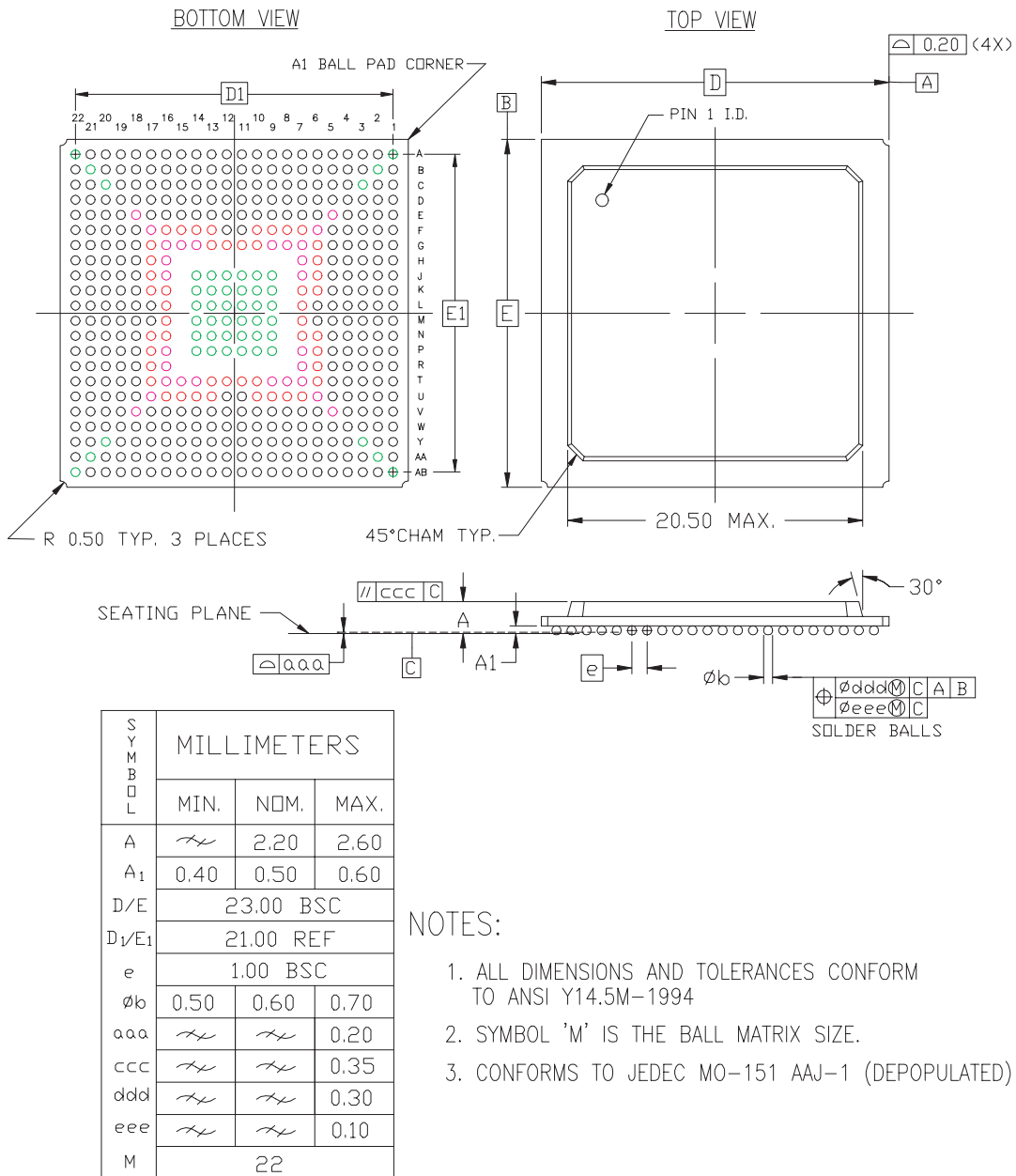


Figure 52: FG456 Fine-Pitch BGA Package Specifications

BG575 Standard BGA Package

As shown in [Table 77](#), the XQR2V1000 QPro Virtex-II device is available in the BG575 BGA package. Following

this table are the **BG575 Standard BGA Package Specifications (1.27mm pitch)**.

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L01N_0 | A3 |
| 0 | IO_L01P_0 | A4 |
| 0 | IO_L02N_0 | D5 |
| 0 | IO_L02P_0 | C5 |
| 0 | IO_L03N_0/VRP_0 | E6 |
| 0 | IO_L03P_0/VRN_0 | D6 |
| 0 | IO_L04N_0/VREF_0 | F7 |
| 0 | IO_L04P_0 | E7 |
| 0 | IO_L05N_0 | G8 |
| 0 | IO_L05P_0 | H9 |
| 0 | IO_L06N_0 | A5 |
| 0 | IO_L06P_0 | A6 |
| 0 | IO_L19N_0 | B5 |
| 0 | IO_L19P_0 | B6 |
| 0 | IO_L21N_0 | D7 |
| 0 | IO_L21P_0/VREF_0 | C7 |
| 0 | IO_L22N_0 | F8 |
| 0 | IO_L22P_0 | E8 |
| 0 | IO_L24N_0 | G9 |
| 0 | IO_L24P_0 | F9 |
| 0 | IO_L49N_0 | G10 |
| 0 | IO_L49P_0 | H10 |
| 0 | IO_L51N_0 | B7 |
| 0 | IO_L51P_0/VREF_0 | B8 |
| 0 | IO_L52N_0 | D8 |
| 0 | IO_L52P_0 | C8 |
| 0 | IO_L54N_0 | E9 |
| 0 | IO_L54P_0 | D9 |
| 0 | IO_L67N_0 | A8 |
| 0 | IO_L67P_0 | A9 |
| 0 | IO_L69N_0 | C9 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L69P_0/VREF_0 | B9 |
| 0 | IO_L70N_0 | F10 |
| 0 | IO_L70P_0 | E10 |
| 0 | IO_L72N_0 | A10 |
| 0 | IO_L72P_0 | A11 |
| 0 | IO_L73N_0 | C10 |
| 0 | IO_L73P_0 | B10 |
| 0 | IO_L91N_0/VREF_0 | D11 |
| 0 | IO_L91P_0 | C11 |
| 0 | IO_L92N_0 | G11 |
| 0 | IO_L92P_0 | E11 |
| 0 | IO_L93N_0 | C12 |
| 0 | IO_L93P_0 | B12 |
| 0 | IO_L94N_0/VREF_0 | E12 |
| 0 | IO_L94P_0 | D12 |
| 0 | IO_L95N_0/GCLK7P | G12 |
| 0 | IO_L95P_0/GCLK6S | F12 |
| 0 | IO_L96N_0/GCLK5P | H11 |
| 0 | IO_L96P_0/GCLK4S | H12 |
| | | |
| 1 | IO_L96N_1/GCLK3P | A13 |
| 1 | IO_L96P_1/GCLK2S | A14 |
| 1 | IO_L95N_1/GCLK1P | B13 |
| 1 | IO_L95P_1/GCLK0S | C13 |
| 1 | IO_L94N_1 | D13 |
| 1 | IO_L94P_1/VREF_1 | E13 |
| 1 | IO_L93N_1 | F13 |
| 1 | IO_L93P_1 | G13 |
| 1 | IO_L92N_1 | H13 |
| 1 | IO_L92P_1 | H14 |
| 1 | IO_L91N_1 | C14 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L91P_1/VREF_1 | D14 |
| 1 | IO_L73N_1 | E14 |
| 1 | IO_L73P_1 | G14 |
| 1 | IO_L72N_1 | A15 |
| 1 | IO_L72P_1 | A16 |
| 1 | IO_L70N_1 | B15 |
| 1 | IO_L70P_1 | C15 |
| 1 | IO_L69N_1/VREF_1 | E15 |
| 1 | IO_L69P_1 | F15 |
| 1 | IO_L67N_1 | G15 |
| 1 | IO_L67P_1 | H15 |
| 1 | IO_L54N_1 | B16 |
| 1 | IO_L54P_1 | C16 |
| 1 | IO_L52N_1 | D16 |
| 1 | IO_L52P_1 | E16 |
| 1 | IO_L51N_1/VREF_1 | F16 |
| 1 | IO_L51P_1 | G16 |
| 1 | IO_L49N_1 | A17 |
| 1 | IO_L49P_1 | A19 |
| 1 | IO_L24N_1 | B17 |
| 1 | IO_L24P_1 | B18 |
| 1 | IO_L22N_1 | C17 |
| 1 | IO_L22P_1 | D17 |
| 1 | IO_L21N_1/VREF_1 | F17 |
| 1 | IO_L21P_1 | E17 |
| 1 | IO_L19N_1 | A20 |
| 1 | IO_L19P_1 | A21 |
| 1 | IO_L06N_1 | B19 |
| 1 | IO_L06P_1 | B20 |
| 1 | IO_L05N_1 | C18 |
| 1 | IO_L05P_1 | D18 |
| 1 | IO_L04N_1 | C20 |
| 1 | IO_L04P_1/VREF_1 | D20 |
| 1 | IO_L03N_1/VRP_1 | D19 |
| 1 | IO_L03P_1/VRN_1 | E19 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L02N_1 | E18 |
| 1 | IO_L02P_1 | F18 |
| 1 | IO_L01N_1 | H16 |
| 1 | IO_L01P_1 | G17 |
| | | |
| 2 | IO_L01N_2 | D22 |
| 2 | IO_L01P_2 | D23 |
| 2 | IO_L02N_2/VRP_2 | E21 |
| 2 | IO_L02P_2/VRN_2 | E22 |
| 2 | IO_L03N_2 | F21 |
| 2 | IO_L03P_2/VREF_2 | F20 |
| 2 | IO_L04N_2 | G20 |
| 2 | IO_L04P_2 | G19 |
| 2 | IO_L06N_2 | H18 |
| 2 | IO_L06P_2 | J17 |
| 2 | IO_L19N_2 | D24 |
| 2 | IO_L19P_2 | E23 |
| 2 | IO_L21N_2 | E24 |
| 2 | IO_L21P_2/VREF_2 | F24 |
| 2 | IO_L22N_2 | F23 |
| 2 | IO_L22P_2 | G23 |
| 2 | IO_L24N_2 | G21 |
| 2 | IO_L24P_2 | G22 |
| 2 | IO_L43N_2 | H19 |
| 2 | IO_L43P_2 | H20 |
| 2 | IO_L45N_2 | J18 |
| 2 | IO_L45P_2/VREF_2 | J19 |
| 2 | IO_L46N_2 | K17 |
| 2 | IO_L46P_2 | K18 |
| 2 | IO_L48N_2 | H23 |
| 2 | IO_L48P_2 | H24 |
| 2 | IO_L49N_2 | H21 |
| 2 | IO_L49P_2 | H22 |
| 2 | IO_L51N_2 | J24 |
| 2 | IO_L51P_2/VREF_2 | K24 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L52N_2 | J22 |
| 2 | IO_L52P_2 | J23 |
| 2 | IO_L54N_2 | J20 |
| 2 | IO_L54P_2 | J21 |
| 2 | IO_L67N_2 | K19 |
| 2 | IO_L67P_2 | K20 |
| 2 | IO_L69N_2 | L17 |
| 2 | IO_L69P_2/VREF_2 | L18 |
| 2 | IO_L70N_2 | K23 |
| 2 | IO_L70P_2 | L24 |
| 2 | IO_L72N_2 | K22 |
| 2 | IO_L72P_2 | L22 |
| 2 | IO_L73N_2 | L21 |
| 2 | IO_L73P_2 | L20 |
| 2 | IO_L91N_2 | M23 |
| 2 | IO_L91P_2 | N24 |
| 2 | IO_L93N_2 | M21 |
| 2 | IO_L93P_2/VREF_2 | M22 |
| 2 | IO_L94N_2 | M19 |
| 2 | IO_L94P_2 | M20 |
| 2 | IO_L96N_2 | M17 |
| 2 | IO_L96P_2 | M18 |
| | | |
| 3 | IO_L96N_3 | N23 |
| 3 | IO_L96P_3 | N22 |
| 3 | IO_L94N_3 | N20 |
| 3 | IO_L94P_3 | N21 |
| 3 | IO_L93N_3/VREF_3 | N19 |
| 3 | IO_L93P_3 | N18 |
| 3 | IO_L91N_3 | N17 |
| 3 | IO_L91P_3 | P17 |
| 3 | IO_L73N_3 | P24 |
| 3 | IO_L73P_3 | R24 |
| 3 | IO_L72N_3 | R23 |
| 3 | IO_L72P_3 | R22 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 3 | IO_L70N_3 | P22 |
| 3 | IO_L70P_3 | P21 |
| 3 | IO_L69N_3/VREF_3 | P20 |
| 3 | IO_L69P_3 | P18 |
| 3 | IO_L67N_3 | T24 |
| 3 | IO_L67P_3 | U24 |
| 3 | IO_L54N_3 | T23 |
| 3 | IO_L54P_3 | T22 |
| 3 | IO_L52N_3 | T21 |
| 3 | IO_L52P_3 | T20 |
| 3 | IO_L51N_3/VREF_3 | R20 |
| 3 | IO_L51P_3 | R19 |
| 3 | IO_L49N_3 | W24 |
| 3 | IO_L49P_3 | W23 |
| 3 | IO_L48N_3 | U23 |
| 3 | IO_L48P_3 | V23 |
| 3 | IO_L46N_3 | U22 |
| 3 | IO_L46P_3 | U21 |
| 3 | IO_L45N_3/VREF_3 | V22 |
| 3 | IO_L45P_3 | V21 |
| 3 | IO_L43N_3 | U19 |
| 3 | IO_L43P_3 | U20 |
| 3 | IO_L24N_3 | T19 |
| 3 | IO_L24P_3 | T18 |
| 3 | IO_L22N_3 | R18 |
| 3 | IO_L22P_3 | R17 |
| 3 | IO_L21N_3/VREF_3 | Y24 |
| 3 | IO_L21P_3 | Y23 |
| 3 | IO_L19N_3 | AA24 |
| 3 | IO_L19P_3 | AB24 |
| 3 | IO_L06N_3 | AA23 |
| 3 | IO_L06P_3 | AA22 |
| 3 | IO_L04N_3 | Y22 |
| 3 | IO_L04P_3 | Y21 |
| 3 | IO_L03N_3/VREF_3 | W21 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 3 | IO_L03P_3 | W20 |
| 3 | IO_L02N_3/VRP_3 | V20 |
| 3 | IO_L02P_3/VRN_3 | V19 |
| 3 | IO_L01N_3 | U18 |
| 3 | IO_L01P_3 | T17 |
| | | |
| 4 | IO_L01N_4/DOUT | AD22 |
| 4 | IO_L01P_4/INIT_B | AD21 |
| 4 | IO_L02N_4/D0 | AA20 |
| 4 | IO_L02P_4/D1 | AB20 |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | Y19 |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | AA19 |
| 4 | IO_L04N_4/VREF_4 | W18 |
| 4 | IO_L04P_4 | Y18 |
| 4 | IO_L05N_4/VRP_4 | U16 |
| 4 | IO_L05P_4/VRN_4 | V17 |
| 4 | IO_L06N_4 | AD20 |
| 4 | IO_L06P_4 | AD19 |
| 4 | IO_L19N_4 | AC20 |
| 4 | IO_L19P_4 | AC19 |
| 4 | IO_L21N_4 | AA18 |
| 4 | IO_L21P_4/VREF_4 | AB18 |
| 4 | IO_L22N_4 | AC18 |
| 4 | IO_L22P_4 | AC17 |
| 4 | IO_L24N_4 | AA17 |
| 4 | IO_L24P_4 | AB17 |
| 4 | IO_L49N_4 | Y17 |
| 4 | IO_L49P_4 | W17 |
| 4 | IO_L51N_4 | V16 |
| 4 | IO_L51P_4/VREF_4 | W16 |
| 4 | IO_L52N_4 | AD17 |
| 4 | IO_L52P_4 | AD16 |
| 4 | IO_L54N_4 | AB16 |
| 4 | IO_L54P_4 | AC16 |
| 4 | IO_L67N_4 | Y16 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L67P_4 | AA16 |
| 4 | IO_L69N_4 | W15 |
| 4 | IO_L69P_4/VREF_4 | Y15 |
| 4 | IO_L70N_4 | U15 |
| 4 | IO_L70P_4 | V15 |
| 4 | IO_L72N_4 | AD15 |
| 4 | IO_L72P_4 | AD14 |
| 4 | IO_L73N_4 | AB15 |
| 4 | IO_L73P_4 | AC15 |
| 4 | IO_L91N_4/VREF_4 | AA14 |
| 4 | IO_L91P_4 | AB14 |
| 4 | IO_L92N_4 | V14 |
| 4 | IO_L92P_4 | Y14 |
| 4 | IO_L93N_4 | AB13 |
| 4 | IO_L93P_4 | AC13 |
| 4 | IO_L94N_4/VREF_4 | Y13 |
| 4 | IO_L94P_4 | AA13 |
| 4 | IO_L95N_4/GCLK3S | V13 |
| 4 | IO_L95P_4/GCLK2P | W13 |
| 4 | IO_L96N_4/GCLK1S | U14 |
| 4 | IO_L96P_4/GCLK0P | U13 |
| | | |
| 5 | IO_L96N_5/GCLK7S | AD12 |
| 5 | IO_L96P_5/GCLK6P | AD11 |
| 5 | IO_L95N_5/GCLK5S | AC12 |
| 5 | IO_L95P_5/GCLK4P | AB12 |
| 5 | IO_L94N_5 | AA12 |
| 5 | IO_L94P_5/VREF_5 | Y12 |
| 5 | IO_L93N_5 | W12 |
| 5 | IO_L93P_5 | V12 |
| 5 | IO_L92N_5 | U12 |
| 5 | IO_L92P_5 | U11 |
| 5 | IO_L91N_5 | AB11 |
| 5 | IO_L91P_5/VREF_5 | AA11 |
| 5 | IO_L73N_5 | Y11 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 5 | IO_L73P_5 | V11 |
| 5 | IO_L72N_5 | AD10 |
| 5 | IO_L72P_5 | AD9 |
| 5 | IO_L70N_5 | AC10 |
| 5 | IO_L70P_5 | AB10 |
| 5 | IO_L69N_5/VREF_5 | Y10 |
| 5 | IO_L69P_5 | W10 |
| 5 | IO_L67N_5 | V10 |
| 5 | IO_L67P_5 | U10 |
| 5 | IO_L54N_5 | AC9 |
| 5 | IO_L54P_5 | AB9 |
| 5 | IO_L52N_5 | AA9 |
| 5 | IO_L52P_5 | Y9 |
| 5 | IO_L51N_5/VREF_5 | W9 |
| 5 | IO_L51P_5 | V9 |
| 5 | IO_L49N_5 | AD8 |
| 5 | IO_L49P_5 | AD6 |
| 5 | IO_L24N_5 | AC8 |
| 5 | IO_L24P_5 | AC7 |
| 5 | IO_L22N_5 | AB8 |
| 5 | IO_L22P_5 | AA8 |
| 5 | IO_L21N_5/VREF_5 | W8 |
| 5 | IO_L21P_5 | Y8 |
| 5 | IO_L19N_5 | AD5 |
| 5 | IO_L19P_5 | AD4 |
| 5 | IO_L06N_5 | AC6 |
| 5 | IO_L06P_5 | AC5 |
| 5 | IO_L05N_5/VRP_5 | AB7 |
| 5 | IO_L05P_5/VRN_5 | AA7 |
| 5 | IO_L04N_5 | AB5 |
| 5 | IO_L04P_5/VREF_5 | AA5 |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | AA6 |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | Y6 |
| 5 | IO_L02N_5/D6 | Y7 |
| 5 | IO_L02P_5/D7 | W7 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 5 | IO_L01N_5/RDWR_B | V8 |
| 5 | IO_L01P_5/CS_B | U9 |
| | | |
| 6 | IO_L01P_6 | AB2 |
| 6 | IO_L01N_6 | AB1 |
| 6 | IO_L02P_6/VRN_6 | AA3 |
| 6 | IO_L02N_6/VRP_6 | AA2 |
| 6 | IO_L03P_6 | Y4 |
| 6 | IO_L03N_6/VREF_6 | Y3 |
| 6 | IO_L04P_6 | W4 |
| 6 | IO_L04N_6 | W5 |
| 6 | IO_L06P_6 | V5 |
| 6 | IO_L06N_6 | V6 |
| 6 | IO_L19P_6 | U7 |
| 6 | IO_L19N_6 | T8 |
| 6 | IO_L21P_6 | AA1 |
| 6 | IO_L21N_6/VREF_6 | Y2 |
| 6 | IO_L22P_6 | Y1 |
| 6 | IO_L22N_6 | W1 |
| 6 | IO_L24P_6 | W2 |
| 6 | IO_L24N_6 | V2 |
| 6 | IO_L43P_6 | V4 |
| 6 | IO_L43N_6 | V3 |
| 6 | IO_L45P_6 | U6 |
| 6 | IO_L45N_6/VREF_6 | U5 |
| 6 | IO_L46P_6 | T7 |
| 6 | IO_L46N_6 | T6 |
| 6 | IO_L48P_6 | R8 |
| 6 | IO_L48N_6 | R7 |
| 6 | IO_L49P_6 | U2 |
| 6 | IO_L49N_6 | U1 |
| 6 | IO_L51P_6 | U4 |
| 6 | IO_L51N_6/VREF_6 | U3 |
| 6 | IO_L52P_6 | T1 |
| 6 | IO_L52N_6 | R1 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L54P_6 | T3 |
| 6 | IO_L54N_6 | T2 |
| 6 | IO_L67P_6 | T5 |
| 6 | IO_L67N_6 | T4 |
| 6 | IO_L69P_6 | R6 |
| 6 | IO_L69N_6/VREF_6 | R5 |
| 6 | IO_L70P_6 | P8 |
| 6 | IO_L70N_6 | P7 |
| 6 | IO_L72P_6 | R2 |
| 6 | IO_L72N_6 | P1 |
| 6 | IO_L73P_6 | R3 |
| 6 | IO_L73N_6 | P3 |
| 6 | IO_L91P_6 | P5 |
| 6 | IO_L91N_6 | P4 |
| 6 | IO_L93P_6 | N4 |
| 6 | IO_L93N_6/VREF_6 | N3 |
| 6 | IO_L94P_6 | N6 |
| 6 | IO_L94N_6 | N5 |
| 6 | IO_L96P_6 | N8 |
| 6 | IO_L96N_6 | N7 |
| | | |
| 7 | IO_L96P_7 | N2 |
| 7 | IO_L96N_7 | M1 |
| 7 | IO_L94P_7 | M2 |
| 7 | IO_L94N_7 | M3 |
| 7 | IO_L93P_7/VREF_7 | M4 |
| 7 | IO_L93N_7 | M5 |
| 7 | IO_L91P_7 | M6 |
| 7 | IO_L91N_7 | M7 |
| 7 | IO_L73P_7 | M8 |
| 7 | IO_L73N_7 | L8 |
| 7 | IO_L72P_7 | L1 |
| 7 | IO_L72N_7 | K1 |
| 7 | IO_L70P_7 | K2 |
| 7 | IO_L70N_7 | K3 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L69P_7/VREF_7 | L3 |
| 7 | IO_L69N_7 | L4 |
| 7 | IO_L67P_7 | L5 |
| 7 | IO_L67N_7 | L7 |
| 7 | IO_L54P_7 | J1 |
| 7 | IO_L54N_7 | H1 |
| 7 | IO_L52P_7 | J2 |
| 7 | IO_L52N_7 | J3 |
| 7 | IO_L51P_7/VREF_7 | J4 |
| 7 | IO_L51N_7 | J5 |
| 7 | IO_L49P_7 | K5 |
| 7 | IO_L49N_7 | K6 |
| 7 | IO_L48P_7 | F1 |
| 7 | IO_L48N_7 | F2 |
| 7 | IO_L46P_7 | H2 |
| 7 | IO_L46N_7 | G2 |
| 7 | IO_L45P_7/VREF_7 | H3 |
| 7 | IO_L45N_7 | H4 |
| 7 | IO_L43P_7 | G3 |
| 7 | IO_L43N_7 | G4 |
| 7 | IO_L24P_7 | H5 |
| 7 | IO_L24N_7 | H6 |
| 7 | IO_L22P_7 | J6 |
| 7 | IO_L22N_7 | J7 |
| 7 | IO_L21P_7/VREF_7 | K7 |
| 7 | IO_L21N_7 | K8 |
| 7 | IO_L19P_7 | E1 |
| 7 | IO_L19N_7 | E2 |
| 7 | IO_L06P_7 | D2 |
| 7 | IO_L06N_7 | D3 |
| 7 | IO_L04P_7 | E3 |
| 7 | IO_L04N_7 | E4 |
| 7 | IO_L03P_7/VREF_7 | F4 |
| 7 | IO_L03N_7 | F5 |
| 7 | IO_L02P_7/VRN_7 | G5 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 7 | IO_L02N_7/VRP_7 | G6 |
| 7 | IO_L01P_7 | H7 |
| 7 | IO_L01N_7 | J8 |
| | | |
| 0 | VCCO_0 | J12 |
| 0 | VCCO_0 | J11 |
| 0 | VCCO_0 | J10 |
| 0 | VCCO_0 | F11 |
| 0 | VCCO_0 | C6 |
| 0 | VCCO_0 | B11 |
| 1 | VCCO_1 | J15 |
| 1 | VCCO_1 | J14 |
| 1 | VCCO_1 | J13 |
| 1 | VCCO_1 | F14 |
| 1 | VCCO_1 | C19 |
| 1 | VCCO_1 | B14 |
| 2 | VCCO_2 | M16 |
| 2 | VCCO_2 | L23 |
| 2 | VCCO_2 | L19 |
| 2 | VCCO_2 | L16 |
| 2 | VCCO_2 | K16 |
| 2 | VCCO_2 | F22 |
| 3 | VCCO_3 | W22 |
| 3 | VCCO_3 | R16 |
| 3 | VCCO_3 | P23 |
| 3 | VCCO_3 | P19 |
| 3 | VCCO_3 | P16 |
| 3 | VCCO_3 | N16 |
| 4 | VCCO_4 | AC14 |
| 4 | VCCO_4 | AB19 |
| 4 | VCCO_4 | W14 |
| 4 | VCCO_4 | T15 |
| 4 | VCCO_4 | T14 |
| 4 | VCCO_4 | T13 |
| 5 | VCCO_5 | AC11 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 5 | VCCO_5 | AB6 |
| 5 | VCCO_5 | W11 |
| 5 | VCCO_5 | T12 |
| 5 | VCCO_5 | T11 |
| 5 | VCCO_5 | T10 |
| 6 | VCCO_6 | W3 |
| 6 | VCCO_6 | R9 |
| 6 | VCCO_6 | P9 |
| 6 | VCCO_6 | P6 |
| 6 | VCCO_6 | P2 |
| 6 | VCCO_6 | N9 |
| 7 | VCCO_7 | M9 |
| 7 | VCCO_7 | L9 |
| 7 | VCCO_7 | L6 |
| 7 | VCCO_7 | L2 |
| 7 | VCCO_7 | K9 |
| 7 | VCCO_7 | F3 |
| | | |
| NA | CCLK | AB23 |
| NA | PROG_B | C1 |
| NA | DONE | AB21 |
| NA | M0 | AC4 |
| NA | M1 | AB4 |
| NA | M2 | AD3 |
| NA | HSWAP_EN | C2 |
| NA | TCK | C23 |
| NA | TDI | D1 |
| NA | TDO | C24 |
| NA | TMS | C21 |
| NA | PWRDWN_B | AC21 |
| NA | DXN | B4 |
| NA | DXP | C4 |
| NA | VBATT | B21 |
| NA | RSVD | A22 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCAUX | AD13 |
| NA | VCCAUX | AC22 |
| NA | VCCAUX | AC3 |
| NA | VCCAUX | N1 |
| NA | VCCAUX | M24 |
| NA | VCCAUX | B22 |
| NA | VCCAUX | B3 |
| NA | VCCAUX | A12 |
| NA | VCCINT | U17 |
| NA | VCCINT | U8 |
| NA | VCCINT | T16 |
| NA | VCCINT | T9 |
| NA | VCCINT | R15 |
| NA | VCCINT | R14 |
| NA | VCCINT | R13 |
| NA | VCCINT | R12 |
| NA | VCCINT | R11 |
| NA | VCCINT | R10 |
| NA | VCCINT | P15 |
| NA | VCCINT | P10 |
| NA | VCCINT | N15 |
| NA | VCCINT | N10 |
| NA | VCCINT | M15 |
| NA | VCCINT | M10 |
| NA | VCCINT | L15 |
| NA | VCCINT | L10 |
| NA | VCCINT | K15 |
| NA | VCCINT | K14 |
| NA | VCCINT | K13 |
| NA | VCCINT | K12 |
| NA | VCCINT | K11 |
| NA | VCCINT | K10 |
| NA | VCCINT | J16 |
| NA | VCCINT | J9 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCINT | H17 |
| NA | VCCINT | H8 |
| NA | GND | AD24 |
| NA | GND | AD23 |
| NA | GND | AD18 |
| NA | GND | AD7 |
| NA | GND | AD2 |
| NA | GND | AD1 |
| NA | GND | AC24 |
| NA | GND | AC23 |
| NA | GND | AC2 |
| NA | GND | AC1 |
| NA | GND | AB22 |
| NA | GND | AB3 |
| NA | GND | AA21 |
| NA | GND | AA15 |
| NA | GND | AA10 |
| NA | GND | AA4 |
| NA | GND | Y20 |
| NA | GND | Y5 |
| NA | GND | W19 |
| NA | GND | W6 |
| NA | GND | V24 |
| NA | GND | V18 |
| NA | GND | V7 |
| NA | GND | V1 |
| NA | GND | R21 |
| NA | GND | R4 |
| NA | GND | P14 |
| NA | GND | P13 |
| NA | GND | P12 |
| NA | GND | P11 |
| NA | GND | N14 |
| NA | GND | N13 |
| NA | GND | N12 |

Table 77: BG575 BGA — XQR2V1000

| Bank | Pin Description | Pin Number |
|-------------|------------------------|-------------------|
| NA | GND | N11 |
| NA | GND | M14 |
| NA | GND | M13 |
| NA | GND | M12 |
| NA | GND | M11 |
| NA | GND | L14 |
| NA | GND | L13 |
| NA | GND | L12 |
| NA | GND | L11 |
| NA | GND | K21 |
| NA | GND | K4 |
| NA | GND | G24 |
| NA | GND | G18 |
| NA | GND | G7 |
| NA | GND | G1 |
| NA | GND | F19 |
| NA | GND | F6 |
| NA | GND | E20 |
| NA | GND | E5 |
| NA | GND | D21 |
| NA | GND | D15 |
| NA | GND | D10 |
| NA | GND | D4 |
| NA | GND | C22 |
| NA | GND | C3 |
| NA | GND | B24 |
| NA | GND | B23 |
| NA | GND | B2 |
| NA | GND | B1 |
| NA | GND | A24 |
| NA | GND | A23 |
| NA | GND | A18 |
| NA | GND | A7 |
| NA | GND | A2 |

BG575 Standard BGA Package Specifications (1.27mm pitch)

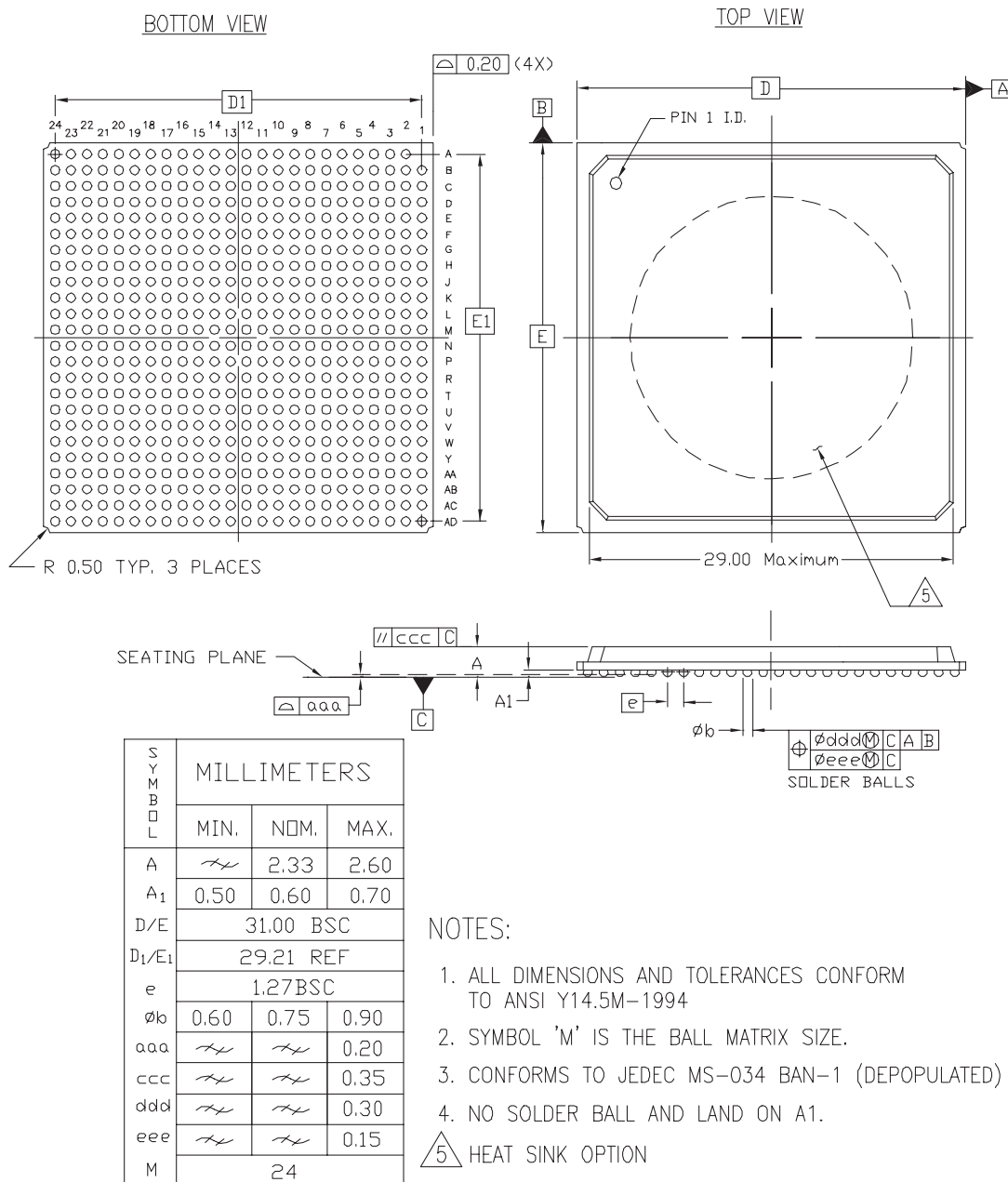


Figure 53: BG575 Standard BGA Package Specifications

BG728 Standard BGA and CG717 Ceramic CGA Packages

As shown in [Table 79](#), the XQR2V3000 QPro Virtex-II device is available in the BG728 BGA and CG717 CGA packages. The CG717 has identical pinout as the BG728 (except for those pins listed as Removed¹) and footprint compatibility. A summary of the removed pins is shown in [Table 78](#). Following this table are the **BG728 Standard BGA Package Specifications (1.27mm pitch)** and the **CG717 Ceramic Column Grid Array (CGA) Package Specifications (1.27mm pitch)**. The CG717 has 11 fewer GND pins than the BG728. The BG728 GND pin numbers missing on the CG717 are shown in [Table 78](#).

Table 78: BG728 GND Pins not available on the CG717¹

| BG728 GND Pin Numbers | | | |
|-----------------------|-----|------|------|
| A2 | A27 | AG1 | AG26 |
| B1 | B27 | AG2 | AG27 |
| A26 | AF1 | AF27 | |

1. Physical pin does not exist for CG717 package.

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L01N_0 | B3 |
| 0 | IO_L01P_0 | A3 |
| 0 | IO_L02N_0 | B4 |
| 0 | IO_L02P_0 | A4 |
| 0 | IO_L03N_0/VRP_0 | C5 |
| 0 | IO_L03P_0/VRN_0 | C6 |
| 0 | IO_L04N_0/VREF_0 | B5 |
| 0 | IO_L04P_0 | A5 |
| 0 | IO_L05N_0 | E6 |
| 0 | IO_L05P_0 | D6 |
| 0 | IO_L06N_0 | B6 |
| 0 | IO_L06P_0 | A6 |
| 0 | IO_L19N_0 | E7 |
| 0 | IO_L19P_0 | D8 |
| 0 | IO_L21N_0 | F8 |
| 0 | IO_L21P_0/VREF_0 | E8 |
| 0 | IO_L22N_0 | C7 |
| 0 | IO_L22P_0 | C8 |
| 0 | IO_L24N_0 | B7 |
| 0 | IO_L24P_0 | A7 |
| 0 | IO_L25N_0 | H9 |
| 0 | IO_L25P_0 | J9 |
| 0 | IO_L27N_0 | F9 |
| 0 | IO_L27P_0/VREF_0 | G9 |
| 0 | IO_L28N_0 | E9 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L28P_0 | D9 |
| 0 | IO_L30N_0 | C9 |
| 0 | IO_L30P_0 | B9 |
| 0 | IO_L49N_0 | A8 |
| 0 | IO_L49P_0 | A9 |
| 0 | IO_L51N_0 | G10 |
| 0 | IO_L51P_0/VREF_0 | H10 |
| 0 | IO_L52N_0 | F10 |
| 0 | IO_L52P_0 | E10 |
| 0 | IO_L54N_0 | D10 |
| 0 | IO_L54P_0 | C10 |
| 0 | IO_L67N_0 | B10 |
| 0 | IO_L67P_0 | A10 |
| 0 | IO_L69N_0 | G11 |
| 0 | IO_L69P_0/VREF_0 | H11 |
| 0 | IO_L70N_0 | F11 |
| 0 | IO_L70P_0 | F12 |
| 0 | IO_L72N_0 | D11 |
| 0 | IO_L72P_0 | C11 |
| 0 | IO_L73N_0 | B11 |
| 0 | IO_L73P_0 | A11 |
| 0 | IO_L75N_0 | H12 |
| 0 | IO_L75P_0/VREF_0 | J12 |
| 0 | IO_L76N_0 | E12 |
| 0 | IO_L76P_0 | D12 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L78N_0 | B12 |
| 0 | IO_L78P_0 | A12 |
| 0 | IO_L91N_0/VREF_0 | J13 |
| 0 | IO_L91P_0 | H13 |
| 0 | IO_L92N_0 | G13 |
| 0 | IO_L92P_0 | F13 |
| 0 | IO_L93N_0 | E13 |
| 0 | IO_L93P_0 | D13 |
| 0 | IO_L94N_0/VREF_0 | B13 |
| 0 | IO_L94P_0 | A13 |
| 0 | IO_L95N_0/GCLK7P | C13 |
| 0 | IO_L95P_0/GCLK6S | C14 |
| 0 | IO_L96N_0/GCLK5P | F14 |
| 0 | IO_L96P_0/GCLK4S | E14 |
| | | |
| 1 | IO_L96N_1/GCLK3P | G14 |
| 1 | IO_L96P_1/GCLK2S | H14 |
| 1 | IO_L95N_1/GCLK1P | A15 |
| 1 | IO_L95P_1/GCLK0S | B15 |
| 1 | IO_L94N_1 | C15 |
| 1 | IO_L94P_1/VREF_1 | D15 |
| 1 | IO_L93N_1 | E15 |
| 1 | IO_L93P_1 | F15 |
| 1 | IO_L92N_1 | G15 |
| 1 | IO_L92P_1 | H15 |
| 1 | IO_L91N_1 | J15 |
| 1 | IO_L91P_1/VREF_1 | J16 |
| 1 | IO_L78N_1 | A16 |
| 1 | IO_L78P_1 | B16 |
| 1 | IO_L76N_1 | D16 |
| 1 | IO_L76P_1 | E16 |
| 1 | IO_L75N_1/VREF_1 | F16 |
| 1 | IO_L75P_1 | F17 |
| 1 | IO_L73N_1 | H16 |
| 1 | IO_L73P_1 | H17 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L72N_1 | A17 |
| 1 | IO_L72P_1 | B17 |
| 1 | IO_L70N_1 | C17 |
| 1 | IO_L70P_1 | D17 |
| 1 | IO_L69N_1/VREF_1 | G18 |
| 1 | IO_L69P_1 | G17 |
| 1 | IO_L67N_1 | A18 |
| 1 | IO_L67P_1 | B18 |
| 1 | IO_L54N_1 | C18 |
| 1 | IO_L54P_1 | D18 |
| 1 | IO_L52N_1 | E18 |
| 1 | IO_L52P_1 | F18 |
| 1 | IO_L51N_1/VREF_1 | H19 |
| 1 | IO_L51P_1 | H18 |
| 1 | IO_L49N_1 | A19 |
| 1 | IO_L49P_1 | A20 |
| 1 | IO_L30N_1 | B19 |
| 1 | IO_L30P_1 | C19 |
| 1 | IO_L28N_1 | D19 |
| 1 | IO_L28P_1 | E19 |
| 1 | IO_L27N_1/VREF_1 | F19 |
| 1 | IO_L27P_1 | G19 |
| 1 | IO_L25N_1 | J19 |
| 1 | IO_L25P_1 | J20 |
| 1 | IO_L24N_1 | C20 |
| 1 | IO_L24P_1 | C21 |
| 1 | IO_L22N_1 | D20 |
| 1 | IO_L22P_1 | E21 |
| 1 | IO_L21N_1/VREF_1 | E20 |
| 1 | IO_L21P_1 | F20 |
| 1 | IO_L19N_1 | A21 |
| 1 | IO_L19P_1 | B21 |
| 1 | IO_L06N_1 | A22 |
| 1 | IO_L06P_1 | B22 |
| 1 | IO_L05N_1 | C22 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L05P_1 | C23 |
| 1 | IO_L04N_1 | D22 |
| 1 | IO_L04P_1/VREF_1 | E22 |
| 1 | IO_L03N_1/VRP_1 | A23 |
| 1 | IO_L03P_1/VRN_1 | B23 |
| 1 | IO_L02N_1 | A24 |
| 1 | IO_L02P_1 | B24 |
| 1 | IO_L01N_1 | A25 |
| 1 | IO_L01P_1 | B25 |
| | | |
| 2 | IO_L01N_2 | C27 |
| 2 | IO_L01P_2 | D27 |
| 2 | IO_L02N_2/VRP_2 | D25 |
| 2 | IO_L02P_2/VRN_2 | D26 |
| 2 | IO_L03N_2 | E24 |
| 2 | IO_L03P_2/VREF_2 | E25 |
| 2 | IO_L04N_2 | E26 |
| 2 | IO_L04P_2 | E27 |
| 2 | IO_L06N_2 | F23 |
| 2 | IO_L06P_2 | F24 |
| 2 | IO_L19N_2 | F25 |
| 2 | IO_L19P_2 | F26 |
| 2 | IO_L21N_2 | F27 |
| 2 | IO_L21P_2/VREF_2 | G27 |
| 2 | IO_L22N_2 | G23 |
| 2 | IO_L22P_2 | H23 |
| 2 | IO_L24N_2 | G25 |
| 2 | IO_L24P_2 | G26 |
| 2 | IO_L25N_2 | H21 |
| 2 | IO_L25P_2 | J21 |
| 2 | IO_L27N_2 | H22 |
| 2 | IO_L27P_2/VREF_2 | J22 |
| 2 | IO_L28N_2 | H24 |
| 2 | IO_L28P_2 | H25 |
| 2 | IO_L30N_2 | H27 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L30P_2 | J27 |
| 2 | IO_L43N_2 | J23 |
| 2 | IO_L43P_2 | J24 |
| 2 | IO_L45N_2 | J25 |
| 2 | IO_L45P_2/VREF_2 | J26 |
| 2 | IO_L46N_2 | K20 |
| 2 | IO_L46P_2 | K21 |
| 2 | IO_L48N_2 | K22 |
| 2 | IO_L48P_2 | K23 |
| 2 | IO_L49N_2 | K24 |
| 2 | IO_L49P_2 | K25 |
| 2 | IO_L51N_2 | K26 |
| 2 | IO_L51P_2/VREF_2 | K27 |
| 2 | IO_L52N_2 | L20 |
| 2 | IO_L52P_2 | M20 |
| 2 | IO_L54N_2 | L21 |
| 2 | IO_L54P_2 | L22 |
| 2 | IO_L67N_2 | L24 |
| 2 | IO_L67P_2 | L25 |
| 2 | IO_L69N_2 | L26 |
| 2 | IO_L69P_2/VREF_2 | L27 |
| 2 | IO_L70N_2 | M19 |
| 2 | IO_L70P_2 | N19 |
| 2 | IO_L72N_2 | M22 |
| 2 | IO_L72P_2 | M23 |
| 2 | IO_L73N_2 | M24 |
| 2 | IO_L73P_2 | N24 |
| 2 | IO_L75N_2 | M26 |
| 2 | IO_L75P_2/VREF_2 | M27 |
| 2 | IO_L76N_2 | N20 |
| 2 | IO_L76P_2 | N21 |
| 2 | IO_L78N_2 | N22 |
| 2 | IO_L78P_2 | N23 |
| 2 | IO_L91N_2 | N25 |
| 2 | IO_L91P_2 | P25 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L93N_2 | N26 |
| 2 | IO_L93P_2/VREF_2 | N27 |
| 2 | IO_L94N_2 | P20 |
| 2 | IO_L94P_2 | P21 |
| 2 | IO_L96N_2 | P22 |
| 2 | IO_L96P_2 | P23 |
| | | |
| 3 | IO_L96N_3 | R27 |
| 3 | IO_L96P_3 | R26 |
| 3 | IO_L94N_3 | R25 |
| 3 | IO_L94P_3 | R24 |
| 3 | IO_L93N_3/VREF_3 | R23 |
| 3 | IO_L93P_3 | T23 |
| 3 | IO_L91N_3 | R22 |
| 3 | IO_L91P_3 | R21 |
| 3 | IO_L78N_3 | R20 |
| 3 | IO_L78P_3 | R19 |
| 3 | IO_L76N_3 | T27 |
| 3 | IO_L76P_3 | T26 |
| 3 | IO_L75N_3/VREF_3 | T24 |
| 3 | IO_L75P_3 | U24 |
| 3 | IO_L73N_3 | T22 |
| 3 | IO_L73P_3 | U22 |
| 3 | IO_L72N_3 | T20 |
| 3 | IO_L72P_3 | T19 |
| 3 | IO_L70N_3 | U27 |
| 3 | IO_L70P_3 | U26 |
| 3 | IO_L69N_3/VREF_3 | U25 |
| 3 | IO_L69P_3 | V25 |
| 3 | IO_L67N_3 | U21 |
| 3 | IO_L67P_3 | U20 |
| 3 | IO_L54N_3 | V27 |
| 3 | IO_L54P_3 | V26 |
| 3 | IO_L52N_3 | V24 |
| 3 | IO_L52P_3 | V23 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 3 | IO_L51N_3/VREF_3 | V22 |
| 3 | IO_L51P_3 | W22 |
| 3 | IO_L49N_3 | V21 |
| 3 | IO_L49P_3 | V20 |
| 3 | IO_L48N_3 | W27 |
| 3 | IO_L48P_3 | Y27 |
| 3 | IO_L46N_3 | W26 |
| 3 | IO_L46P_3 | W25 |
| 3 | IO_L45N_3/VREF_3 | W24 |
| 3 | IO_L45P_3 | W23 |
| 3 | IO_L43N_3 | W21 |
| 3 | IO_L43P_3 | W20 |
| 3 | IO_L28N_3 | W19 |
| 3 | IO_L28P_3 | Y19 |
| 3 | IO_L27N_3/VREF_3 | Y25 |
| 3 | IO_L27P_3 | Y24 |
| 3 | IO_L25N_3 | Y23 |
| 3 | IO_L25P_3 | AA23 |
| 3 | IO_L24N_3 | Y22 |
| 3 | IO_L24P_3 | Y21 |
| 3 | IO_L22N_3 | AA27 |
| 3 | IO_L22P_3 | AB27 |
| 3 | IO_L21N_3/VREF_3 | AA26 |
| 3 | IO_L21P_3 | AA25 |
| 3 | IO_L19N_3 | AB26 |
| 3 | IO_L19P_3 | AB25 |
| 3 | IO_L06N_3 | AB24 |
| 3 | IO_L06P_3 | AB23 |
| 3 | IO_L04N_3 | AC27 |
| 3 | IO_L04P_3 | AC26 |
| 3 | IO_L03N_3/VREF_3 | AC25 |
| 3 | IO_L03P_3 | AC24 |
| 3 | IO_L02N_3/VRP_3 | AD27 |
| 3 | IO_L02P_3/VRN_3 | AE27 |
| 3 | IO_L01N_3 | AD26 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 3 | IO_L01P_3 | AD25 |
| | | |
| 4 | IO_L01N_4/DOU | AF25 |
| 4 | IO_L01P_4/INIT_B | AG25 |
| 4 | IO_L02N_4/D0 | AF24 |
| 4 | IO_L02P_4/D1 | AG24 |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | AD23 |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | AE23 |
| 4 | IO_L04N_4/VREF_4 | AF23 |
| 4 | IO_L04P_4 | AG23 |
| 4 | IO_L05N_4/VRP_4 | AD22 |
| 4 | IO_L05P_4/VRN_4 | AE22 |
| 4 | IO_L06N_4 | AF22 |
| 4 | IO_L06P_4 | AG22 |
| 4 | IO_L19N_4 | AC21 |
| 4 | IO_L19P_4 | AB21 |
| 4 | IO_L21N_4 | AE21 |
| 4 | IO_L21P_4/VREF_4 | AE20 |
| 4 | IO_L22N_4 | AF21 |
| 4 | IO_L22P_4 | AG21 |
| 4 | IO_L24N_4 | AB20 |
| 4 | IO_L24P_4 | AA20 |
| 4 | IO_L25N_4 | AC20 |
| 4 | IO_L25P_4 | AD20 |
| 4 | IO_L27N_4 | AG20 |
| 4 | IO_L27P_4/VREF_4 | AG19 |
| 4 | IO_L28N_4 | AB19 |
| 4 | IO_L28P_4 | AA19 |
| 4 | IO_L30N_4 | AC19 |
| 4 | IO_L30P_4 | AD19 |
| 4 | IO_L49N_4 | AE19 |
| 4 | IO_L49P_4 | AF19 |
| 4 | IO_L51N_4 | AA18 |
| 4 | IO_L51P_4/VREF_4 | Y18 |
| 4 | IO_L52N_4 | AB18 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L52P_4 | AC18 |
| 4 | IO_L54N_4 | AD18 |
| 4 | IO_L54P_4 | AE18 |
| 4 | IO_L67N_4 | AF18 |
| 4 | IO_L67P_4 | AG18 |
| 4 | IO_L69N_4 | AA17 |
| 4 | IO_L69P_4/VREF_4 | Y17 |
| 4 | IO_L70N_4 | AB17 |
| 4 | IO_L70P_4 | AB16 |
| 4 | IO_L72N_4 | AD17 |
| 4 | IO_L72P_4 | AE17 |
| 4 | IO_L73N_4 | AF17 |
| 4 | IO_L73P_4 | AG17 |
| 4 | IO_L75N_4 | Y16 |
| 4 | IO_L75P_4/VREF_4 | W16 |
| 4 | IO_L76N_4 | AC16 |
| 4 | IO_L76P_4 | AD16 |
| 4 | IO_L78N_4 | AF16 |
| 4 | IO_L78P_4 | AG16 |
| 4 | IO_L91N_4/VREF_4 | W15 |
| 4 | IO_L91P_4 | Y15 |
| 4 | IO_L92N_4 | AB15 |
| 4 | IO_L92P_4 | AA15 |
| 4 | IO_L93N_4 | AC15 |
| 4 | IO_L93P_4 | AD15 |
| 4 | IO_L94N_4/VREF_4 | AE15 |
| 4 | IO_L94P_4 | AE14 |
| 4 | IO_L95N_4/GCLK3S | AF15 |
| 4 | IO_L95P_4/GCLK2P | AG15 |
| 4 | IO_L96N_4/GCLK1S | Y14 |
| 4 | IO_L96P_4/GCLK0P | AA14 |
| | | |
| 5 | IO_L96N_5/GCLK7S | AC14 |
| 5 | IO_L96P_5/GCLK6P | AB14 |
| 5 | IO_L95N_5/GCLK5S | AG13 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 5 | IO_L95P_5/GCLK4P | AF13 |
| 5 | IO_L94N_5 | AE13 |
| 5 | IO_L94P_5/VREF_5 | AD13 |
| 5 | IO_L93N_5 | AC13 |
| 5 | IO_L93P_5 | AB13 |
| 5 | IO_L92N_5 | AA13 |
| 5 | IO_L92P_5 | Y13 |
| 5 | IO_L91N_5 | W13 |
| 5 | IO_L91P_5/VREF_5 | W12 |
| 5 | IO_L78N_5 | AG12 |
| 5 | IO_L78P_5 | AF12 |
| 5 | IO_L76N_5 | AD12 |
| 5 | IO_L76P_5 | AC12 |
| 5 | IO_L75N_5/VREF_5 | AB12 |
| 5 | IO_L75P_5 | AB11 |
| 5 | IO_L73N_5 | Y12 |
| 5 | IO_L73P_5 | Y11 |
| 5 | IO_L72N_5 | AG11 |
| 5 | IO_L72P_5 | AF11 |
| 5 | IO_L70N_5 | AE11 |
| 5 | IO_L70P_5 | AD11 |
| 5 | IO_L69N_5/VREF_5 | AA10 |
| 5 | IO_L69P_5 | AA11 |
| 5 | IO_L67N_5 | AG10 |
| 5 | IO_L67P_5 | AF10 |
| 5 | IO_L54N_5 | AE10 |
| 5 | IO_L54P_5 | AD10 |
| 5 | IO_L52N_5 | AC10 |
| 5 | IO_L52P_5 | AB10 |
| 5 | IO_L51N_5/VREF_5 | Y9 |
| 5 | IO_L51P_5 | Y10 |
| 5 | IO_L49N_5 | AG9 |
| 5 | IO_L49P_5 | AG8 |
| 5 | IO_L30N_5 | AF9 |
| 5 | IO_L30P_5 | AE9 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 5 | IO_L28N_5 | AD9 |
| 5 | IO_L28P_5 | AC9 |
| 5 | IO_L27N_5/VREF_5 | AB9 |
| 5 | IO_L27P_5 | AA9 |
| 5 | IO_L25N_5 | AE8 |
| 5 | IO_L25P_5 | AE7 |
| 5 | IO_L24N_5 | AD8 |
| 5 | IO_L24P_5 | AC8 |
| 5 | IO_L22N_5 | AB8 |
| 5 | IO_L22P_5 | AA8 |
| 5 | IO_L21N_5/VREF_5 | AG7 |
| 5 | IO_L21P_5 | AF7 |
| 5 | IO_L19N_5 | AC7 |
| 5 | IO_L19P_5 | AB7 |
| 5 | IO_L06N_5 | AG6 |
| 5 | IO_L06P_5 | AF6 |
| 5 | IO_L05N_5/VRP_5 | AE6 |
| 5 | IO_L05P_5/VRN_5 | AD6 |
| 5 | IO_L04N_5 | AG5 |
| 5 | IO_L04P_5/VREF_5 | AF5 |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | AE5 |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | AD5 |
| 5 | IO_L02N_5/D6 | AG4 |
| 5 | IO_L02P_5/D7 | AF4 |
| 5 | IO_L01N_5/RDWR_B | AG3 |
| 5 | IO_L01P_5/CS_B | AF3 |
| | | |
| 6 | IO_L01P_6 | AE1 |
| 6 | IO_L01N_6 | AD1 |
| 6 | IO_L02P_6/VRN_6 | AD3 |
| 6 | IO_L02N_6/VRP_6 | AD2 |
| 6 | IO_L03P_6 | AC4 |
| 6 | IO_L03N_6/VREF_6 | AC3 |
| 6 | IO_L04P_6 | AC2 |
| 6 | IO_L04N_6 | AC1 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L06P_6 | AB5 |
| 6 | IO_L06N_6 | AB4 |
| 6 | IO_L19P_6 | AB3 |
| 6 | IO_L19N_6 | AB2 |
| 6 | IO_L21P_6 | AB1 |
| 6 | IO_L21N_6/VREF_6 | AA1 |
| 6 | IO_L22P_6 | AA5 |
| 6 | IO_L22N_6 | AA6 |
| 6 | IO_L24P_6 | AA3 |
| 6 | IO_L24N_6 | AA2 |
| 6 | IO_L25P_6 | Y5 |
| 6 | IO_L25N_6 | Y6 |
| 6 | IO_L27P_6 | Y4 |
| 6 | IO_L27N_6/VREF_6 | Y3 |
| 6 | IO_L28P_6 | Y1 |
| 6 | IO_L28N_6 | W1 |
| 6 | IO_L43P_6 | W8 |
| 6 | IO_L43N_6 | W9 |
| 6 | IO_L45P_6 | W6 |
| 6 | IO_L45N_6/VREF_6 | W7 |
| 6 | IO_L46P_6 | W5 |
| 6 | IO_L46N_6 | W4 |
| 6 | IO_L48P_6 | W3 |
| 6 | IO_L48N_6 | W2 |
| 6 | IO_L49P_6 | V7 |
| 6 | IO_L49N_6 | V8 |
| 6 | IO_L51P_6 | V5 |
| 6 | IO_L51N_6/VREF_6 | V6 |
| 6 | IO_L52P_6 | V4 |
| 6 | IO_L52N_6 | V3 |
| 6 | IO_L54P_6 | V2 |
| 6 | IO_L54N_6 | V1 |
| 6 | IO_L67P_6 | U8 |
| 6 | IO_L67N_6 | T8 |
| 6 | IO_L69P_6 | U6 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L69N_6/VREF_6 | U7 |
| 6 | IO_L70P_6 | U4 |
| 6 | IO_L70N_6 | U3 |
| 6 | IO_L72P_6 | U2 |
| 6 | IO_L72N_6 | U1 |
| 6 | IO_L73P_6 | T9 |
| 6 | IO_L73N_6 | R9 |
| 6 | IO_L75P_6 | T5 |
| 6 | IO_L75N_6/VREF_6 | T6 |
| 6 | IO_L76P_6 | T4 |
| 6 | IO_L76N_6 | R4 |
| 6 | IO_L78P_6 | T2 |
| 6 | IO_L78N_6 | T1 |
| 6 | IO_L91P_6 | R7 |
| 6 | IO_L91N_6 | R8 |
| 6 | IO_L93P_6 | R5 |
| 6 | IO_L93N_6/VREF_6 | R6 |
| 6 | IO_L94P_6 | R3 |
| 6 | IO_L94N_6 | P3 |
| 6 | IO_L96P_6 | R2 |
| 6 | IO_L96N_6 | R1 |
| | | |
| 7 | IO_L96P_7 | P5 |
| 7 | IO_L96N_7 | P6 |
| 7 | IO_L94P_7 | P7 |
| 7 | IO_L94N_7 | P8 |
| 7 | IO_L93P_7/VREF_7 | N1 |
| 7 | IO_L93N_7 | N2 |
| 7 | IO_L91P_7 | N3 |
| 7 | IO_L91N_7 | N4 |
| 7 | IO_L78P_7 | N6 |
| 7 | IO_L78N_7 | N7 |
| 7 | IO_L76P_7 | N9 |
| 7 | IO_L76N_7 | N8 |
| 7 | IO_L75P_7/VREF_7 | N5 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L75N_7 | M6 |
| 7 | IO_L73P_7 | M1 |
| 7 | IO_L73N_7 | M2 |
| 7 | IO_L72P_7 | M4 |
| 7 | IO_L72N_7 | M5 |
| 7 | IO_L70P_7 | M8 |
| 7 | IO_L70N_7 | M9 |
| 7 | IO_L69P_7/VREF_7 | L1 |
| 7 | IO_L69N_7 | L2 |
| 7 | IO_L67P_7 | L3 |
| 7 | IO_L67N_7 | L4 |
| 7 | IO_L54P_7 | K1 |
| 7 | IO_L54N_7 | K2 |
| 7 | IO_L52P_7 | K4 |
| 7 | IO_L52N_7 | K5 |
| 7 | IO_L51P_7/VREF_7 | L6 |
| 7 | IO_L51N_7 | L7 |
| 7 | IO_L49P_7 | K6 |
| 7 | IO_L49N_7 | K7 |
| 7 | IO_L48P_7 | L8 |
| 7 | IO_L48N_7 | K8 |
| 7 | IO_L46P_7 | J1 |
| 7 | IO_L46N_7 | H1 |
| 7 | IO_L45P_7/VREF_7 | J2 |
| 7 | IO_L45N_7 | J3 |
| 7 | IO_L43P_7 | K3 |
| 7 | IO_L43N_7 | J4 |
| 7 | IO_L30P_7 | H3 |
| 7 | IO_L30N_7 | H4 |
| 7 | IO_L28P_7 | J5 |
| 7 | IO_L28N_7 | J6 |
| 7 | IO_L27P_7/VREF_7 | H5 |
| 7 | IO_L27N_7 | H6 |
| 7 | IO_L25P_7 | J7 |
| 7 | IO_L25N_7 | J8 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L24P_7 | G1 |
| 7 | IO_L24N_7 | F1 |
| 7 | IO_L22P_7 | G2 |
| 7 | IO_L22N_7 | G3 |
| 7 | IO_L21P_7/VREF_7 | F2 |
| 7 | IO_L21N_7 | F3 |
| 7 | IO_L19P_7 | G5 |
| 7 | IO_L19N_7 | G6 |
| 7 | IO_L06P_7 | F4 |
| 7 | IO_L06N_7 | F5 |
| 7 | IO_L04P_7 | E1 |
| 7 | IO_L04N_7 | E2 |
| 7 | IO_L03P_7/VREF_7 | D1 |
| 7 | IO_L03N_7 | C1 |
| 7 | IO_L02P_7/VRN_7 | E3 |
| 7 | IO_L02N_7/VRP_7 | E4 |
| 7 | IO_L01P_7 | D2 |
| 7 | IO_L01N_7 | D3 |
| | | |
| 0 | VCCO_0 | K13 |
| 0 | VCCO_0 | K12 |
| 0 | VCCO_0 | K11 |
| 0 | VCCO_0 | J11 |
| 0 | VCCO_0 | J10 |
| 0 | VCCO_0 | G12 |
| 0 | VCCO_0 | D7 |
| 0 | VCCO_0 | C12 |
| 1 | VCCO_1 | K17 |
| 1 | VCCO_1 | K16 |
| 1 | VCCO_1 | K15 |
| 1 | VCCO_1 | J18 |
| 1 | VCCO_1 | J17 |
| 1 | VCCO_1 | G16 |
| 1 | VCCO_1 | D21 |
| 1 | VCCO_1 | C16 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 2 | VCCO_2 | N18 |
| 2 | VCCO_2 | M25 |
| 2 | VCCO_2 | M21 |
| 2 | VCCO_2 | M18 |
| 2 | VCCO_2 | L19 |
| 2 | VCCO_2 | L18 |
| 2 | VCCO_2 | K19 |
| 2 | VCCO_2 | G24 |
| 3 | VCCO_3 | AA24 |
| 3 | VCCO_3 | V19 |
| 3 | VCCO_3 | U19 |
| 3 | VCCO_3 | U18 |
| 3 | VCCO_3 | T25 |
| 3 | VCCO_3 | T21 |
| 3 | VCCO_3 | T18 |
| 3 | VCCO_3 | R18 |
| 4 | VCCO_4 | AE16 |
| 4 | VCCO_4 | AD21 |
| 4 | VCCO_4 | AA16 |
| 4 | VCCO_4 | W18 |
| 4 | VCCO_4 | W17 |
| 4 | VCCO_4 | V17 |
| 4 | VCCO_4 | V16 |
| 4 | VCCO_4 | V15 |
| 5 | VCCO_5 | AE12 |
| 5 | VCCO_5 | AD7 |
| 5 | VCCO_5 | AA12 |
| 5 | VCCO_5 | W11 |
| 5 | VCCO_5 | W10 |
| 5 | VCCO_5 | V13 |
| 5 | VCCO_5 | V12 |
| 5 | VCCO_5 | V11 |
| 6 | VCCO_6 | AA4 |
| 6 | VCCO_6 | V9 |
| 6 | VCCO_6 | U10 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 6 | VCCO_6 | U9 |
| 6 | VCCO_6 | T10 |
| 6 | VCCO_6 | T7 |
| 6 | VCCO_6 | T3 |
| 6 | VCCO_6 | R10 |
| 7 | VCCO_7 | M10 |
| 7 | VCCO_7 | M7 |
| 7 | VCCO_7 | M3 |
| 7 | VCCO_7 | L10 |
| 7 | VCCO_7 | L9 |
| 7 | VCCO_7 | K9 |
| 7 | VCCO_7 | G4 |
| 7 | VCCO_7 | N10 |
| | | |
| NA | CCLK | AA22 |
| NA | PROG_B | C4 |
| NA | DONE | AC22 |
| NA | M0 | AC6 |
| NA | M1 | Y7 |
| NA | M2 | AE4 |
| NA | HSWAP_EN | D5 |
| NA | TCK | G20 |
| NA | TDI | H7 |
| NA | TDO | G22 |
| NA | TMS | F21 |
| NA | PWRDWN_B | AE24 |
| NA | DXN | G8 |
| NA | DXP | F7 |
| NA | VBATT | D23 |
| NA | RSVD | C24 |
| | | |
| NA | VCCAUX | AF14 |
| NA | VCCAUX | AE26 |
| NA | VCCAUX | AE2 |
| NA | VCCAUX | P26 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCAUX | P2 |
| NA | VCCAUX | C26 |
| NA | VCCAUX | C2 |
| NA | VCCAUX | B14 |
| NA | VCCINT | V18 |
| NA | VCCINT | V14 |
| NA | VCCINT | V10 |
| NA | VCCINT | U17 |
| NA | VCCINT | U16 |
| NA | VCCINT | U15 |
| NA | VCCINT | U14 |
| NA | VCCINT | U13 |
| NA | VCCINT | U12 |
| NA | VCCINT | U11 |
| NA | VCCINT | T17 |
| NA | VCCINT | T11 |
| NA | VCCINT | R17 |
| NA | VCCINT | R11 |
| NA | VCCINT | P18 |
| NA | VCCINT | P17 |
| NA | VCCINT | P11 |
| NA | VCCINT | P10 |
| NA | VCCINT | N17 |
| NA | VCCINT | N11 |
| NA | VCCINT | M17 |
| NA | VCCINT | M11 |
| NA | VCCINT | L17 |
| NA | VCCINT | L16 |
| NA | VCCINT | L15 |
| NA | VCCINT | L14 |
| NA | VCCINT | L13 |
| NA | VCCINT | L12 |
| NA | VCCINT | L11 |
| NA | VCCINT | K18 |
| NA | VCCINT | K14 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|-------------------|
| NA | VCCINT | K10 |
| NA | GND | AG27 ¹ |
| NA | GND | AG26 ¹ |
| NA | GND | AG14 |
| NA | GND | AG2 ¹ |
| NA | GND | AG1 ¹ |
| NA | GND | AF27 ¹ |
| NA | GND | AF26 |
| NA | GND | AF20 |
| NA | GND | AF8 |
| NA | GND | AF2 |
| NA | GND | AF1 ¹ |
| NA | GND | AE25 |
| NA | GND | AE3 |
| NA | GND | AD24 |
| NA | GND | AD14 |
| NA | GND | AD4 |
| NA | GND | AC23 |
| NA | GND | AC17 |
| NA | GND | AC11 |
| NA | GND | AC5 |
| NA | GND | AB22 |
| NA | GND | AB6 |
| NA | GND | AA21 |
| NA | GND | AA7 |
| NA | GND | Y26 |
| NA | GND | Y20 |
| NA | GND | Y8 |
| NA | GND | Y2 |
| NA | GND | W14 |
| NA | GND | U23 |
| NA | GND | U5 |
| NA | GND | T16 |
| NA | GND | T15 |
| NA | GND | T14 |

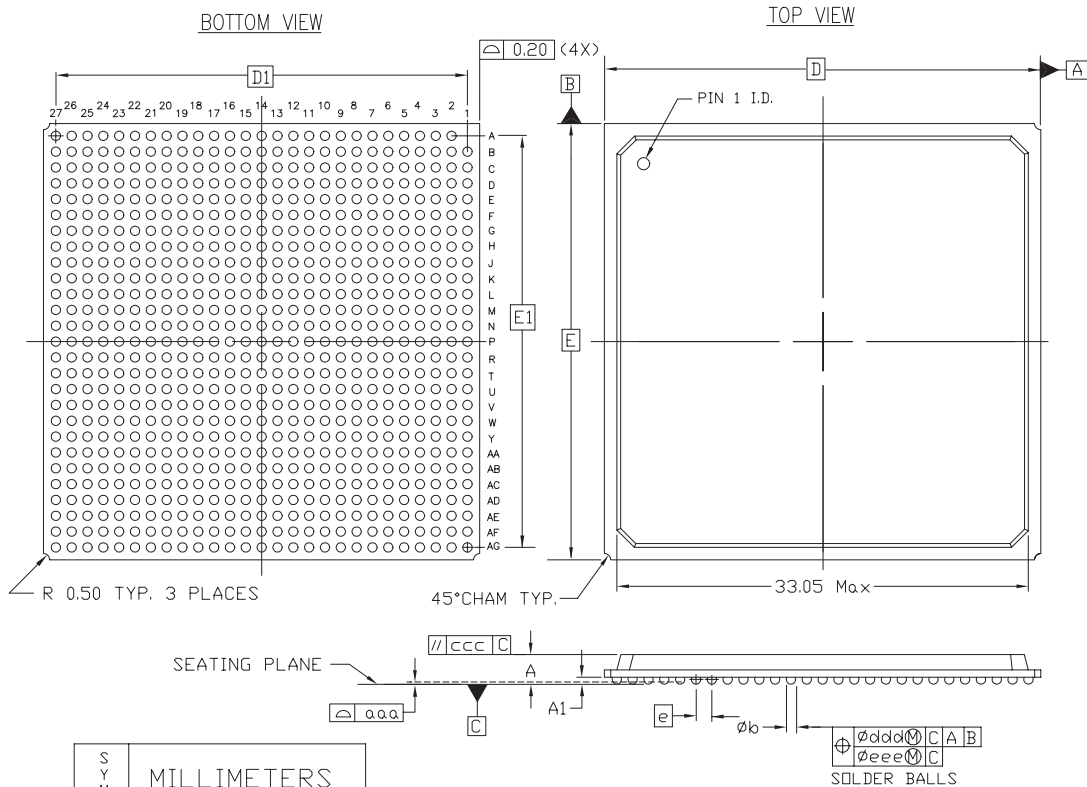
Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | T13 |
| NA | GND | T12 |
| NA | GND | R16 |
| NA | GND | R15 |
| NA | GND | R14 |
| NA | GND | R13 |
| NA | GND | R12 |
| NA | GND | P27 |
| NA | GND | P24 |
| NA | GND | P19 |
| NA | GND | P16 |
| NA | GND | P15 |
| NA | GND | P14 |
| NA | GND | P13 |
| NA | GND | P12 |
| NA | GND | P9 |
| NA | GND | P4 |
| NA | GND | P1 |
| NA | GND | N16 |
| NA | GND | N15 |
| NA | GND | N14 |
| NA | GND | N13 |
| NA | GND | N12 |
| NA | GND | M16 |
| NA | GND | M15 |
| NA | GND | M14 |
| NA | GND | M13 |
| NA | GND | M12 |
| NA | GND | L23 |
| NA | GND | L5 |
| NA | GND | J14 |
| NA | GND | H26 |
| NA | GND | H20 |
| NA | GND | H8 |
| NA | GND | H2 |

Table 79: BG728 BGA and CG717 CGA— XQR2V3000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------------|
| NA | GND | G21 |
| NA | GND | G7 |
| NA | GND | F22 |
| NA | GND | F6 |
| NA | GND | E23 |
| NA | GND | E17 |
| NA | GND | E11 |
| NA | GND | E5 |
| NA | GND | D24 |
| NA | GND | D14 |
| NA | GND | D4 |
| NA | GND | C25 |
| NA | GND | C3 |
| NA | GND | B27 ¹ |
| NA | GND | B26 |
| NA | GND | B20 |
| NA | GND | B8 |
| NA | GND | B2 |
| NA | GND | B1 ¹ |
| NA | GND | A27 ¹ |
| NA | GND | A26 ¹ |
| NA | GND | A14 |
| NA | GND | A2 |

BG728 Standard BGA Package Specifications (1.27mm pitch)



| SYMBOL | MILLIMETERS | | |
|--------------------------------|-------------------|-------------------|------|
| | MIN. | NOM. | MAX. |
| A | $\sqrt{\text{H}}$ | 2.33 | 2.60 |
| A ₁ | 0.50 | 0.60 | 0.70 |
| D/E | 35.00 BSC | | |
| D ₁ /E ₁ | 33.02 REF | | |
| e | 1.27BSC | | |
| øb | 0.60 | 0.75 | 0.90 |
| aaa | $\sqrt{\text{H}}$ | $\sqrt{\text{H}}$ | 0.20 |
| ccc | $\sqrt{\text{H}}$ | $\sqrt{\text{H}}$ | 0.35 |
| ddd | $\sqrt{\text{H}}$ | $\sqrt{\text{H}}$ | 0.30 |
| eee | $\sqrt{\text{H}}$ | $\sqrt{\text{H}}$ | 0.15 |
| M | 27 | | |

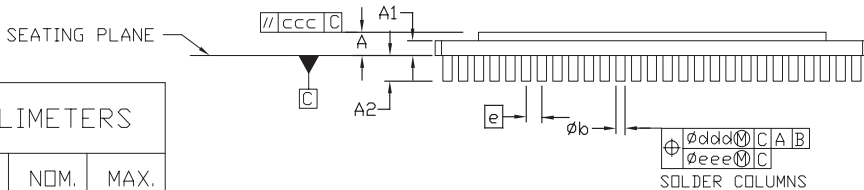
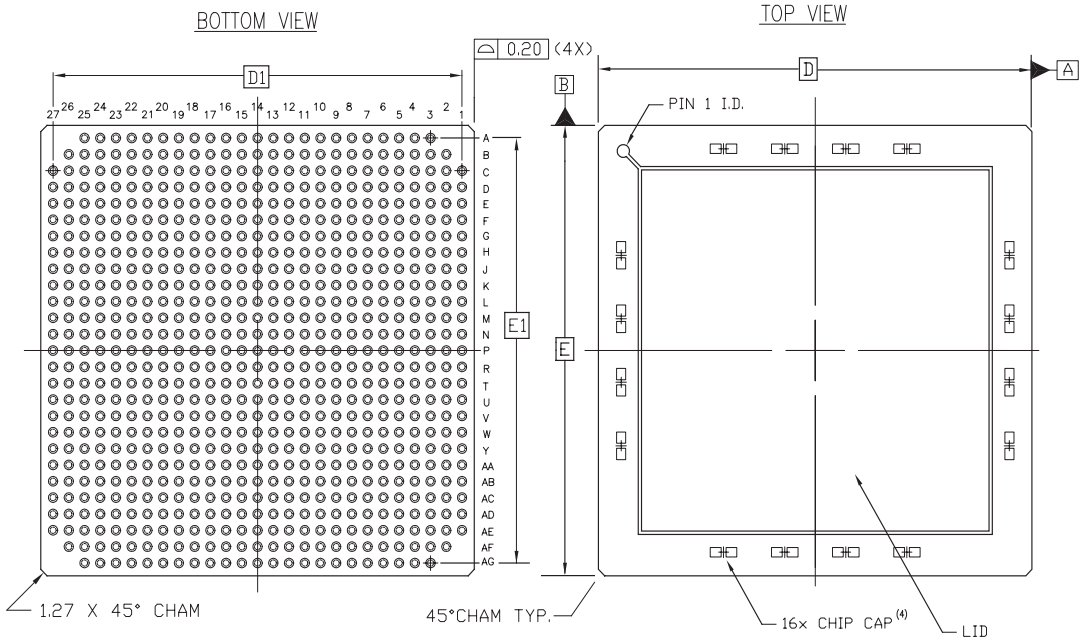
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAR-1
4. NO SOLDER BALL AND LAND ON A₁.

Figure 54: BG728 Standard BGA Package Specifications

CG717 Ceramic Column Grid Array (CGA) Package Specifications (1.27mm pitch)

CG717 (LGA WITH CAST SOLDER COLUMN)



| SYMBOL | MILLIMETERS | | |
|-------------------|---------------------|---------------------|------|
| | MIN. | NOM. | MAX. |
| A | $\sqrt{\text{---}}$ | 3.00 | 3.30 |
| A ₁ | 2.30 | 2.56 | 2.82 |
| A ₂ | 2.10 | 2.20 | 2.30 |
| D/E ₁ | 35.00 BSC | | |
| D ₁ /E | 33.00 REF | | |
| e | 1.27BSC | | |
| ϕb | 0.51 | 0.54 | 0.57 |
| ccc | $\sqrt{\text{---}}$ | $\sqrt{\text{---}}$ | 0.35 |
| ddd | $\sqrt{\text{---}}$ | $\sqrt{\text{---}}$ | 0.30 |
| eee | $\sqrt{\text{---}}$ | $\sqrt{\text{---}}$ | 0.15 |
| M | 27 | | |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. LEAD FINISH: HIGH TEMP. SOLDER Pb(90%)/Sn(10%)
4. 0402 CHIP CAPACITORS OPTIONAL

Figure 55: CG717 Ceramic CGA Package Specifications

CF1144 Ceramic Flip-Chip Fine-Pitch CGA Package

As shown in [Table 81](#), The XQR2V6000 QPro Virtex-II device is available in the CF1144 flip-chip fine-pitch CGA package. Pins for this package are the same as the FF1152, except for those pins shown in [Table 80](#) have been removed. Following this table are the **CF1144 Ceramic Flip-Chip Fine-Pitch CGA Package Specifications (1.00mm pitch)**. The CF1144 has eight fewer GND pins than the FF1152. The FF1152 GND Pin numbers missing on the CF1144 are shown in [Table 80](#).

Table 80: FF1152 GND Pins not available on the CF1144

| FF1152 GND Pin Numbers | | | |
|------------------------|-----|-----|------|
| A2 | A33 | AN1 | AN34 |
| B1 | B34 | AP2 | AP33 |

1. Physical pin does not exist for CF1144 package

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L01N_0 | D29 |
| 0 | IO_L01P_0 | C29 |
| 0 | IO_L02N_0 | H26 |
| 0 | IO_L02P_0 | G26 |
| 0 | IO_L03N_0/VRP_0 | E28 |
| 0 | IO_L03P_0/VRN_0 | E27 |
| 0 | IO_L04N_0/VREF_0 | F25 |
| 0 | IO_L04P_0 | F26 |
| 0 | IO_L05N_0 | H25 |
| 0 | IO_L05P_0 | H24 |
| 0 | IO_L06N_0 | E26 |
| 0 | IO_L06P_0 | F27 |
| 0 | IO_L19N_0 | B32 |
| 0 | IO_L19P_0 | C33 |
| 0 | IO_L20N_0 | J24 |
| 0 | IO_L20P_0 | J23 |
| 0 | IO_L21N_0 | C27 |
| 0 | IO_L21P_0/VREF_0 | C28 |
| 0 | IO_L22N_0 | B30 |
| 0 | IO_L22P_0 | B31 |
| 0 | IO_L23N_0 | K23 |
| 0 | IO_L23P_0 | K22 |
| 0 | IO_L24N_0 | C26 |
| 0 | IO_L24P_0 | D27 |
| 0 | IO_L25N_0 | A30 |
| 0 | IO_L25P_0 | A31 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L26N_0 | G24 |
| 0 | IO_L26P_0 | G25 |
| 0 | IO_L27N_0 | E25 |
| 0 | IO_L27P_0/VREF_0 | E24 |
| 0 | IO_L28N_0 | D25 |
| 0 | IO_L28P_0 | D26 |
| 0 | IO_L29N_0 | H23 |
| 0 | IO_L29P_0 | H22 |
| 0 | IO_L30N_0 | F23 |
| 0 | IO_L30P_0 | F24 |
| 0 | IO_L49N_0 | B28 |
| 0 | IO_L49P_0 | B29 |
| 0 | IO_L50N_0 | J22 |
| 0 | IO_L50P_0 | J21 |
| 0 | IO_L51N_0 | A28 |
| 0 | IO_L51P_0/VREF_0 | A29 |
| 0 | IO_L52N_0 | A26 |
| 0 | IO_L52P_0 | B27 |
| 0 | IO_L53N_0 | C24 |
| 0 | IO_L53P_0 | D24 |
| 0 | IO_L54N_0 | D22 |
| 0 | IO_L54P_0 | D23 |
| 0 | IO_L60N_0 | B25 |
| 0 | IO_L60P_0 | B26 |
| 0 | IO_L67N_0 | B23 |
| 0 | IO_L67P_0 | B24 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L68N_0 | G22 |
| 0 | IO_L68P_0 | G23 |
| 0 | IO_L69N_0 | F22 |
| 0 | IO_L69P_0/VREF_0 | F21 |
| 0 | IO_L70N_0 | A23 |
| 0 | IO_L70P_0 | A24 |
| 0 | IO_L71N_0 | K21 |
| 0 | IO_L71P_0 | K20 |
| 0 | IO_L72N_0 | C22 |
| 0 | IO_L72P_0 | C23 |
| 0 | IO_L73N_0 | E21 |
| 0 | IO_L73P_0 | E22 |
| 0 | IO_L74N_0 | H21 |
| 0 | IO_L74P_0 | H20 |
| 0 | IO_L75N_0 | G20 |
| 0 | IO_L75P_0/VREF_0 | F20 |
| 0 | IO_L76N_0 | B21 |
| 0 | IO_L76P_0 | B22 |
| 0 | IO_L77N_0 | J20 |
| 0 | IO_L77P_0 | K19 |
| 0 | IO_L78N_0 | D20 |
| 0 | IO_L78P_0 | D21 |
| 0 | IO_L79N_0 | A21 |
| 0 | IO_L79P_0 | A22 |
| 0 | IO_L80N_0 | L19 |
| 0 | IO_L80P_0 | L18 |
| 0 | IO_L81N_0 | B19 |
| 0 | IO_L81P_0/VREF_0 | A20 |
| 0 | IO_L82N_0 | A18 |
| 0 | IO_L82P_0 | B18 |
| 0 | IO_L83N_0 | H19 |
| 0 | IO_L83P_0 | H18 |
| 0 | IO_L84N_0 | C20 |
| 0 | IO_L84P_0 | C21 |
| 0 | IO_L91N_0/VREF_0 | D19 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 0 | IO_L91P_0 | D18 |
| 0 | IO_L92N_0 | G18 |
| 0 | IO_L92P_0 | G19 |
| 0 | IO_L93N_0 | F18 |
| 0 | IO_L93P_0 | F19 |
| 0 | IO_L94N_0/VREF_0 | C19 |
| 0 | IO_L94P_0 | C18 |
| 0 | IO_L95N_0/GCLK7P | K18 |
| 0 | IO_L95P_0/GCLK6S | J18 |
| 0 | IO_L96N_0/GCLK5P | E19 |
| 0 | IO_L96P_0/GCLK4S | E18 |
| | | |
| 1 | IO_L96N_1/GCLK3P | E17 |
| 1 | IO_L96P_1/GCLK2S | E16 |
| 1 | IO_L95N_1/GCLK1P | H17 |
| 1 | IO_L95P_1/GCLK0S | H16 |
| 1 | IO_L94N_1 | D17 |
| 1 | IO_L94P_1/VREF_1 | D16 |
| 1 | IO_L93N_1 | F16 |
| 1 | IO_L93P_1 | F17 |
| 1 | IO_L92N_1 | G16 |
| 1 | IO_L92P_1 | G17 |
| 1 | IO_L91N_1 | C16 |
| 1 | IO_L91P_1/VREF_1 | C15 |
| 1 | IO_L84N_1 | D14 |
| 1 | IO_L84P_1 | D15 |
| 1 | IO_L83N_1 | J17 |
| 1 | IO_L83P_1 | K17 |
| 1 | IO_L82N_1 | B17 |
| 1 | IO_L82P_1 | A17 |
| 1 | IO_L81N_1/VREF_1 | A15 |
| 1 | IO_L81P_1 | B16 |
| 1 | IO_L80N_1 | L17 |
| 1 | IO_L80P_1 | L16 |
| 1 | IO_L79N_1 | A13 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L79P_1 | A14 |
| 1 | IO_L78N_1 | C13 |
| 1 | IO_L78P_1 | C14 |
| 1 | IO_L77N_1 | K16 |
| 1 | IO_L77P_1 | K15 |
| 1 | IO_L76N_1 | B13 |
| 1 | IO_L76P_1 | B14 |
| 1 | IO_L75N_1/VREF_1 | F15 |
| 1 | IO_L75P_1 | G15 |
| 1 | IO_L74N_1 | H15 |
| 1 | IO_L74P_1 | H14 |
| 1 | IO_L73N_1 | A11 |
| 1 | IO_L73P_1 | A12 |
| 1 | IO_L72N_1 | E13 |
| 1 | IO_L72P_1 | E14 |
| 1 | IO_L71N_1 | J15 |
| 1 | IO_L71P_1 | J14 |
| 1 | IO_L70N_1 | D12 |
| 1 | IO_L70P_1 | D13 |
| 1 | IO_L69N_1/VREF_1 | F14 |
| 1 | IO_L69P_1 | F13 |
| 1 | IO_L68N_1 | C11 |
| 1 | IO_L68P_1 | C12 |
| 1 | IO_L67N_1 | B11 |
| 1 | IO_L67P_1 | B12 |
| 1 | IO_L60N_1 | F11 |
| 1 | IO_L60P_1 | F12 |
| 1 | IO_L54N_1 | D10 |
| 1 | IO_L54P_1 | D11 |
| 1 | IO_L53N_1 | G12 |
| 1 | IO_L53P_1 | G13 |
| 1 | IO_L52N_1 | B9 |
| 1 | IO_L52P_1 | B10 |
| 1 | IO_L51N_1/VREF_1 | B8 |
| 1 | IO_L51P_1 | A9 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L50N_1 | K14 |
| 1 | IO_L50P_1 | K13 |
| 1 | IO_L49N_1 | A6 |
| 1 | IO_L49P_1 | A7 |
| 1 | IO_L30N_1 | D9 |
| 1 | IO_L30P_1 | C9 |
| 1 | IO_L29N_1 | H13 |
| 1 | IO_L29P_1 | H12 |
| 1 | IO_L28N_1 | C7 |
| 1 | IO_L28P_1 | C8 |
| 1 | IO_L27N_1/VREF_1 | E11 |
| 1 | IO_L27P_1 | E10 |
| 1 | IO_L26N_1 | J13 |
| 1 | IO_L26P_1 | K12 |
| 1 | IO_L25N_1 | B6 |
| 1 | IO_L25P_1 | B7 |
| 1 | IO_L24N_1 | E8 |
| 1 | IO_L24P_1 | E9 |
| 1 | IO_L23N_1 | G10 |
| 1 | IO_L23P_1 | G11 |
| 1 | IO_L22N_1 | A4 |
| 1 | IO_L22P_1 | A5 |
| 1 | IO_L21N_1/VREF_1 | F10 |
| 1 | IO_L21P_1 | G9 |
| 1 | IO_L20N_1 | J12 |
| 1 | IO_L20P_1 | J11 |
| 1 | IO_L19N_1 | B4 |
| 1 | IO_L19P_1 | B5 |
| 1 | IO_L06N_1 | D6 |
| 1 | IO_L06P_1 | C6 |
| 1 | IO_L05N_1 | H11 |
| 1 | IO_L05P_1 | J10 |
| 1 | IO_L04N_1 | D8 |
| 1 | IO_L04P_1/VREF_1 | E7 |
| 1 | IO_L03N_1/VRP_1 | F9 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 1 | IO_L03P_1/VRN_1 | F8 |
| 1 | IO_L02N_1 | H10 |
| 1 | IO_L02P_1 | H9 |
| 1 | IO_L01N_1 | C2 |
| 1 | IO_L01P_1 | B3 |
| | | |
| 2 | IO_L01N_2 | E2 |
| 2 | IO_L01P_2 | D2 |
| 2 | IO_L02N_2/VRP_2 | K11 |
| 2 | IO_L02P_2/VRN_2 | K10 |
| 2 | IO_L03N_2 | F5 |
| 2 | IO_L03P_2/VREF_2 | G5 |
| 2 | IO_L04N_2 | E3 |
| 2 | IO_L04P_2 | D3 |
| 2 | IO_L05N_2 | J9 |
| 2 | IO_L05P_2 | K9 |
| 2 | IO_L06N_2 | F4 |
| 2 | IO_L06P_2 | E4 |
| 2 | IO_L19N_2 | E1 |
| 2 | IO_L19P_2 | D1 |
| 2 | IO_L20N_2 | J8 |
| 2 | IO_L20P_2 | K8 |
| 2 | IO_L21N_2 | H7 |
| 2 | IO_L21P_2/VREF_2 | J7 |
| 2 | IO_L22N_2 | H6 |
| 2 | IO_L22P_2 | G6 |
| 2 | IO_L23N_2 | L10 |
| 2 | IO_L23P_2 | L9 |
| 2 | IO_L24N_2 | G3 |
| 2 | IO_L24P_2 | F3 |
| 2 | IO_L25N_2 | G2 |
| 2 | IO_L25P_2 | F2 |
| 2 | IO_L26N_2 | M10 |
| 2 | IO_L26P_2 | N10 |
| 2 | IO_L27N_2 | J6 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L27P_2/VREF_2 | K6 |
| 2 | IO_L28N_2 | J5 |
| 2 | IO_L28P_2 | H5 |
| 2 | IO_L29N_2 | L7 |
| 2 | IO_L29P_2 | K7 |
| 2 | IO_L30N_2 | J4 |
| 2 | IO_L30P_2 | H4 |
| 2 | IO_L43N_2 | G1 |
| 2 | IO_L43P_2 | F1 |
| 2 | IO_L44N_2 | L8 |
| 2 | IO_L44P_2 | M8 |
| 2 | IO_L45N_2 | J1 |
| 2 | IO_L45P_2/VREF_2 | H2 |
| 2 | IO_L46N_2 | J3 |
| 2 | IO_L46P_2 | H3 |
| 2 | IO_L47N_2 | M9 |
| 2 | IO_L47P_2 | N9 |
| 2 | IO_L48N_2 | L5 |
| 2 | IO_L48P_2 | K5 |
| 2 | IO_L49N_2 | K2 |
| 2 | IO_L49P_2 | J2 |
| 2 | IO_L50N_2 | N7 |
| 2 | IO_L50P_2 | M7 |
| 2 | IO_L51N_2 | L6 |
| 2 | IO_L51P_2/VREF_2 | M6 |
| 2 | IO_L52N_2 | M3 |
| 2 | IO_L52P_2 | L3 |
| 2 | IO_L53N_2 | L4 |
| 2 | IO_L53P_2 | K4 |
| 2 | IO_L54N_2 | N4 |
| 2 | IO_L54P_2 | M4 |
| 2 | IO_L67N_2 | M2 |
| 2 | IO_L67P_2 | L2 |
| 2 | IO_L68N_2 | N8 |
| 2 | IO_L68P_2 | P8 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L69N_2 | N6 |
| 2 | IO_L69P_2/VREF_2 | P6 |
| 2 | IO_L70N_2 | P5 |
| 2 | IO_L70P_2 | N5 |
| 2 | IO_L71N_2 | P10 |
| 2 | IO_L71P_2 | R10 |
| 2 | IO_L72N_2 | P3 |
| 2 | IO_L72P_2 | N3 |
| 2 | IO_L73N_2 | M1 |
| 2 | IO_L73P_2 | L1 |
| 2 | IO_L74N_2 | P9 |
| 2 | IO_L74P_2 | R9 |
| 2 | IO_L75N_2 | P2 |
| 2 | IO_L75P_2/VREF_2 | N2 |
| 2 | IO_L76N_2 | R4 |
| 2 | IO_L76P_2 | P4 |
| 2 | IO_L77N_2 | R8 |
| 2 | IO_L77P_2 | T8 |
| 2 | IO_L78N_2 | T3 |
| 2 | IO_L78P_2 | R3 |
| 2 | IO_L79N_2 | P1 |
| 2 | IO_L79P_2 | N1 |
| 2 | IO_L80N_2 | T11 |
| 2 | IO_L80P_2 | U11 |
| 2 | IO_L81N_2 | R7 |
| 2 | IO_L81P_2/VREF_2 | R6 |
| 2 | IO_L82N_2 | U5 |
| 2 | IO_L82P_2 | T5 |
| 2 | IO_L83N_2 | T10 |
| 2 | IO_L83P_2 | U10 |
| 2 | IO_L84N_2 | U4 |
| 2 | IO_L84P_2 | T4 |
| 2 | IO_L91N_2 | T2 |
| 2 | IO_L91P_2 | R1 |
| 2 | IO_L92N_2 | U7 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 2 | IO_L92P_2 | T7 |
| 2 | IO_L93N_2 | T6 |
| 2 | IO_L93P_2/VREF_2 | U6 |
| 2 | IO_L94N_2 | U1 |
| 2 | IO_L94P_2 | U2 |
| 2 | IO_L95N_2 | U9 |
| 2 | IO_L95P_2 | U8 |
| 2 | IO_L96N_2 | U3 |
| 2 | IO_L96P_2 | V4 |
| | | |
| 3 | IO_L96N_3 | V6 |
| 3 | IO_L96P_3 | W6 |
| 3 | IO_L95N_3 | V5 |
| 3 | IO_L95P_3 | W5 |
| 3 | IO_L94N_3 | V7 |
| 3 | IO_L94P_3 | W7 |
| 3 | IO_L93N_3/VREF_3 | V10 |
| 3 | IO_L93P_3 | W10 |
| 3 | IO_L92N_3 | V1 |
| 3 | IO_L92P_3 | V2 |
| 3 | IO_L91N_3 | W3 |
| 3 | IO_L91P_3 | Y3 |
| 3 | IO_L84N_3 | V9 |
| 3 | IO_L84P_3 | V8 |
| 3 | IO_L83N_3 | W4 |
| 3 | IO_L83P_3 | Y4 |
| 3 | IO_L82N_3 | W11 |
| 3 | IO_L82P_3 | V11 |
| 3 | IO_L81N_3/VREF_3 | W8 |
| 3 | IO_L81P_3 | Y8 |
| 3 | IO_L80N_3 | W2 |
| 3 | IO_L80P_3 | Y1 |
| 3 | IO_L79N_3 | AA3 |
| 3 | IO_L79P_3 | AB3 |
| 3 | IO_L78N_3 | Y6 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 3 | IO_L78P_3 | AA6 |
| 3 | IO_L77N_3 | AA4 |
| 3 | IO_L77P_3 | AB4 |
| 3 | IO_L76N_3 | Y7 |
| 3 | IO_L76P_3 | AA8 |
| 3 | IO_L75N_3/VREF_3 | Y10 |
| 3 | IO_L75P_3 | AA10 |
| 3 | IO_L74N_3 | AA1 |
| 3 | IO_L74P_3 | AB1 |
| 3 | IO_L73N_3 | AA5 |
| 3 | IO_L73P_3 | AB5 |
| 3 | IO_L72N_3 | AA9 |
| 3 | IO_L72P_3 | Y9 |
| 3 | IO_L71N_3 | AA2 |
| 3 | IO_L71P_3 | AB2 |
| 3 | IO_L70N_3 | AB6 |
| 3 | IO_L70P_3 | AC6 |
| 3 | IO_L69N_3/VREF_3 | AD1 |
| 3 | IO_L69P_3 | AC1 |
| 3 | IO_L68N_3 | AC3 |
| 3 | IO_L68P_3 | AD3 |
| 3 | IO_L67N_3 | AC4 |
| 3 | IO_L67P_3 | AD4 |
| 3 | IO_L54N_3 | AB7 |
| 3 | IO_L54P_3 | AC7 |
| 3 | IO_L53N_3 | AC2 |
| 3 | IO_L53P_3 | AD2 |
| 3 | IO_L52N_3 | AC8 |
| 3 | IO_L52P_3 | AB8 |
| 3 | IO_L51N_3/VREF_3 | AB10 |
| 3 | IO_L51P_3 | AC10 |
| 3 | IO_L50N_3 | AD5 |
| 3 | IO_L50P_3 | AE5 |
| 3 | IO_L49N_3 | AE4 |
| 3 | IO_L49P_3 | AF4 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 3 | IO_L48N_3 | AB9 |
| 3 | IO_L48P_3 | AC9 |
| 3 | IO_L47N_3 | AE2 |
| 3 | IO_L47P_3 | AF1 |
| 3 | IO_L46N_3 | AD6 |
| 3 | IO_L46P_3 | AE6 |
| 3 | IO_L45N_3/VREF_3 | AD9 |
| 3 | IO_L45P_3 | AE9 |
| 3 | IO_L44N_3 | AF2 |
| 3 | IO_L44P_3 | AG2 |
| 3 | IO_L43N_3 | AF3 |
| 3 | IO_L43P_3 | AG3 |
| 3 | IO_L30N_3 | AD7 |
| 3 | IO_L30P_3 | AE7 |
| 3 | IO_L29N_3 | AF5 |
| 3 | IO_L29P_3 | AG5 |
| 3 | IO_L28N_3 | AE8 |
| 3 | IO_L28P_3 | AD8 |
| 3 | IO_L27N_3/VREF_3 | AF8 |
| 3 | IO_L27P_3 | AF9 |
| 3 | IO_L26N_3 | AH1 |
| 3 | IO_L26P_3 | AJ1 |
| 3 | IO_L25N_3 | AG4 |
| 3 | IO_L25P_3 | AH5 |
| 3 | IO_L24N_3 | AF6 |
| 3 | IO_L24P_3 | AG6 |
| 3 | IO_L23N_3 | AH3 |
| 3 | IO_L23P_3 | AJ3 |
| 3 | IO_L22N_3 | AF7 |
| 3 | IO_L22P_3 | AG7 |
| 3 | IO_L21N_3/VREF_3 | AL1 |
| 3 | IO_L21P_3 | AK1 |
| 3 | IO_L20N_3 | AH2 |
| 3 | IO_L20P_3 | AJ2 |
| 3 | IO_L19N_3 | AJ4 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 3 | IO_L19P_3 | AK4 |
| 3 | IO_L06N_3 | AE10 |
| 3 | IO_L06P_3 | AD10 |
| 3 | IO_L05N_3 | AK2 |
| 3 | IO_L05P_3 | AL2 |
| 3 | IO_L04N_3 | AH6 |
| 3 | IO_L04P_3 | AJ5 |
| 3 | IO_L03N_3/VREF_3 | AE11 |
| 3 | IO_L03P_3 | AF11 |
| 3 | IO_L02N_3/VRP_3 | AK3 |
| 3 | IO_L02P_3/VRN_3 | AL3 |
| 3 | IO_L01N_3 | AF10 |
| 3 | IO_L01P_3 | AG9 |
| | | |
| 4 | IO_L01N_4/DOUT | AM4 |
| 4 | IO_L01P_4/INIT_B | AL5 |
| 4 | IO_L02N_4/D0 | AG10 |
| 4 | IO_L02P_4/D1 | AH11 |
| 4 | IO_L03N_4/D2/ALT_VRP_4 | AK7 |
| 4 | IO_L03P_4/D3/ALT_VRN_4 | AK8 |
| 4 | IO_L04N_4/VREF_4 | AL6 |
| 4 | IO_L04P_4 | AM6 |
| 4 | IO_L05N_4/VRP_4 | AK9 |
| 4 | IO_L05P_4/VRN_4 | AJ8 |
| 4 | IO_L06N_4 | AM8 |
| 4 | IO_L06P_4 | AM7 |
| 4 | IO_L19N_4 | AN3 |
| 4 | IO_L19P_4 | AM2 |
| 4 | IO_L20N_4 | AJ10 |
| 4 | IO_L20P_4 | AJ9 |
| 4 | IO_L21N_4 | AH9 |
| 4 | IO_L21P_4/VREF_4 | AH10 |
| 4 | IO_L22N_4 | AN5 |
| 4 | IO_L22P_4 | AN4 |
| 4 | IO_L23N_4 | AE12 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L23P_4 | AE13 |
| 4 | IO_L24N_4 | AM9 |
| 4 | IO_L24P_4 | AL8 |
| 4 | IO_L25N_4 | AP5 |
| 4 | IO_L25P_4 | AP4 |
| 4 | IO_L26N_4 | AG11 |
| 4 | IO_L26P_4 | AG12 |
| 4 | IO_L27N_4 | AN7 |
| 4 | IO_L27P_4/VREF_4 | AN6 |
| 4 | IO_L28N_4 | AL10 |
| 4 | IO_L28P_4 | AL9 |
| 4 | IO_L29N_4 | AF12 |
| 4 | IO_L29P_4 | AF13 |
| 4 | IO_L30N_4 | AK10 |
| 4 | IO_L30P_4 | AK11 |
| 4 | IO_L49N_4 | AP7 |
| 4 | IO_L49P_4 | AP6 |
| 4 | IO_L50N_4 | AH13 |
| 4 | IO_L50P_4 | AH12 |
| 4 | IO_L51N_4 | AJ11 |
| 4 | IO_L51P_4/VREF_4 | AJ12 |
| 4 | IO_L52N_4 | AP9 |
| 4 | IO_L52P_4 | AN8 |
| 4 | IO_L53N_4 | AG13 |
| 4 | IO_L53P_4 | AG14 |
| 4 | IO_L54N_4 | AM11 |
| 4 | IO_L54P_4 | AL11 |
| 4 | IO_L60N_4 | AN10 |
| 4 | IO_L60P_4 | AN9 |
| 4 | IO_L67N_4 | AN12 |
| 4 | IO_L67P_4 | AN11 |
| 4 | IO_L68N_4 | AE14 |
| 4 | IO_L68P_4 | AE15 |
| 4 | IO_L69N_4 | AJ13 |
| 4 | IO_L69P_4/VREF_4 | AJ14 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L70N_4 | AL13 |
| 4 | IO_L70P_4 | AL12 |
| 4 | IO_L71N_4 | AF14 |
| 4 | IO_L71P_4 | AF15 |
| 4 | IO_L72N_4 | AM13 |
| 4 | IO_L72P_4 | AM12 |
| 4 | IO_L73N_4 | AP12 |
| 4 | IO_L73P_4 | AP11 |
| 4 | IO_L74N_4 | AG15 |
| 4 | IO_L74P_4 | AG16 |
| 4 | IO_L75N_4 | AN14 |
| 4 | IO_L75P_4/VREF_4 | AN13 |
| 4 | IO_L76N_4 | AP14 |
| 4 | IO_L76P_4 | AP13 |
| 4 | IO_L77N_4 | AD16 |
| 4 | IO_L77P_4 | AD17 |
| 4 | IO_L78N_4 | AK14 |
| 4 | IO_L78P_4 | AK13 |
| 4 | IO_L79N_4 | AN16 |
| 4 | IO_L79P_4 | AP15 |
| 4 | IO_L80N_4 | AE16 |
| 4 | IO_L80P_4 | AE17 |
| 4 | IO_L81N_4 | AH15 |
| 4 | IO_L81P_4/VREF_4 | AJ15 |
| 4 | IO_L82N_4 | AP17 |
| 4 | IO_L82P_4 | AN17 |
| 4 | IO_L83N_4 | AH17 |
| 4 | IO_L83P_4 | AH16 |
| 4 | IO_L84N_4 | AL15 |
| 4 | IO_L84P_4 | AL14 |
| 4 | IO_L91N_4/VREF_4 | AL16 |
| 4 | IO_L91P_4 | AL17 |
| 4 | IO_L92N_4 | AJ17 |
| 4 | IO_L92P_4 | AJ16 |
| 4 | IO_L93N_4 | AM15 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 4 | IO_L93P_4 | AM14 |
| 4 | IO_L94N_4/VREF_4 | AM16 |
| 4 | IO_L94P_4 | AM17 |
| 4 | IO_L95N_4/GCLK3S | AF17 |
| 4 | IO_L95P_4/GCLK2P | AG17 |
| 4 | IO_L96N_4/GCLK1S | AK16 |
| 4 | IO_L96P_4/GCLK0P | AK17 |
| | | |
| 5 | IO_L96N_5/GCLK7S | AK18 |
| 5 | IO_L96P_5/GCLK6P | AK19 |
| 5 | IO_L95N_5/GCLK5S | AG18 |
| 5 | IO_L95P_5/GCLK4P | AF18 |
| 5 | IO_L94N_5 | AL18 |
| 5 | IO_L94P_5/VREF_5 | AL19 |
| 5 | IO_L93N_5 | AJ19 |
| 5 | IO_L93P_5 | AJ18 |
| 5 | IO_L92N_5 | AH19 |
| 5 | IO_L92P_5 | AH18 |
| 5 | IO_L91N_5 | AM19 |
| 5 | IO_L91P_5/VREF_5 | AM20 |
| 5 | IO_L84N_5 | AL21 |
| 5 | IO_L84P_5 | AL20 |
| 5 | IO_L83N_5 | AM22 |
| 5 | IO_L83P_5 | AM21 |
| 5 | IO_L82N_5 | AN18 |
| 5 | IO_L82P_5 | AP18 |
| 5 | IO_L81N_5/VREF_5 | AP20 |
| 5 | IO_L81P_5 | AN19 |
| 5 | IO_L80N_5 | AE18 |
| 5 | IO_L80P_5 | AE19 |
| 5 | IO_L79N_5 | AP22 |
| 5 | IO_L79P_5 | AP21 |
| 5 | IO_L78N_5 | AK22 |
| 5 | IO_L78P_5 | AK21 |
| 5 | IO_L77N_5 | AD18 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 5 | IO_L77P_5 | AD19 |
| 5 | IO_L76N_5 | AN22 |
| 5 | IO_L76P_5 | AN21 |
| 5 | IO_L75N_5/VREF_5 | AJ20 |
| 5 | IO_L75P_5 | AH20 |
| 5 | IO_L74N_5 | AG19 |
| 5 | IO_L74P_5 | AG20 |
| 5 | IO_L73N_5 | AP24 |
| 5 | IO_L73P_5 | AP23 |
| 5 | IO_L72N_5 | AL23 |
| 5 | IO_L72P_5 | AL22 |
| 5 | IO_L71N_5 | AF20 |
| 5 | IO_L71P_5 | AF21 |
| 5 | IO_L70N_5 | AM24 |
| 5 | IO_L70P_5 | AM23 |
| 5 | IO_L69N_5/VREF_5 | AJ21 |
| 5 | IO_L69P_5 | AJ22 |
| 5 | IO_L68N_5 | AJ24 |
| 5 | IO_L68P_5 | AJ23 |
| 5 | IO_L67N_5 | AN24 |
| 5 | IO_L67P_5 | AN23 |
| 5 | IO_L60N_5 | AN26 |
| 5 | IO_L60P_5 | AN25 |
| 5 | IO_L54N_5 | AL25 |
| 5 | IO_L54P_5 | AL24 |
| 5 | IO_L53N_5 | AE20 |
| 5 | IO_L53P_5 | AE21 |
| 5 | IO_L52N_5 | AN27 |
| 5 | IO_L52P_5 | AP26 |
| 5 | IO_L51N_5/VREF_5 | AP29 |
| 5 | IO_L51P_5 | AP28 |
| 5 | IO_L50N_5 | AG21 |
| 5 | IO_L50P_5 | AG22 |
| 5 | IO_L49N_5 | AN29 |
| 5 | IO_L49P_5 | AN28 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------------|------------|
| 5 | IO_L30N_5 | AK24 |
| 5 | IO_L30P_5 | AK25 |
| 5 | IO_L29N_5 | AH23 |
| 5 | IO_L29P_5 | AH22 |
| 5 | IO_L28N_5 | AP31 |
| 5 | IO_L28P_5 | AP30 |
| 5 | IO_L27N_5/VREF_5 | AH24 |
| 5 | IO_L27P_5 | AH25 |
| 5 | IO_L26N_5 | AF22 |
| 5 | IO_L26P_5 | AF23 |
| 5 | IO_L25N_5 | AM27 |
| 5 | IO_L25P_5 | AM26 |
| 5 | IO_L24N_5 | AL27 |
| 5 | IO_L24P_5 | AL26 |
| 5 | IO_L23N_5 | AH26 |
| 5 | IO_L23P_5 | AJ25 |
| 5 | IO_L22N_5 | AN31 |
| 5 | IO_L22P_5 | AN30 |
| 5 | IO_L21N_5/VREF_5 | AK26 |
| 5 | IO_L21P_5 | AK27 |
| 5 | IO_L20N_5 | AG23 |
| 5 | IO_L20P_5 | AF24 |
| 5 | IO_L19N_5 | AM33 |
| 5 | IO_L19P_5 | AN32 |
| 5 | IO_L06N_5 | AJ27 |
| 5 | IO_L06P_5 | AJ26 |
| 5 | IO_L05N_5/VRP_5 | AE22 |
| 5 | IO_L05P_5/VRN_5 | AE23 |
| 5 | IO_L04N_5 | AM28 |
| 5 | IO_L04P_5/VREF_5 | AM29 |
| 5 | IO_L03N_5/D4/ALT_VRP_5 | AK28 |
| 5 | IO_L03P_5/D5/ALT_VRN_5 | AL29 |
| 5 | IO_L02N_5/D6 | AG24 |
| 5 | IO_L02P_5/D7 | AG25 |
| 5 | IO_L01N_5/RDWR_B | AL30 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 5 | IO_L01P_5/CS_B | AM31 |
| | | |
| 6 | IO_L01P_6 | AE24 |
| 6 | IO_L01N_6 | AD25 |
| 6 | IO_L02P_6/VRN_6 | AJ30 |
| 6 | IO_L02N_6/VRP_6 | AH30 |
| 6 | IO_L03P_6 | AL32 |
| 6 | IO_L03N_6/VREF_6 | AK32 |
| 6 | IO_L04P_6 | AF25 |
| 6 | IO_L04N_6 | AE25 |
| 6 | IO_L05P_6 | AJ31 |
| 6 | IO_L05N_6 | AK31 |
| 6 | IO_L06P_6 | AH29 |
| 6 | IO_L06N_6 | AG29 |
| 6 | IO_L19P_6 | AG26 |
| 6 | IO_L19N_6 | AF26 |
| 6 | IO_L20P_6 | AL33 |
| 6 | IO_L20N_6 | AK33 |
| 6 | IO_L21P_6 | AJ32 |
| 6 | IO_L21N_6/VREF_6 | AH32 |
| 6 | IO_L22P_6 | AG28 |
| 6 | IO_L22N_6 | AF28 |
| 6 | IO_L23P_6 | AG30 |
| 6 | IO_L23N_6 | AF30 |
| 6 | IO_L24P_6 | AF29 |
| 6 | IO_L24N_6 | AE29 |
| 6 | IO_L25P_6 | AF27 |
| 6 | IO_L25N_6 | AE27 |
| 6 | IO_L26P_6 | AL34 |
| 6 | IO_L26N_6 | AK34 |
| 6 | IO_L27P_6 | AE28 |
| 6 | IO_L27N_6/VREF_6 | AD28 |
| 6 | IO_L28P_6 | AE26 |
| 6 | IO_L28N_6 | AD26 |
| 6 | IO_L29P_6 | AF31 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L29N_6 | AG31 |
| 6 | IO_L30P_6 | AF32 |
| 6 | IO_L30N_6 | AG32 |
| 6 | IO_L43P_6 | AC25 |
| 6 | IO_L43N_6 | AB25 |
| 6 | IO_L44P_6 | AJ33 |
| 6 | IO_L44N_6 | AH33 |
| 6 | IO_L45P_6 | AE31 |
| 6 | IO_L45N_6/VREF_6 | AD32 |
| 6 | IO_L46P_6 | AD27 |
| 6 | IO_L46N_6 | AC27 |
| 6 | IO_L47P_6 | AJ34 |
| 6 | IO_L47N_6 | AH34 |
| 6 | IO_L48P_6 | AE30 |
| 6 | IO_L48N_6 | AD30 |
| 6 | IO_L49P_6 | AC26 |
| 6 | IO_L49N_6 | AB26 |
| 6 | IO_L50P_6 | AD29 |
| 6 | IO_L50N_6 | AC29 |
| 6 | IO_L51P_6 | AF33 |
| 6 | IO_L51N_6/VREF_6 | AG33 |
| 6 | IO_L52P_6 | AC28 |
| 6 | IO_L52N_6 | AB28 |
| 6 | IO_L53P_6 | AF34 |
| 6 | IO_L53N_6 | AE33 |
| 6 | IO_L54P_6 | AB27 |
| 6 | IO_L54N_6 | AA27 |
| 6 | IO_L67P_6 | AA25 |
| 6 | IO_L67N_6 | Y25 |
| 6 | IO_L68P_6 | AD33 |
| 6 | IO_L68N_6 | AC33 |
| 6 | IO_L69P_6 | AC32 |
| 6 | IO_L69N_6/VREF_6 | AB32 |
| 6 | IO_L70P_6 | AA26 |
| 6 | IO_L70N_6 | Y26 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L71P_6 | AD34 |
| 6 | IO_L71N_6 | AC34 |
| 6 | IO_L72P_6 | AC31 |
| 6 | IO_L72N_6 | AD31 |
| 6 | IO_L73P_6 | Y27 |
| 6 | IO_L73N_6 | W27 |
| 6 | IO_L74P_6 | AB29 |
| 6 | IO_L74N_6 | AA29 |
| 6 | IO_L75P_6 | AB31 |
| 6 | IO_L75N_6/VREF_6 | AA31 |
| 6 | IO_L76P_6 | Y28 |
| 6 | IO_L76N_6 | Y29 |
| 6 | IO_L77P_6 | AB33 |
| 6 | IO_L77N_6 | AA33 |
| 6 | IO_L78P_6 | AA30 |
| 6 | IO_L78N_6 | AB30 |
| 6 | IO_L79P_6 | W24 |
| 6 | IO_L79N_6 | V24 |
| 6 | IO_L80P_6 | AB34 |
| 6 | IO_L80N_6 | AA34 |
| 6 | IO_L81P_6 | W33 |
| 6 | IO_L81N_6/VREF_6 | Y34 |
| 6 | IO_L82P_6 | W25 |
| 6 | IO_L82N_6 | V25 |
| 6 | IO_L83P_6 | Y32 |
| 6 | IO_L83N_6 | AA32 |
| 6 | IO_L84P_6 | W29 |
| 6 | IO_L84N_6 | V29 |
| 6 | IO_L91P_6 | W28 |
| 6 | IO_L91N_6 | V28 |
| 6 | IO_L92P_6 | V33 |
| 6 | IO_L92N_6 | V34 |
| 6 | IO_L93P_6 | Y31 |
| 6 | IO_L93N_6/VREF_6 | W31 |
| 6 | IO_L94P_6 | V26 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 6 | IO_L94N_6 | V27 |
| 6 | IO_L95P_6 | W30 |
| 6 | IO_L95N_6 | V30 |
| 6 | IO_L96P_6 | V32 |
| 6 | IO_L96N_6 | W32 |
| | | |
| 7 | IO_L96P_7 | U31 |
| 7 | IO_L96N_7 | V31 |
| 7 | IO_L95P_7 | T28 |
| 7 | IO_L95N_7 | U28 |
| 7 | IO_L94P_7 | U33 |
| 7 | IO_L94N_7 | U34 |
| 7 | IO_L93P_7/VREF_7 | U29 |
| 7 | IO_L93N_7 | T29 |
| 7 | IO_L92P_7 | U27 |
| 7 | IO_L92N_7 | U26 |
| 7 | IO_L91P_7 | T30 |
| 7 | IO_L91N_7 | U30 |
| 7 | IO_L84P_7 | R32 |
| 7 | IO_L84N_7 | T32 |
| 7 | IO_L83P_7 | U25 |
| 7 | IO_L83N_7 | T25 |
| 7 | IO_L82P_7 | R34 |
| 7 | IO_L82N_7 | T33 |
| 7 | IO_L81P_7/VREF_7 | N34 |
| 7 | IO_L81N_7 | P34 |
| 7 | IO_L80P_7 | U24 |
| 7 | IO_L80N_7 | T24 |
| 7 | IO_L79P_7 | R31 |
| 7 | IO_L79N_7 | T31 |
| 7 | IO_L78P_7 | N32 |
| 7 | IO_L78N_7 | P32 |
| 7 | IO_L77P_7 | T27 |
| 7 | IO_L77N_7 | R27 |
| 7 | IO_L76P_7 | N33 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L76N_7 | P33 |
| 7 | IO_L75P_7/VREF_7 | R29 |
| 7 | IO_L75N_7 | R28 |
| 7 | IO_L74P_7 | R26 |
| 7 | IO_L74N_7 | P26 |
| 7 | IO_L73P_7 | N31 |
| 7 | IO_L73N_7 | P31 |
| 7 | IO_L72P_7 | N30 |
| 7 | IO_L72N_7 | P30 |
| 7 | IO_L71P_7 | R25 |
| 7 | IO_L71N_7 | P25 |
| 7 | IO_L70P_7 | L34 |
| 7 | IO_L70N_7 | M34 |
| 7 | IO_L69P_7/VREF_7 | P29 |
| 7 | IO_L69N_7 | N29 |
| 7 | IO_L68P_7 | P27 |
| 7 | IO_L68N_7 | N27 |
| 7 | IO_L67P_7 | L32 |
| 7 | IO_L67N_7 | M32 |
| 7 | IO_L54P_7 | L31 |
| 7 | IO_L54N_7 | M31 |
| 7 | IO_L53P_7 | K29 |
| 7 | IO_L53N_7 | L30 |
| 7 | IO_L52P_7 | L33 |
| 7 | IO_L52N_7 | M33 |
| 7 | IO_L51P_7/VREF_7 | M29 |
| 7 | IO_L51N_7 | L29 |
| 7 | IO_L50P_7 | M28 |
| 7 | IO_L50N_7 | N28 |
| 7 | IO_L49P_7 | K30 |
| 7 | IO_L49N_7 | K31 |
| 7 | IO_L48P_7 | H32 |
| 7 | IO_L48N_7 | J32 |
| 7 | IO_L47P_7 | N26 |
| 7 | IO_L47N_7 | M26 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L46P_7 | J33 |
| 7 | IO_L46N_7 | K33 |
| 7 | IO_L45P_7/VREF_7 | H33 |
| 7 | IO_L45N_7 | J34 |
| 7 | IO_L44P_7 | M27 |
| 7 | IO_L44N_7 | L27 |
| 7 | IO_L43P_7 | H31 |
| 7 | IO_L43N_7 | J31 |
| 7 | IO_L30P_7 | F32 |
| 7 | IO_L30N_7 | G32 |
| 7 | IO_L29P_7 | N25 |
| 7 | IO_L29N_7 | M25 |
| 7 | IO_L28P_7 | F34 |
| 7 | IO_L28N_7 | G34 |
| 7 | IO_L27P_7/VREF_7 | J30 |
| 7 | IO_L27N_7 | H30 |
| 7 | IO_L26P_7 | K28 |
| 7 | IO_L26N_7 | L28 |
| 7 | IO_L25P_7 | H28 |
| 7 | IO_L25N_7 | J29 |
| 7 | IO_L24P_7 | G29 |
| 7 | IO_L24N_7 | H29 |
| 7 | IO_L23P_7 | L26 |
| 7 | IO_L23N_7 | K26 |
| 7 | IO_L22P_7 | F33 |
| 7 | IO_L22N_7 | G33 |
| 7 | IO_L21P_7/VREF_7 | J28 |
| 7 | IO_L21N_7 | J27 |
| 7 | IO_L20P_7 | K27 |
| 7 | IO_L20N_7 | J26 |
| 7 | IO_L19P_7 | E31 |
| 7 | IO_L19N_7 | F31 |
| 7 | IO_L06P_7 | D32 |
| 7 | IO_L06N_7 | E32 |
| 7 | IO_L05P_7 | L25 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|------------------|------------|
| 7 | IO_L05N_7 | K24 |
| 7 | IO_L04P_7 | D34 |
| 7 | IO_L04N_7 | E34 |
| 7 | IO_L03P_7/VREF_7 | G30 |
| 7 | IO_L03N_7 | F30 |
| 7 | IO_L02P_7/VRN_7 | K25 |
| 7 | IO_L02N_7/VRP_7 | J25 |
| 7 | IO_L01P_7 | D33 |
| 7 | IO_L01N_7 | E33 |
| | | |
| 0 | VCCO_0 | M22 |
| 0 | VCCO_0 | M21 |
| 0 | VCCO_0 | M20 |
| 0 | VCCO_0 | M19 |
| 0 | VCCO_0 | M18 |
| 0 | VCCO_0 | L23 |
| 0 | VCCO_0 | L22 |
| 0 | VCCO_0 | L21 |
| 0 | VCCO_0 | L20 |
| 0 | VCCO_0 | E20 |
| 0 | VCCO_0 | D28 |
| 0 | VCCO_0 | A25 |
| 0 | VCCO_0 | A19 |
| 1 | VCCO_1 | M17 |
| 1 | VCCO_1 | M16 |
| 1 | VCCO_1 | M15 |
| 1 | VCCO_1 | M14 |
| 1 | VCCO_1 | M13 |
| 1 | VCCO_1 | L15 |
| 1 | VCCO_1 | L14 |
| 1 | VCCO_1 | L13 |
| 1 | VCCO_1 | L12 |
| 1 | VCCO_1 | E15 |
| 1 | VCCO_1 | D7 |
| 1 | VCCO_1 | A16 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 1 | VCCO_1 | A10 |
| 2 | VCCO_2 | U12 |
| 2 | VCCO_2 | T12 |
| 2 | VCCO_2 | T1 |
| 2 | VCCO_2 | R12 |
| 2 | VCCO_2 | R11 |
| 2 | VCCO_2 | R5 |
| 2 | VCCO_2 | P12 |
| 2 | VCCO_2 | P11 |
| 2 | VCCO_2 | N12 |
| 2 | VCCO_2 | N11 |
| 2 | VCCO_2 | M11 |
| 2 | VCCO_2 | K1 |
| 2 | VCCO_2 | G4 |
| 3 | VCCO_3 | AH4 |
| 3 | VCCO_3 | AE1 |
| 3 | VCCO_3 | AC11 |
| 3 | VCCO_3 | AB12 |
| 3 | VCCO_3 | AB11 |
| 3 | VCCO_3 | AA12 |
| 3 | VCCO_3 | AA11 |
| 3 | VCCO_3 | Y12 |
| 3 | VCCO_3 | Y11 |
| 3 | VCCO_3 | Y5 |
| 3 | VCCO_3 | W12 |
| 3 | VCCO_3 | W1 |
| 3 | VCCO_3 | V12 |
| 4 | VCCO_4 | AP16 |
| 4 | VCCO_4 | AP10 |
| 4 | VCCO_4 | AL7 |
| 4 | VCCO_4 | AK15 |
| 4 | VCCO_4 | AD15 |
| 4 | VCCO_4 | AD14 |
| 4 | VCCO_4 | AD13 |
| 4 | VCCO_4 | AD12 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 4 | VCCO_4 | AC17 |
| 4 | VCCO_4 | AC16 |
| 4 | VCCO_4 | AC15 |
| 4 | VCCO_4 | AC14 |
| 4 | VCCO_4 | AC13 |
| 5 | VCCO_5 | AP25 |
| 5 | VCCO_5 | AP19 |
| 5 | VCCO_5 | AL28 |
| 5 | VCCO_5 | AK20 |
| 5 | VCCO_5 | AD23 |
| 5 | VCCO_5 | AD22 |
| 5 | VCCO_5 | AD21 |
| 5 | VCCO_5 | AD20 |
| 5 | VCCO_5 | AC22 |
| 5 | VCCO_5 | AC21 |
| 5 | VCCO_5 | AC20 |
| 5 | VCCO_5 | AC19 |
| 5 | VCCO_5 | AC18 |
| 6 | VCCO_6 | AH31 |
| 6 | VCCO_6 | AE34 |
| 6 | VCCO_6 | AC24 |
| 6 | VCCO_6 | AB24 |
| 6 | VCCO_6 | AB23 |
| 6 | VCCO_6 | AA24 |
| 6 | VCCO_6 | AA23 |
| 6 | VCCO_6 | Y30 |
| 6 | VCCO_6 | Y24 |
| 6 | VCCO_6 | Y23 |
| 6 | VCCO_6 | W34 |
| 6 | VCCO_6 | W23 |
| 6 | VCCO_6 | V23 |
| 7 | VCCO_7 | U23 |
| 7 | VCCO_7 | T34 |
| 7 | VCCO_7 | T23 |
| 7 | VCCO_7 | R30 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| 7 | VCCO_7 | R24 |
| 7 | VCCO_7 | R23 |
| 7 | VCCO_7 | P24 |
| 7 | VCCO_7 | P23 |
| 7 | VCCO_7 | N24 |
| 7 | VCCO_7 | N23 |
| 7 | VCCO_7 | M24 |
| 7 | VCCO_7 | K34 |
| 7 | VCCO_7 | G31 |
| | | |
| NA | CCLK | AH8 |
| NA | PROG_B | D30 |
| NA | DONE | AJ7 |
| NA | M0 | AH27 |
| NA | M1 | AJ28 |
| NA | M2 | AK29 |
| NA | HSWAP_EN | E29 |
| NA | TCK | F7 |
| NA | TDI | C31 |
| NA | TDO | D5 |
| NA | TMS | E6 |
| NA | PWRDWN_B | AK6 |
| NA | DXN | F28 |
| NA | DXP | G27 |
| NA | VBATT | C4 |
| NA | RSVD | G8 |
| NA | VCCAUX | AM30 |
| NA | VCCAUX | AM18 |
| NA | VCCAUX | AM5 |
| NA | VCCAUX | V3 |
| NA | VCCAUX | U32 |
| NA | VCCAUX | C30 |
| NA | VCCAUX | C17 |
| NA | VCCAUX | C5 |
| NA | VCCINT | AD24 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCINT | AD11 |
| NA | VCCINT | AC23 |
| NA | VCCINT | AC12 |
| NA | VCCINT | AB22 |
| NA | VCCINT | AB21 |
| NA | VCCINT | AB20 |
| NA | VCCINT | AB19 |
| NA | VCCINT | AB18 |
| NA | VCCINT | AB17 |
| NA | VCCINT | AB16 |
| NA | VCCINT | AB15 |
| NA | VCCINT | AB14 |
| NA | VCCINT | AB13 |
| NA | VCCINT | AA22 |
| NA | VCCINT | AA13 |
| NA | VCCINT | Y22 |
| NA | VCCINT | Y13 |
| NA | VCCINT | W22 |
| NA | VCCINT | W13 |
| NA | VCCINT | V22 |
| NA | VCCINT | V13 |
| NA | VCCINT | U22 |
| NA | VCCINT | U13 |
| NA | VCCINT | T22 |
| NA | VCCINT | T13 |
| NA | VCCINT | R22 |
| NA | VCCINT | R13 |
| NA | VCCINT | P22 |
| NA | VCCINT | P13 |
| NA | VCCINT | N22 |
| NA | VCCINT | N21 |
| NA | VCCINT | N20 |
| NA | VCCINT | N19 |
| NA | VCCINT | N18 |
| NA | VCCINT | N17 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | VCCINT | N16 |
| NA | VCCINT | N15 |
| NA | VCCINT | N14 |
| NA | VCCINT | N13 |
| NA | VCCINT | M23 |
| NA | VCCINT | M12 |
| NA | VCCINT | L24 |
| NA | VCCINT | L11 |
| | | |
| NA | GND | AP32 |
| NA | GND | AP27 |
| NA | GND | AP8 |
| NA | GND | AP3 |
| NA | GND | AN33 |
| NA | GND | AN20 |
| NA | GND | AN15 |
| NA | GND | AN2 |
| NA | GND | AM34 |
| NA | GND | AM32 |
| NA | GND | AM25 |
| NA | GND | AM10 |
| NA | GND | AM3 |
| NA | GND | AM1 |
| NA | GND | AL31 |
| NA | GND | AL4 |
| NA | GND | AK30 |
| NA | GND | AK23 |
| NA | GND | AK12 |
| NA | GND | AK5 |
| NA | GND | AJ29 |
| NA | GND | AJ6 |
| NA | GND | AH28 |
| NA | GND | AH21 |
| NA | GND | AH14 |
| NA | GND | AH7 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | AG34 |
| NA | GND | AG27 |
| NA | GND | AG8 |
| NA | GND | AG1 |
| NA | GND | AF19 |
| NA | GND | AF16 |
| NA | GND | AE32 |
| NA | GND | AE3 |
| NA | GND | AC30 |
| NA | GND | AC5 |
| NA | GND | AA28 |
| NA | GND | AA21 |
| NA | GND | AA20 |
| NA | GND | AA19 |
| NA | GND | AA18 |
| NA | GND | AA17 |
| NA | GND | AA16 |
| NA | GND | AA15 |
| NA | GND | AA14 |
| NA | GND | AA7 |
| NA | GND | Y33 |
| NA | GND | Y21 |
| NA | GND | Y20 |
| NA | GND | Y19 |
| NA | GND | Y18 |
| NA | GND | Y17 |
| NA | GND | Y16 |
| NA | GND | Y15 |
| NA | GND | Y14 |
| NA | GND | Y2 |
| NA | GND | W26 |
| NA | GND | W21 |
| NA | GND | W20 |
| NA | GND | W19 |
| NA | GND | W18 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | W17 |
| NA | GND | W16 |
| NA | GND | W15 |
| NA | GND | W14 |
| NA | GND | W9 |
| NA | GND | V21 |
| NA | GND | V20 |
| NA | GND | V19 |
| NA | GND | V18 |
| NA | GND | V17 |
| NA | GND | V16 |
| NA | GND | V15 |
| NA | GND | V14 |
| NA | GND | U21 |
| NA | GND | U20 |
| NA | GND | U19 |
| NA | GND | U18 |
| NA | GND | U17 |
| NA | GND | U16 |
| NA | GND | U15 |
| NA | GND | U14 |
| NA | GND | T26 |
| NA | GND | T21 |
| NA | GND | T20 |
| NA | GND | T19 |
| NA | GND | T18 |
| NA | GND | T17 |
| NA | GND | T16 |
| NA | GND | T15 |
| NA | GND | T14 |
| NA | GND | T9 |
| NA | GND | R33 |
| NA | GND | R21 |
| NA | GND | R20 |
| NA | GND | R19 |

Table 81: CF1144 CGA — XQR2V6000

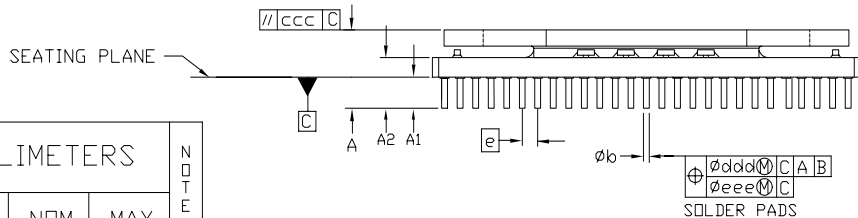
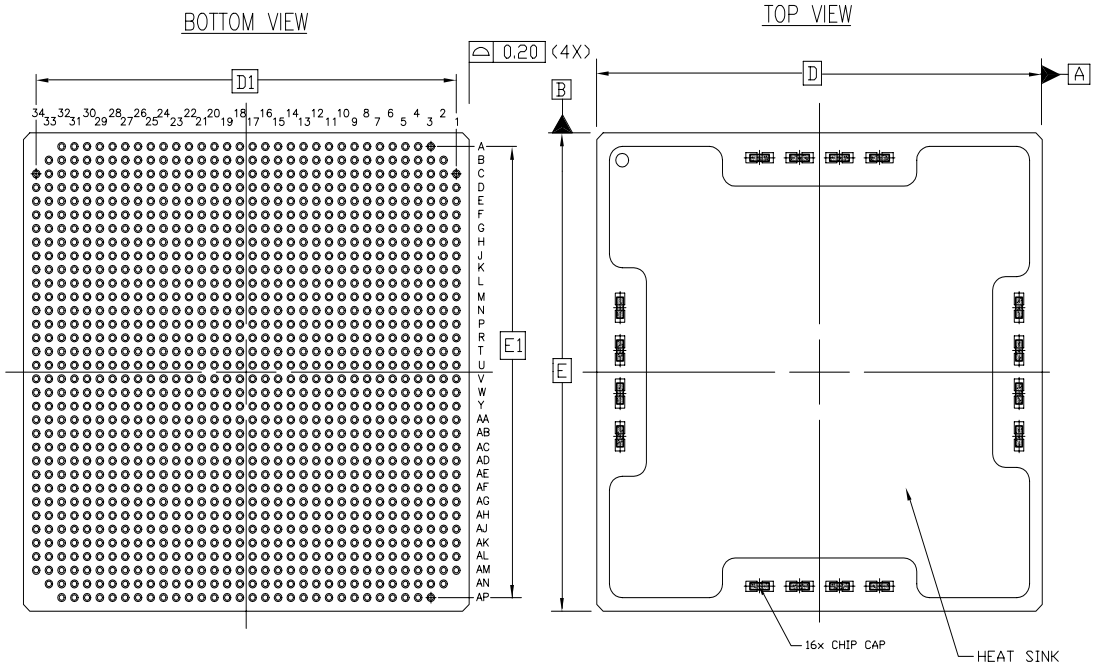
| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | R18 |
| NA | GND | R17 |
| NA | GND | R16 |
| NA | GND | R15 |
| NA | GND | R14 |
| NA | GND | R2 |
| NA | GND | P28 |
| NA | GND | P21 |
| NA | GND | P20 |
| NA | GND | P19 |
| NA | GND | P18 |
| NA | GND | P17 |
| NA | GND | P16 |
| NA | GND | P15 |
| NA | GND | P14 |
| NA | GND | P7 |
| NA | GND | M30 |
| NA | GND | M5 |
| NA | GND | K32 |
| NA | GND | K3 |
| NA | GND | J19 |
| NA | GND | J16 |
| NA | GND | H34 |
| NA | GND | H27 |
| NA | GND | H8 |
| NA | GND | H1 |
| NA | GND | G28 |
| NA | GND | G21 |
| NA | GND | G14 |
| NA | GND | G7 |
| NA | GND | F29 |
| NA | GND | F6 |
| NA | GND | E30 |
| NA | GND | E23 |
| NA | GND | E12 |

Table 81: CF1144 CGA — XQR2V6000

| Bank | Pin Description | Pin Number |
|------|-----------------|------------|
| NA | GND | E5 |
| NA | GND | D31 |
| NA | GND | D4 |
| NA | GND | C34 |
| NA | GND | C32 |
| NA | GND | C25 |
| NA | GND | C10 |
| NA | GND | C3 |
| NA | GND | C1 |
| NA | GND | B33 |
| NA | GND | B20 |
| NA | GND | B15 |
| NA | GND | B2 |
| NA | GND | A32 |
| NA | GND | A27 |
| NA | GND | A8 |
| NA | GND | A3 |

CF1144 Ceramic Flip-Chip Fine-Pitch CGA Package Specifications (1.00mm pitch)

CF1144 WITH CAST COLUMNS



| SYMBOL | MILLIMETERS | | | NOTE |
|--------------------------------|-------------------|-------------------|------|------|
| | MIN. | NOM. | MAX. | |
| A | 6.30 | 6.65 | 7.00 | |
| A ₁ | 2.05 | 2.20 | 2.35 | |
| A ₂ | 3.40 | 3.70 | 4.00 | |
| D/E | 35.00 BASIC | | | |
| D ₁ /E ₁ | 33.00 REF | | | |
| e | 1.00 BASIC | | | |
| φ _b | 0.51 | 0.54 | 0.57 | |
| ccc | \sphericalangle | \sphericalangle | 0.35 | |
| ddd | \sphericalangle | \sphericalangle | 0.30 | |
| eee | \sphericalangle | \sphericalangle | 0.10 | |
| M | 34 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAR-1 (DEPOPULATED)

Figure 56: CF1144 Ceramic Flip-Chip Fine-Pitch CGA Package Specifications

Revision History

This section records the change history for this module of the data sheet.

| Date | Version | Revision |
|----------|---------|-------------------------|
| 9/24/03 | 1.0 | Advance release. |
| 01/08/04 | 1.1 | Initial Xilinx release. |