Dual Bipolar JFET Operational Amplifier

GENERAL DESCRIPTION

The XR-082/XR-083 family of dual bipolar JFET operational amplifiers are designed to offer higher performance than conventional bipolar op amps. Each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. These operational amplifier circuits are fabricated using ion-implantation technology which combines well-matched junction JFETs and high-performance bipolar transistors on the same monolithic chip.

The XR-082 of family of dual bipolar JFET op amps are packaged in 8-pin dual-in-line packages. The XR-083 family of op amps offer independent offset adjustment for each of the individual op amps on the same chip, and are available in 14-pin dual-in-line packages.

FEATURES

Direct Replacement for TL082/TL083
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
High Input Impedance . . JFET Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew Rate . . 13 V/μs, Typical

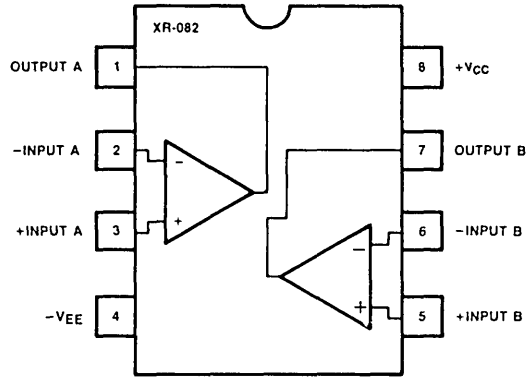
APPLICATIONS

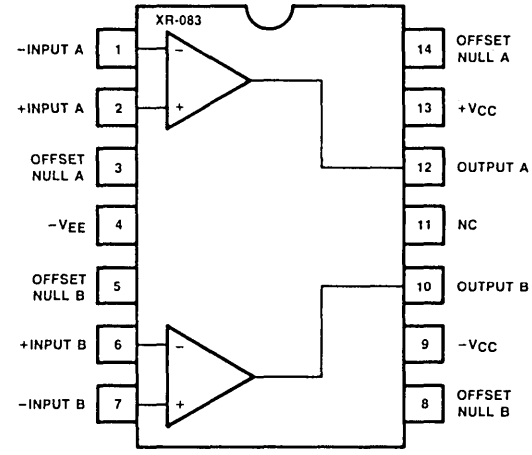
Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW°C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to + 150°C

FUNCTIONAL BLOCK DIAGRAMS





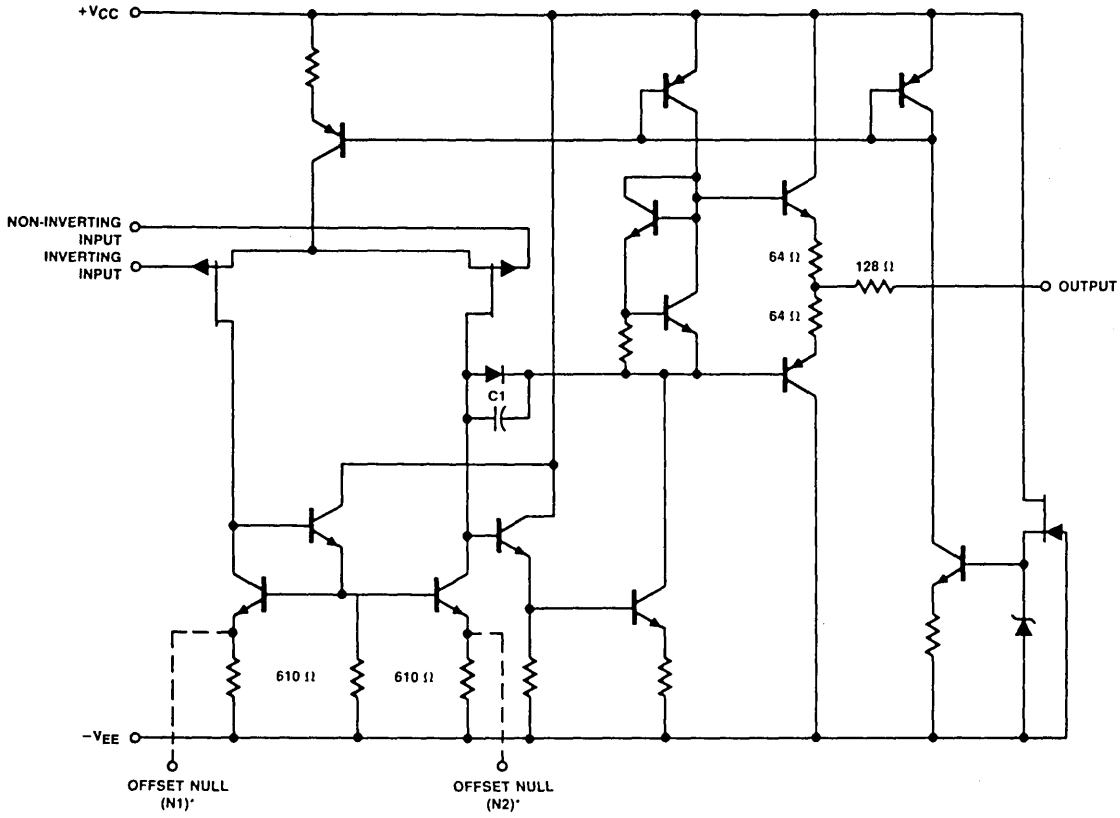
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-082M/XR-083M	Ceramic	−55°C to +125°C
XR-082N/XR-083N	Ceramic	−25°C to + 85°C
XR-082P/XR-083P	Plastic	−25°C to + 85°C
XR-082CN/XR-083CN	Ceramic	0°C to + 70°C
XR-082CP/XR-083CP	Plastic	0°C to + 70°C

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.

		XR-082M/ XR-083M			XR-082/ XR-083			XR-082C/ XR-083C				
SYMBOL	PARAMETERS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OS} V_{OS}	Input Offset Voltage		3	6 9		3	6 9		5	15 20	mV mV	R_S = 50Ω R_S = 50Ω, T_A = Full Range
$\Delta V_{OS}/\Delta T$	Offset Voltage Temp. Coef.		10			10			10		µV/°C	R_S = 50Ω, T_A = Full Range
I_B	Input Bias Current		30	200		30	200		30	400	pA	
I_B	Input Bias Current Over Temp.			50			20			20	nA	T_A = Full Range
I_{OS}	Input Offset Current		5	100		5	100		5	200	pA	
	Input Offset Current Over Temp.			20			10			5	nA	T_A = Full Range
I_{CC}	Supply Current (per amplifier)		1.4	2.8		1.4	2.8		1.4	2.8	mA	No Load, No Input Signal
V_{ICM}	Input Common Mode Range	±12			±12			±10			V	
A_{VOL}	Voltage Gain	50 25	200		50 25	200		25 15	200		V/mV	R_L ≥ 2 kΩ, V_O = ±10V T_A = Full Range
V_{OPP}	Max. Output Swing (peak-to-peak)	24 24	27		24 24	27		24 24	27		V	R_L ≥ 10 kΩ T_A = Full Range
R_{IN}	Input Resistance		10^{12}			10^{12}			10^{12}		Ω	
BW	Unity-Gain Bandwidth		3			3			3		MHz	
CMRR	Common-Mode Rejection	80	86		80	86		70	76		dB	R_S ≤ 10 kΩ
PSRR	Supply-Voltage Rejection	80	86		80	86		70	76		dB	
	Channel Separation		120			120			120		dB	A_V = 100, Freq. = 1 kHz
dV_{OUT}/DT	Slew Rate		13			13			13		V/µS	A_V = 1, R_L = 2 kΩ, C_L = 100 pF, V_1 = 10V
T_R T_O	Rise Time Overshoot		0.1 10			0.1 10			0.1 10		µsec %	A_V = 1, R_L = 2 kΩ C_L = 100 pF, V_1 = 20 mV
E_N	Equivalent Input Noise Voltage		20			20			20		nV/√Hz	R_S = 100Ω f = 1 kHz

Note 1: For Supply Voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.



EQUIVALENT SCHEMATIC DIAGRAM