

FEATURES

- Internal R/C Oscillator
- Provides seven filters in one 16 pin package
- Dual Inputs for summing Left and Right Channels
- Provides 30 dB of Gain
- Low Noise CMOS
- Electro-Static Discharge (ESD) Protection

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems

GENERAL DESCRIPTION

The XR-1091 is an eight output switched-capacitor band pass filter dedicated for use in audio applications. Seven of the outputs are from bandpass filters spaced 1 1/2 octaves apart starting at 63 Hz. The eighth output is the peak of the seven outputs. All of the outputs provide a peak hold for use with most display circuits. The two inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed.

The XR-1091 is available in a 16 pin plastic DIP. The XR-1091 is fabricated in 2 μm double polysilicon CMOS for low noise and low clock feedthrough. The nominal operating voltages are ±5 VDC to ±6 VDC. The self contained oscillator is designed to operate at 400 kHz with an external resistor and capacitor.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1091ECP	16 Lead 300 Mil PDIP	-30°C to +75°C

BLOCK DIAGRAM

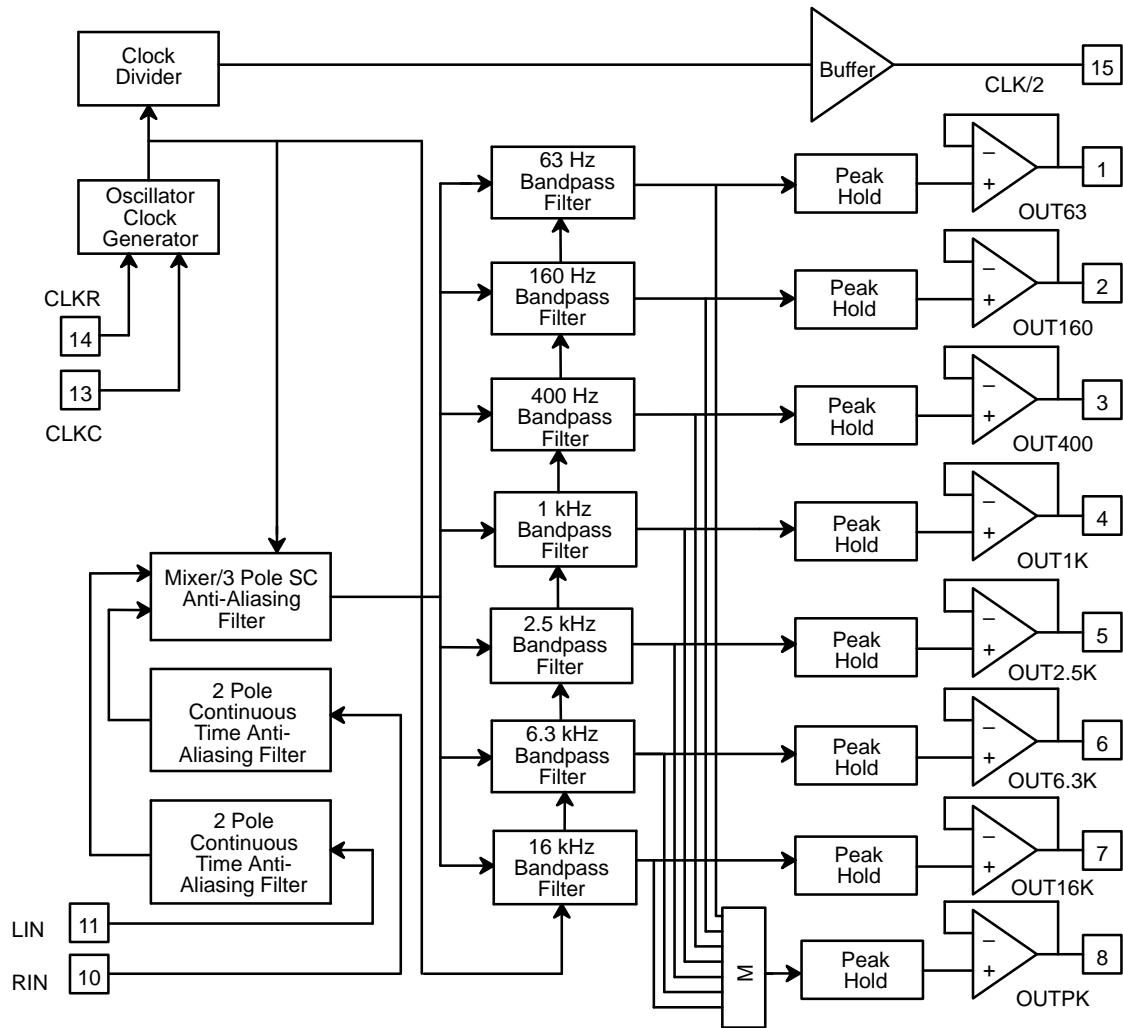
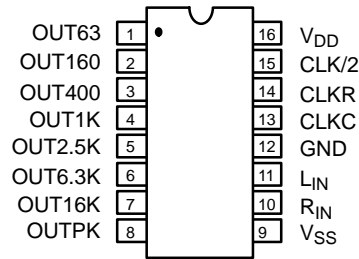


Figure 1. 7-Band Graphic Equalizer Display Filter

PIN CONFIGURATION



16 Pin PDIP (0.300")

PIN DESCRIPTION

Pin #	Symbol	Description
1	OUT63	Peak held output of the 63 Hz filter. This output can drive a 10 K Ω load.
2	OUT160	Peak held output of the 160 Hz bandpass filter.
3	OUT400	Peak held output of the 400 Hz bandpass filter.
4	OUT1 K	Peak held output of the 1 kHz bandpass filter.
5	OUT2.5 K	Peak held output of the 2.5 kHz bandpass filter.
6	OUT6.3 K	Peak held output of the 6.3 kHz bandpass filter.
7	OUT16 K	Peak held output of the 16 kHz bandpass filter.
8	OUT	Peak output of the above also peak held.
9	V _{SS}	Nominally -6 VDC. This should be decoupled with at least a 0.47 μ F capacitor to ground located as close as possible to this pin.
10	R _{IN}	Right Channel Input. The input impedance of this pin is greater than 1 x 10 ¹² Ω .
11	L _{IN}	Left Channel Input. The input impedance of this pin is greater than 1 x10 ¹² Ω .
12	GND	Ground for both digital and analog.
13	CLKC	Clock Capacitor. The timing capacitor should be tied from this pin to ground.
14	CLKR	Clock Resistor. The timing resistor would be tied from this pin to pin 13 CLKC.
15	CLK/2	This output is at 200 kHz in normal operation. The clock swings from V _{SS} to V _{DD} .
16	V _{DD}	Nominally tied to +6 VDC. This pin should be decoupled with a 0.47 μ F capacitor to ground located as close as possible to this pin.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{DD} = +6$ VDC, $V_{SS} = -6$ VDC, $T_A = 25^\circ\text{C}$, S1 open, S2, S3 to ground, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{DD5}	Supply Current		10.0		mA	$V_{DD} = 5$ VDC, $V_{SS} = -5$ VDC
I_{DD6}	Supply Current		10.7	18.0	mA	$V_{DD} = +6$ VDC, $V_{SS} = -6$ VDC
I_{IL}	Input Leakage	-10		+10	μA	
TCLKRP (R-C)	Clock Freq	385	400	415	kHz	$R = 1.46$ K Ω , $C = 1$ nF
TCLK2P (R-C)	Clock/2 Freq	185	200	215	kHz	$R_L = 100$ K Ω , $C_L = 100$ pF
ECLKR	External Clock Voltage	5			V _{pp}	$V_{CLK\ IN} = \pm 2.5$ Vpk
ECLK2	Clock/2 External Source	190	200	210	kHz	$R_L = 100$ K Ω , $C_L = 100$ pF
V_{OS}	Output Offset	0	125	200	mV	S1 to Pins 1 thru 8 sequentially
$V_{OUT\ 6.3KR}$	6.3 kHz Output, R_{IN}	3.33	3.95	4.7	V	S3 to signal source = 125 mVpk $f_{IN} = 6.3$ kHz, S1 to Pin 6
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 6.3 kHz
$V_{OUT\ 63}$	63 Hz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 63$ Hz, S1 to Pin 1
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 63 Hz
$V_{OUT\ 160}$	160 Hz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 160$ Hz, S1 to Pin 2
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 160 Hz
$V_{OUT\ 400}$	400 Hz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 400$ Hz, S1 to Pin 3
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 400 Hz
$V_{OUT\ 1K}$	1 kHz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 1$ kHz, S1 to Pin 4
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 1 kHz
$V_{OUT\ 2.5K}$	2.5 kHz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 2.5$ kHz, S1 to Pin 5
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 2.5 kHz
$V_{OUT\ 6.3K}$	6.3 kHz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 6.3$ kHz, S1 to Pin 6
		28.5	30.0	31.5	dB	
		4.65	5.2	6.0	V	200 mVpk, 6.3 kHz

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OUT16K}	16 kHz Output, L_{IN}	3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 16$ kHz, S1 to Pin 7
$V_{OUT PEAK}$	PEAK OUT, L_{IN}	28.5	30.0	31.5	dB	200 mVpk, 16 kHz
		4.65	5.2	6.0	V	
		3.33	3.95	4.7	V	S2 to signal source = 125 mVpk $f_{IN} = 1$ kHz, S1 to Pin 8
		28.5	30.0	31.5	dB	
4.65	5.2	6.0	V	200 mVpk, 1 kHz		

Notes:

Recommended power on sequence: V_{SS} first, followed by V_{DD} . When only 1 channel input is used, then the other input has to be grounded.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} +7 VDC
 V_{SS} -7 VDC

Power Dissipation
 16 Pin Plastic Dip 650 mW
 Derate above 25°C 5 mW/°C
 Storage Temperature -60°C to +150°C

SYSTEM DESCRIPTION

The XR-1091 unlike most switched-capacitor filters does not require an external clock source in order to provide the sampling clocks. This allows the designer to place the XR-1091 in any application where an active filter design is in place. The XR-1091 provides bandpass filters with center frequencies at 63 Hz, 160 Hz, 400 Hz, 1 kHz, 2.5 kHz, 6.3 kHz, and 16 kHz. These frequencies are standards in the consumer audio market. The peak

detector outputs referenced to 0V can be used to drive a variety of display decoders.

The XR-1091 contains a continuous time anti-aliasing filter with a corner frequency of 80 kHz. This prevents most signals from affecting the performance of the filters. If two separate displays are desired, then two XR-1091's could be used with the unused inputs grounded.

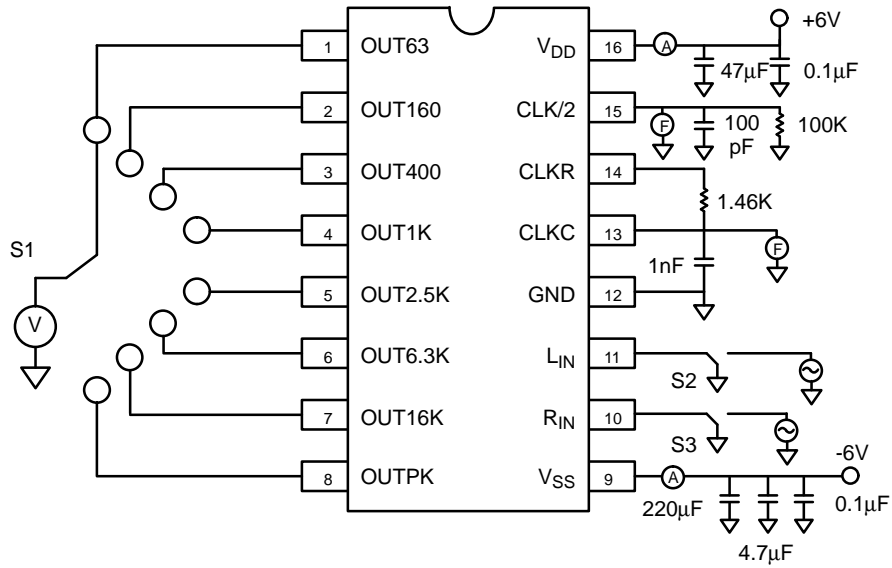


Figure 2. Test Circuit

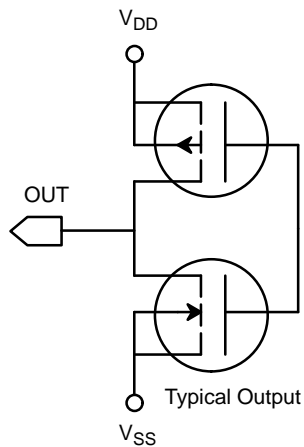


Figure 3. Typical Output

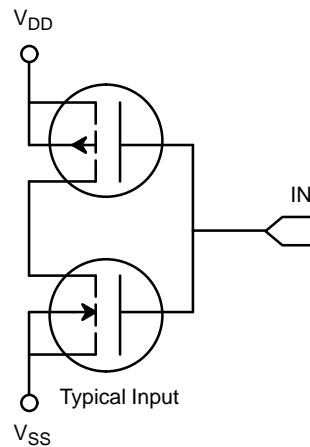


Figure 4. Typical Input

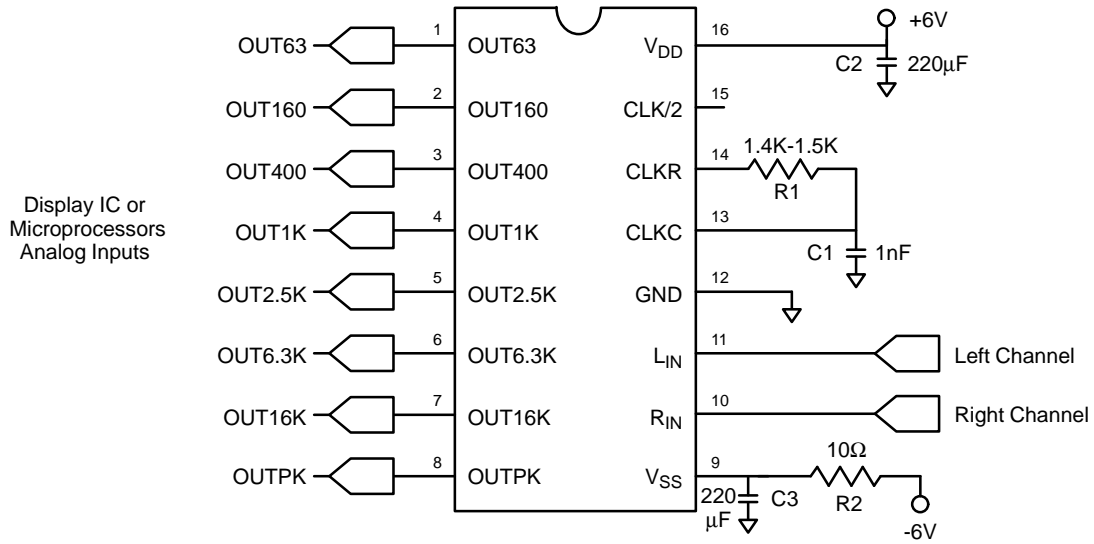
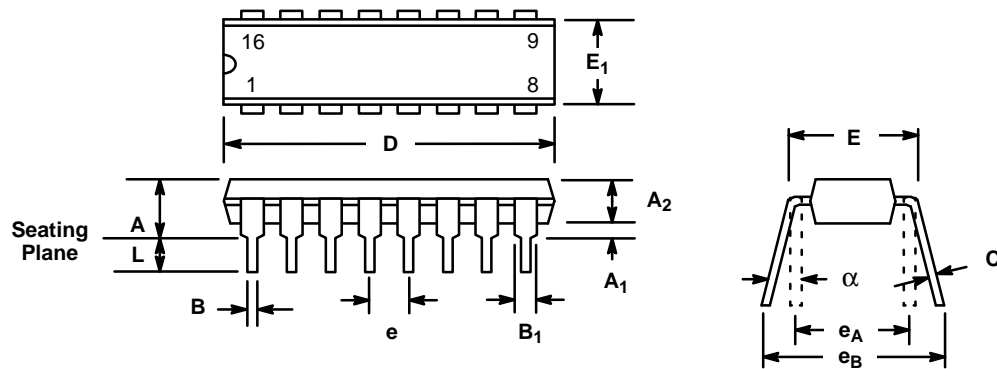


Figure 5. Typical Applications Circuit

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

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Datasheet September 1996

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