XR-1095

Seven Band Graphic Equalizer
Filter and Display Driver with
µController Interface

...the analog plus company™

September 1996-4

FEATURES

- Single Chip Equalizer and Display Driver
- Accurate Switched-Capacitor Filters
- 30dB of Gain
- Peak Hold Display Driver
- Accessory Display Driver
- µController Interface
- Simple Resistor and Capacitor Oscillator
- DIM Control for Display Brightness
- Inputs to Sum Left and Right Channels
- Low Noise, Low Power CMOS
- Set Data Mode with Flash Option

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems
- Spectrum Analyzers

GENERAL DESCRIPTION

The XR-1095 is a single chip graphic equalizer and display driver containing switched-capacitor band–pass filters, filter multiplexer, µcontroller interface, data latches and high voltage vacuum fluorescent display driver. The seven band-pass filters have 1.32 octave spacing from 63Hz up to 16kHz. They are followed by seven peak detectors, a filter multiplexer, and high voltage driver. A digital peak detector is provided for the maximum signal level (total output) in the band-pass filter frequency range. The chip also contains an accessory display driver. An internal µcontroller serial interface port facilitates the loading of control data for the display, accessory display data, and filter display data when the device is in set data mode.

Two separate inputs are included for summing the left and right channel inputs. If a separate display is desired for each channel, the unused input should be grounded and a separate device used for each input. The output multiplexer is designed to interface with most vacuum florescent display drivers. The display can have up to 13 levels and 7 frequency bands, as well as peak sum and accessory display. The high voltage P-channel drive transistors can drive up to 45 V. An on-chip power on reset circuit blanks the display outputs for 1/2 second after power up to eliminate power up noise on the display.

The XR-1095 is fabricated in a 3 micron double polysilicon CMOS process, resulting in accurate filters, tight gain tolerances and low noise. The nominal operating voltage is ±5VDC. The chip includes a self contained RC oscillator with a nominal frequency of 500kHz. Only an external resistor and capacitor are needed.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1095CP	42 Lead 600 Mil SDIP	-30°C to 75°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

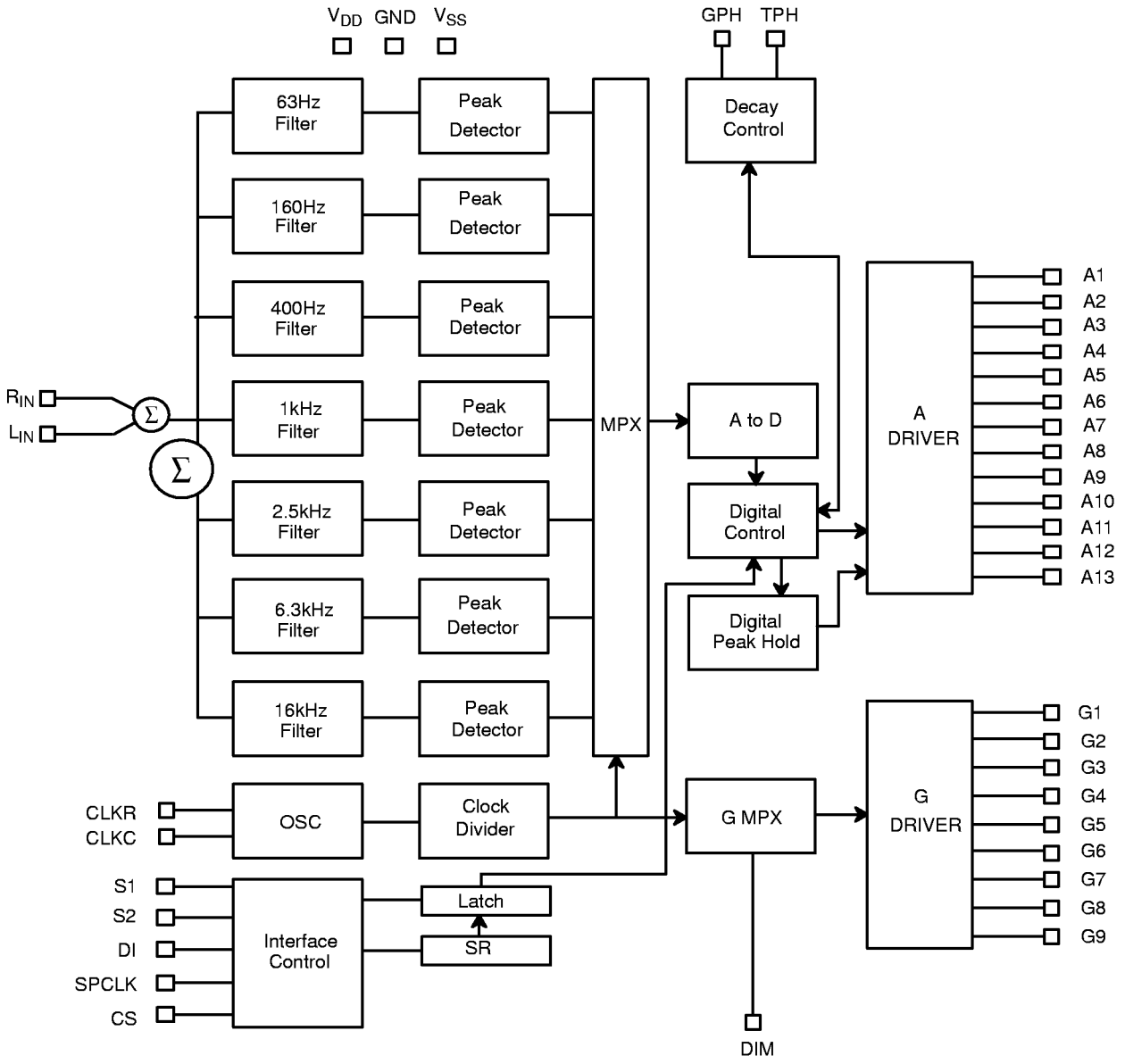
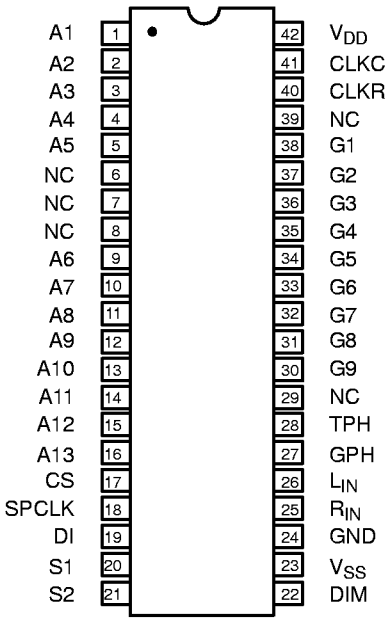


Figure 1. Block Diagram

PIN CONFIGURATION



42 Lead SDIP (0.600")

PIN DESCRIPTION

Pin#	Symbol	Description
1-5, 9-16	A1-A5 A6-A13	Display levels 1-13, indicating signal strength on G1-G8 and accessory display on G9.
6-8, 29, 39	NC	No Connect
		Time allocation for display function
38	G1	63Hz
37	G2	160Hz
36	G3	400Hz
35	G4	1kHz
34	G5	2.5kHz
33	G6	6.3kHz
32	G7	16kHz
31	G8	Total Output
30	G9	Accessory Display
25	R_{IN}	Right Channel Input
26	L_{IN}	Left Channel Input
22	DIM	Brightness control varies width of G outputs. Also accessible via microcontroller interface.
27	GPH	Filter amplitude display duration control. A resistor and timing capacitor from this pin to V_{ss} adjust peak hold decay time.

PIN DESCRIPTION (CONT'D)

Pin#	Symbol	Description
28	TPH	Filter amplitude display duration control. A resistor and timing capacitor from this pin to V_{ss} adjust peak hold decay time.
40	CLKR	Oscillator timing resistor between this pin and CLKC pin.
41	CLKC	Oscillator timing capacitor between this Pin and V_{ss}.
20	S1	Chip Select 1 Pin
21	S2	Chip Select 2 Pin
19	DI	Serial Port Data
18	SPCLK	Serial Port Clock
17	CS	Chip Select
42	V_{DD}	Plus Supply, Nominally 5VDC
23	V_{SS}	Minus Supply, Nominally -5VDC
24	GND	Analog Input Reference

DC ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} =+5V_{DC}, V_{SS}=-5V_{DC}, T_A=+25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	+Supply	4.5	5.0	6.0	VDC	
V_{SS}	-Supply	-4.5	-5.0	-6.0	VDC	
I_{DD}	Supply Current			19.5	mA	V_{DD}=5; V_{SS}=-5
I_{IL}	Input Leakage	-2		2	µA	Digital Inputs Analog Inputs
I_{OFF}	Output Off Leakage A & G Outputs			10	µA	V_{IN}=0V; V_D=-38V
V_{IH}	Digital Input High Voltage Threshold			2.4	VDC	
V_{IL}	Digital Input Low Voltage Threshold			.8	VDC	
F_{CLK}	Clock Frequency Accuracy	475	500	525	kHz	R=1.1kΩ C=1nF
f_O	Filter Center Frequency Accuracy	-7		+7	%	
F_{SPC}	Maximum Serial Port Clock Frequency			1.0	MHz	
t_{STRP}	Data Valid Before Serial Port Clock	100			nS	
t_{HOLD}	Data Valid After Serial Port Clock	0			nS	
t_{SPC}	Serial Port Clock Pulse Width	200			nS	
V_{OUTG}	All G Outputs	-1.0	2.5	5	V	V_{DD}=5V IGL=14mA
V_{OUTA}	All A Outputs	2.5	3.75	5	V	V_{DD}=5V IAL=2.5mA
F_{SS}	Flash Frequency		2		Hz	
t_F	Duty Factor		672 192		us us	Dim = 0 Dim = V+
t_D	Duty Cycle		1/11.4 1/39.5			Dim = 0 Dim = V+
TPH	Total Hold Time		0.5		S	R=100kΩ, C=1µf
GPH	Individual f_C Hold Time		0.5		S	R=100kΩ, C=1µf
A1[1]	-12dB	6	7	8	mvpk	
A2	-10dB	8	9.5	11	mvpk	
A3	-8dB	11	13	15	mvpk	
A4	-6dB	15	17	19	mvpk	
A5	-4dB	19	21	24	mvpk	
A6	-2dB	24	26.7	29	mvpk	

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
A7	-0dB	29	34	38	mvpk	
A8	+2dB	38	42	47.5	mvpk	
A9	+4dB	47.5	53	59.8	mvpk	
A10	+6dB	59.8	67	75.3	mvpk	
A11	+8dB	75.3	84	95	mvpk	
A12	+10dB	95	106	119	mvpk	
A13	+12dB	119	134	150	mvpk	

Notes
[1]Amplified levels are relative to V_{SS} at -5 volts nominal. Levels will vary linearly with voltage on V_{SS}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} 7VDC
V_{SS} . . . . . -7VDC
VDS of High Voltage P-Channel Driving Transistors:
Relative to V_{DD} . . . . . - 45 V

Power Dissipations (package limitation)
42 Pin Plastic Package 1W
Derate above 25°C . . . . . 9 mW/°C
Storage Temperature . . . . . -60°C to +150°C

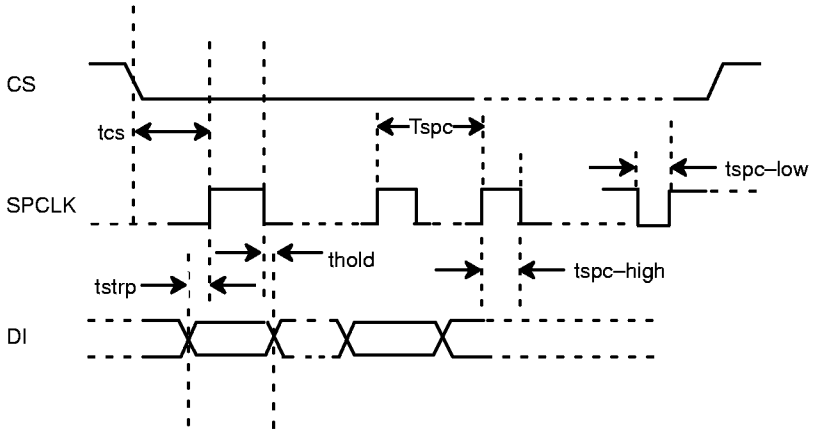


Figure 2. Serial Interface Port Timing Chart

tcs: Chip Select Valid Before Serial Port Clock (200 ns min)

tstrp: Data Valid Before Serial Port Clock (100 ns min)

thold: Data Valid After Serial Port Clock (0 ns min)

tspc: Serial Port Clock Pulse Width (200 ns min high or low)[1]

Fspc: Serial Port Clock Frequency (1 MHz max)

Tspc: Serial Port Clock Period (1 us min)

Notes
[1] tspc-high or tspc-low can be 200 ns min, but not both. Tspc must be 1 us min.

SERIAL PORT BIT MAP

b0		not used *
b4	b5	Accessory memo
0	0	off
1	0	on
*b9		Total peak hold
0		off
1		on

b10		Peak hold
0		off
1		on
b11		Accessory A1 control
0		on
1		off
b12		Set data/level display
0		Set data display GEQ
1		Set level display SPEANA

b13		Dimmer on/off
0		off
1		on

b1	b2	b3	Flash command data
0	0	0	No flash
1	0	0	f1 flash
0	1	0	f2 flash
1	1	0	f3 flash
0	0	1	f4 flash
1	0	1	f5 flash
0	1	1	f6 flash
1	1	1	f7 flash

b6	b7	b8	Accessory Mn control
0	0	0	off
1	0	0	M1
0	1	0	M2
1	1	0	M3
0	0	1	M4
1	0	1	M5
0	1	1	M6

b14	b15	Accessory display
0	0	off
1	0	Right
0	1	Left
1	1	MIX

b16 to b50 are set data for each filter

LSB	-	MSB	Filter
b16	-	b20	f1
b21	-	b25	f2
b26	-	b30	f3
b31	-	b35	f4
b36	-	b40	f5
b41	-	b45	f6
b46	-	b50	f7

*b9 low turns the total peak hold display off

LSB				MSB	Display
0	0	1	1	1	+12db
0	1	0	1	1	+10db
0	0	0	1	1	+8db
0	1	1	0	1	+6db
0	0	1	0	1	+4db
0	1	0	0	1	+2db
0	0	0	0	1	+0db
0	1	1	1	0	-2db
0	0	1	1	0	-4db
0	1	0	1	0	-6db
0	0	0	1	0	-8db
0	1	1	0	0	-10db
0	0	1	0	0	-12db

SERIAL PORT BIT MAP (CONT'D)

b51-b61 Key code (S1/S2 select)

S1	S2	b51	b52	b53	b54	b55	b56	b57	b58	b59	b60	b61	
0	0	0	0	0	1	0	0	1	1	1	1	1	Chip select 0
1	0	1	0	0	1	0	0	1	1	1	1	1	Chip select 1
0	1	0	1	0	1	0	0	1	1	1	1	1	Chip select 2
1	1	1	1	0	1	0	0	1	1	1	1	1	Chip select 2

** First bit loaded into the Serial port is bit b61, last bit loaded in is bit bϕ*

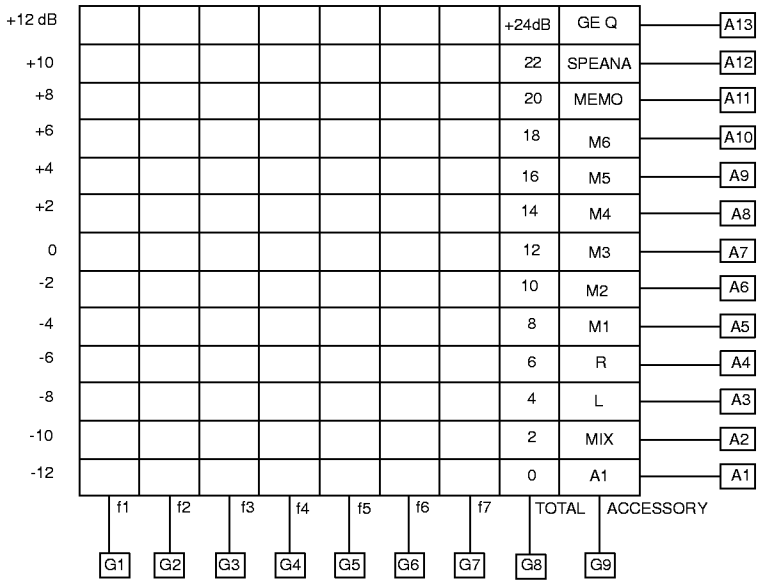


Figure 3. Typical Display

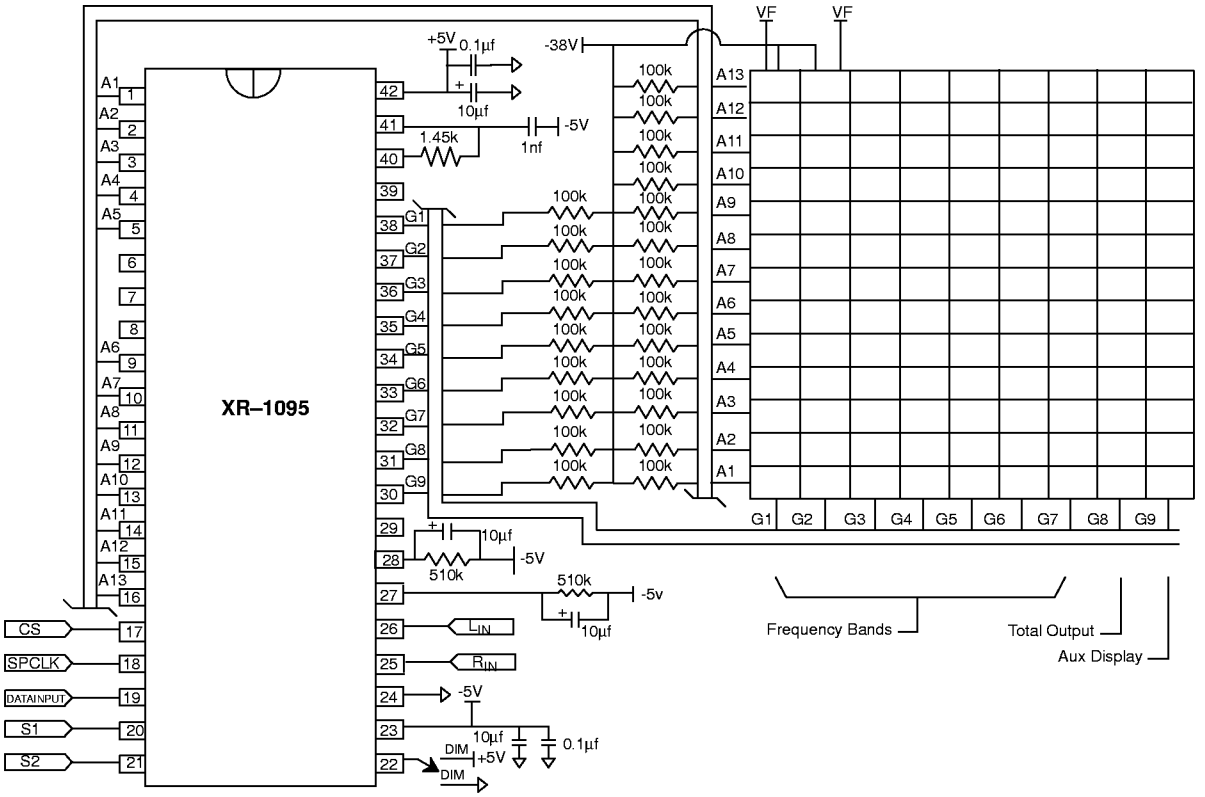
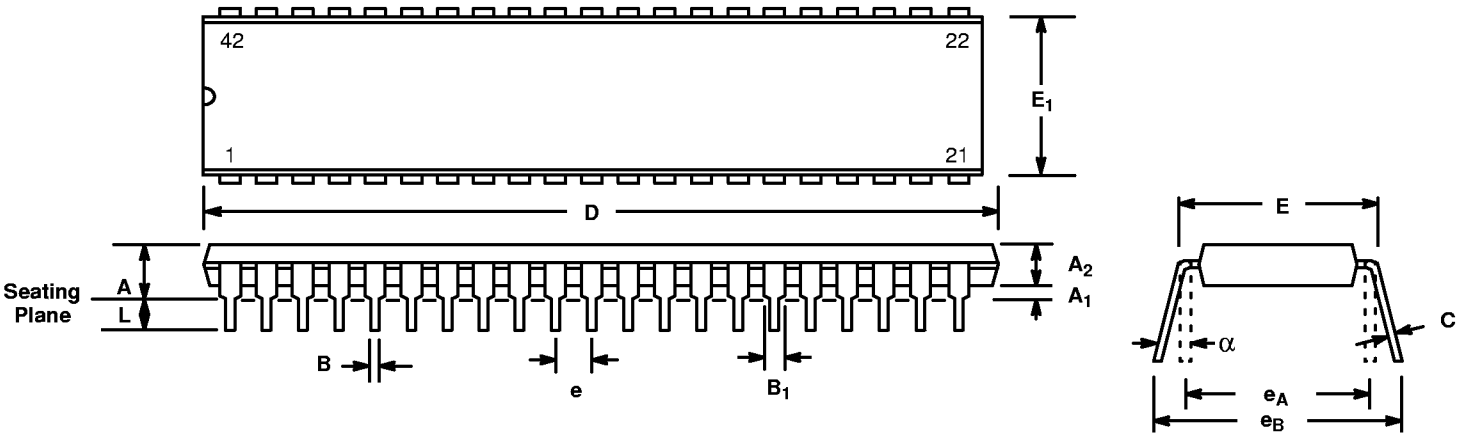


Figure 4. Typical Application Schematic

42 LEAD SHRINK PLASTIC DUAL-IN-LINE (600 MIL SDIP)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.150	0.200	3.81	5.08
A_1	0.020	0.070	0.51	1.78
A_2	0.120	0.180	3.05	4.57
B	0.014	0.023	0.35	0.59
B_1	0.030	0.055	0.75	1.42
C	0.008	0.014	0.20	0.36
D	1.460	1.540	37.08	39.12
E	0.600	0.624	15.24	15.87
E_1	0.500	0.570	12.70	14.48
e	0.070 BSC		1.78 BSC	
e_A	0.600 BSC		15.24 BSC	
e_B	0.600	0.700	15.24	17.78
L	0.100	0.150	2.54	3.40
α	0°	15°	0°	15°

Note: The control dimension is the inch column