Hard Disk Read/Write

GENERAL DESCRIPTION

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3½" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117, manufactured with a high speed bipolar process, operates on +5 V and +12 V.

FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor with Automatic Disable
TTL Compatible Inputs

APPLICATIONS

Single or Multiple Platter Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

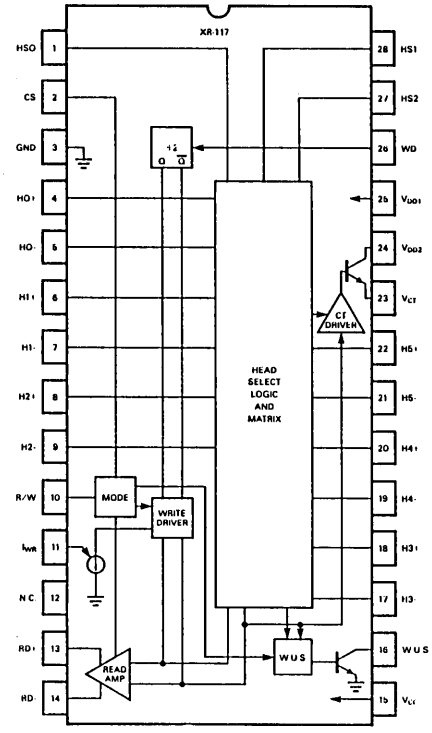
V_{DD1} and V_{DD2}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-117-2CP	Plastic	0°C to 70°C
XR-117-4CP	Plastic	0°C to 70°C
XR-117-6CP	Plastic	0°C to 70°C
XR-117-xCN	Ceramic	0°C to 70°C
XR-117-xCQ*	Surface Mount Quad	0°C to 70°C
XR-117-xMD*	Surface Mount	0°C to 70°C
XR-117-x *	PLCC	0°C to 70°C

x = 2, 4, or 6, depending on number of heads required
* = contact factory for availability

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

Four major blocks comprise the XR-117: a multiplexer for head selection, write data control circuitry, read signal amplifiers and buffers, and a power supply monitor that disables the device whenever improper supply voltages are present. Designed for six read/write heads, the XR-117 is also available in smaller packages for systems requiring only two or four heads. The 30 MHz minimum bandwidth facilitates data rates exceeding 25 Mbits per second.

Less than 2 $nV/\sqrt{Hz}$ (nominal) noise allows error free operation with small input signals. Up to 50 mA of write current output means the disk signal can be large, further enhancing the readback signal-to-noise ratio for very low error rates.

Cascading multiple XR-117s is accomplished by alternately enabling and disabling devices via the chip select (CS) pin. Guaranteed write current tolerances allow close write matching between devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 3.1$ kΩ, $L_h = 10$ μH, $R_d = 750$ Ω, C_L (R_{D+}, R_{D-}), ≤ 20 pF, Data Rate = 5 MHz.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			25	mA	V_{DD} = 13.2 V, Idle Mode
				50	mA	V_{DD} = 13.2 V, Read Mode
				30	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
P_D	Power Dissipation			400	mW	V_{CC} - 5.5 V, V_{DD} = 13.2 V, Idle Mode
				600	mW	Read Mode
				700	mW	Write Mode, I_W = 50 mA, R_{CT} = 130 Ω
				1050	mW	Write Mode, I_W = 50 mA, R_{CT} = 0 Ω
V_{CT}	Center Tap Voltage		4.0		V	
			6.0		V	
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.1	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	μA	V_{OH} = 5 V
DIGITAL INPUTS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input Current, Low	−0.4			mA	
I_{IH}	Input Current, High			100	μA	
WRITE CHARACTERISTICS						
	Write Current Accuracy	−5		+5	%	Note 1
I_W	Recommended Write Current Range	10	45	50	mA	
	Differential Head Voltage Swing	5.7	10		Vpeak	
	Unselected Differential Head Current			2	mApeak	
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			kΩ	
	WD Rate (Transisition Frequency)	125	500	625	kHz	
K_I	Current Source Factor		20			$K_I = I_W$/(Current through R_W)

READ CHARACTERISTICS						
A_V	Differential Voltage Gain	80	100	120	V/V	V_{in} = 1 mVp-p @ 300 kHz $R_{L+} = R_{L-}$ = 1 kΩ
R_{in}	Differential Input Resistance	2			kΩ	
C_{in}	Differential Input Capacitance			23	pF	f = 5 MHz
e_{ni}	Input Noise Voltage		1.5	2.1	$nV/\sqrt{Hz}$	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	55		MHz	−3dB point $\|Zs\| < 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current			45	μA	
CMRR	Common Mode Rejection Ratio	50			dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45			dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2}, or V_{CC}
	Channel Separation	45			dB	Unselected Channel: V_{in} = 100 mVp-p at 5 MHz Selected Channel: V_{in} = 0 V
	Output Offset Voltage	−480	± 50	480	mV	
V_{CM}	Common Mode Output Voltage	5	6	7	V	
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	μS	**Note 2**
	Write to Read		0.1	1	μS	Note 3, Note 4
CS CS	Start-Up Delay		0.1	1	μS	Delay to 90% of I_W or to 90% of 100 mV 10 MHz read signal envelope.
	Inhibit Delay		0.1	1	μS	Note 4
	Head Switching Delay		0.1	1	μS	Note 3 Switching between any heads.
WUS	Write Unsafe Safe to Unsafe	1.6	2.5	8.0	μS	I_W = 50 mA, See Fig. 1, TD1
	Unsafe to Safe		0.2	1	μS	I_W = 20 mA, See Fig. 2, TD2
I_W	Head Current					
	Propagation Delay		4	25	nS	L_h = 0 μH, R_h = 0 Ω, Note 5,
	Asymmetry			2	nS	Note 6 See Fig. 1, TD3
	Rise or Fall Time		9	20	nS	10% to 90% or 90% to 10% points

Note 1: Error from $I_W = \frac{140}{R_W}(\frac{V}{\Omega})$
Note 2: Delay to 90% of I_W
Note 3: Delay to 90% of 100 mVp-p 10 MHz read single envelope
Note 4: Delay to 90% decay of I_W
Note 5: From 50% points
Note 6: Input WD has 50% duty cycle and 1 nS rise and fall times.

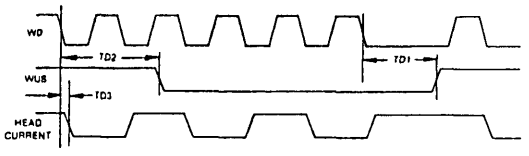


Figure 1. Write Mode Timing Diagram

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/W) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak signal amplitude and provides low output impedance.

APPLICATIONS INFORMATION

As will all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-117 is available in small outline surface mount and flat-pak packages facilitating installation near the drive heads. Its high frequency characteristics lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

The V_{CC} supply monitor disables writing when V_{CC} drops below about 4 V.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage drop then is across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\ (\frac{55}{I_W})$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small outline packages. For low write currents, R_{CT} may be deleted, with V_{DD2} directly connected to the supply.

In addition to the individual head damping resistors, a ferrite bead around the V_{CT} line to the heads will further reduce overshoot and ringing in extreme conditions.

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low, are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditons also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of about 2 kΩ is necessary for operation of this open collector output.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 30 MHz minimum bandwidth and low noise characteristics (1.5nV/$\sqrt{Hz}$ typical) provide substantial margins in most drives. The ouput should be AC coupled to delete the approximately 6 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.