Dual Operational Transconductance Amplifier

GENERAL DESCRIPTION

The XR-13600 is a dual operational transconductance (Norton) amplifier with predistortion diodes and non-committed Darlington buffer outputs.

The device is especially suitable for electronically controllable gain amplifiers, controlled frequency filters, an other applications requiring current or voltage adjustments.

FEATURES

Direct Replacement for LM-13600 and LM-13600 A
Transconductance Adjustable Over 4 Decades
Excellent Transconductance-Control Linearity
Uncommitted Darlington Output Buffers
On-Chip Predistortion Diodes
Excellent Matching Between Amplifiers
Wide Supply Range: ±2V to ±18V

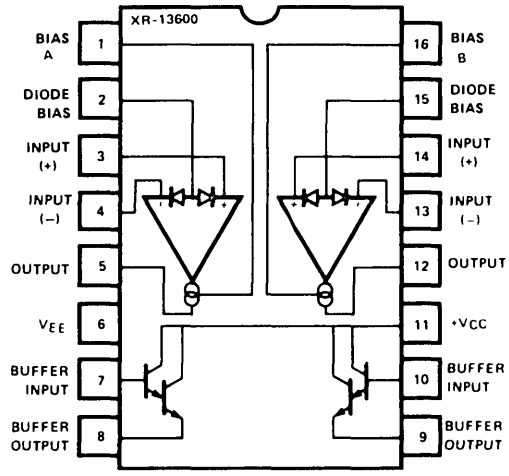
APPLICATIONS

Current-Controlled Amplifiers
Current-Controlled Impedances
Current-Controlled Filters
Current-Controlled Oscillators
Multipliers/Attenuators
Sample and Hold Circuits
Electronic Music Synthesis

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (See Note 1)	±22 V
Power Dissipation (T_A = 25°C, see Note 2)	625 mW
Derate Above 25°C	5 mW/°C
DC Input Voltage	$+V_{CC}$ to $-V_{EE}$
Differential Input Voltage	±5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_B)	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-13600AP	Plastic	0°C to + 70°C
XR-13600CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-13600 consists of two programmable transconductance amplifiers with high input impedance and push-pull outputs. The two amplifiers share common supplies but otherwise operate independently. Each amplifier's transconductance is directly proportional to its applied bias current. To improve signal-to-noise performance, predistortion diodes are included on the inputs; the use of these diodes results in a 10 dB improvement referenced to 0.5% THD. Independent Darlington emitter followers are included to buffer the outputs.

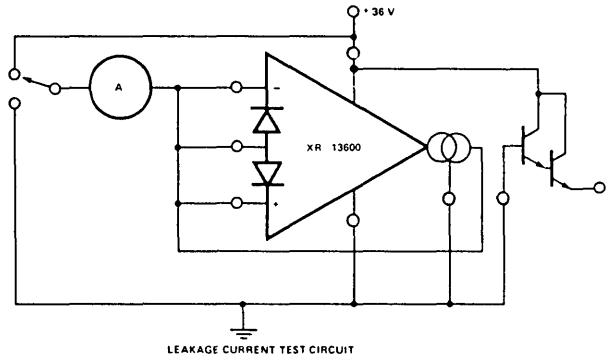
XR-13600

ELECTRICAL CHARACTERISTICS

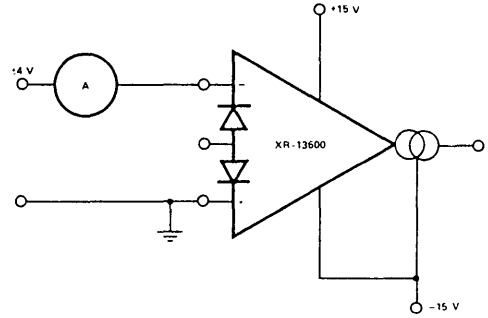
Test Conditions: T_A = +25°C, Supply Voltage = ±15V, unless otherwise specified.

PARAMETERS	XR-13600A			XR-13600C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage (V_{OS})		0.4	2		0.4	5	mV	
			5				mV	Over Temperature Range
		0.3	2		0.3	5	mV	I_B = 5μA
V_{OS} Including Diodes		0.5	2		0.5	5	mV	Diode Bias Current (I_D) = 500 μA
Input Offset Change		0.1	3		0.1		mV	5μA ≤ I_B ≤ 500μA
Input Offset Current		0.1	0.6		0.1	0.6	μA	
Input Bias Current		0.4	5		0.4	5	μA	T_A = 25°C
		1	7		1	8	μA	Over Temperature Range
Forward Transconductance (g_m)	7700	9600	12000	6700	9600	13000	μmho	T_A = 25°C
	4000			5400			μmho	Over Temperature Range
g_m Tracking		0.3			0.3		dB	
Peak Output Current	3	5	7		5		μA	RL = 0, I_B = 5μA
	350	500	650	350	500	650	μA	RL = 0, I_B = 500μA
	300			300			μA	RL = 0, Over Specified Temp Range
Peak Output Voltage								
Positive	+12	+14.2		+12	+14.2		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Negative	−12	−14.4		−12	−14.4		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Supply Current		2.6			2.6		mA	I_B = 500 μA, Both Channels
V_{OS} Sensitivity								
Positive		20	150		20	150	μV/V	Δ V_{OS}/Δ V +
Negative		20	150		20	150	μV/V	Δ V_{OS}/Δ V −
CMRR	80	110		80	110		dB	
Common Mode Range	±12	±13.5		±12	±13.5		V	Referred to Input (Note 5)
Channel Separation		100			100		dB	20 Hz < f < 20 KHz
Diff. Input Current		0.02	10		0.02	100	nA	I_B = 0, Input = ±4 V
Leakage Current		0.2	5		0.2	100	nA	I_B = 0 (refer To Test Circuit)
Input Resistance	10	26		10	26		KΩ	
Open Loop Bandwidth		2			2		MHz	
Slew Rate		50			50		V/μSec	Unity Gain Compensated
Buff. Input Current		0.4	5		0.4	5	μA	(Note 5)
Peak Buffer Output Voltage	10			10			V	(Note 5)

TEST CIRCUITS



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

Note 1. For selections to a supply voltage above ±22 V, contact factory.

Note 2. For operating at high temperatures, the device may be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

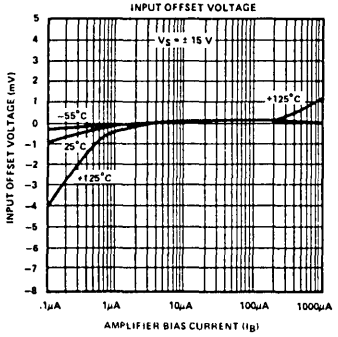
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_{CC} = V_{EE} = 15V, T_A = 25°C, amplifier bias current (I_B) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

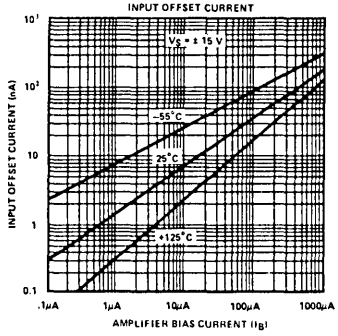
Note 5. These specifications apply for V_{CC} = V_{EE} = 15 V, I_B = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_{EE}$ and the input of the buffer is connected to the transconductance amplifier output.

TYPICAL PERFORMANCE CHARACTERISTICS

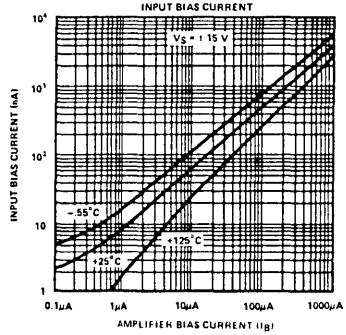
INPUT OFFSET VOLTAGE



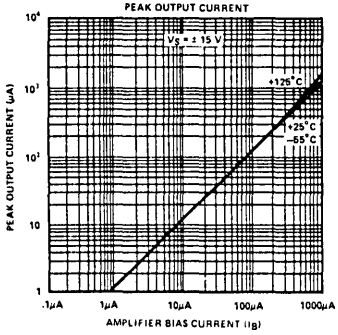
INPUT OFFSET CURRENT



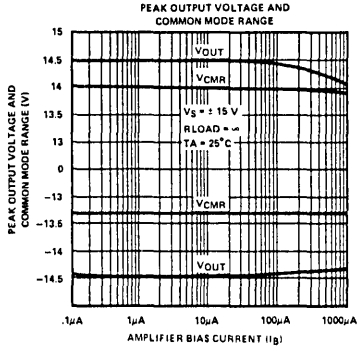
INPUT BIAS CURRENT



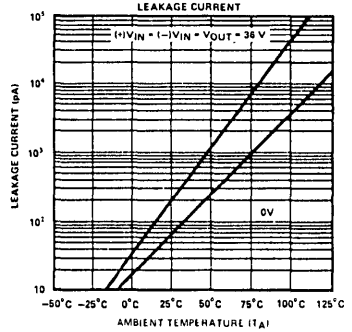
PEAK OUTPUT CURRENT



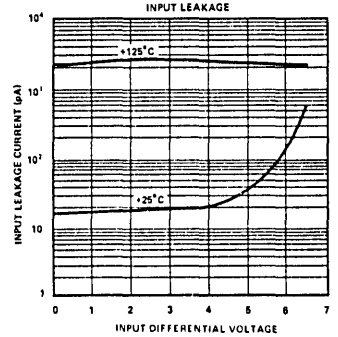
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



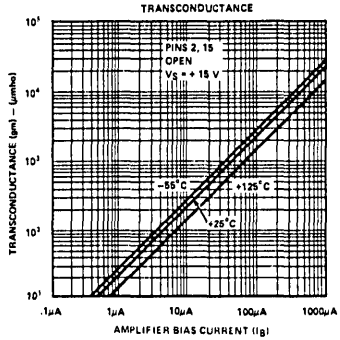
LEAKAGE CURRENT



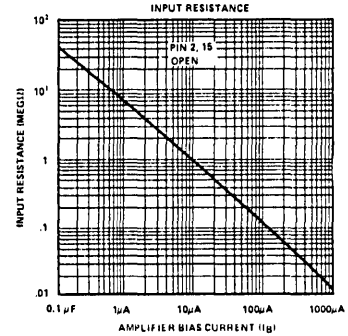
INPUT LEAKAGE



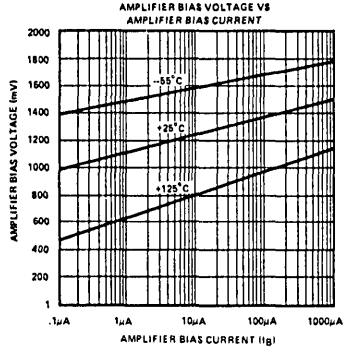
TRANSCONDUCTANCE



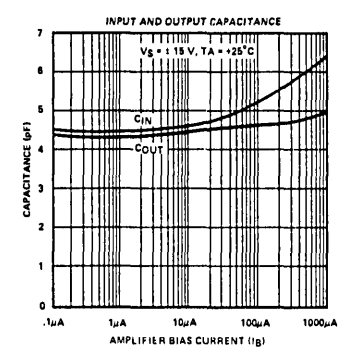
INPUT RESISTANCE



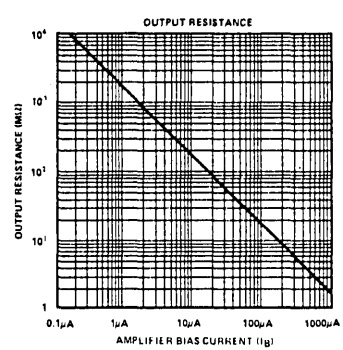
AMPLIFIER BIAS VOLTAGE VS AMPLIFIER BIAS CURRENT



INPUT AND OUTPUT CAPACITANCE



OUTPUT RESISTANCE



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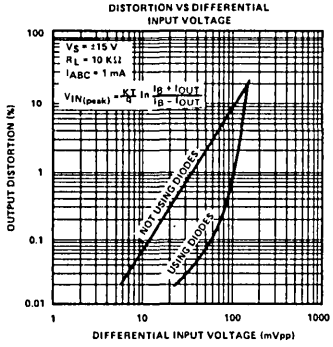
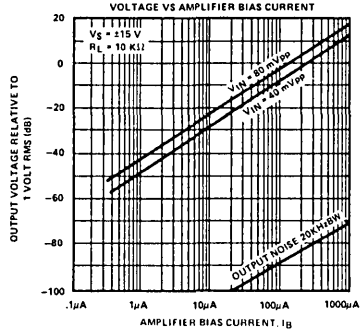
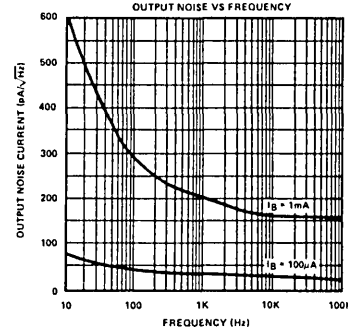
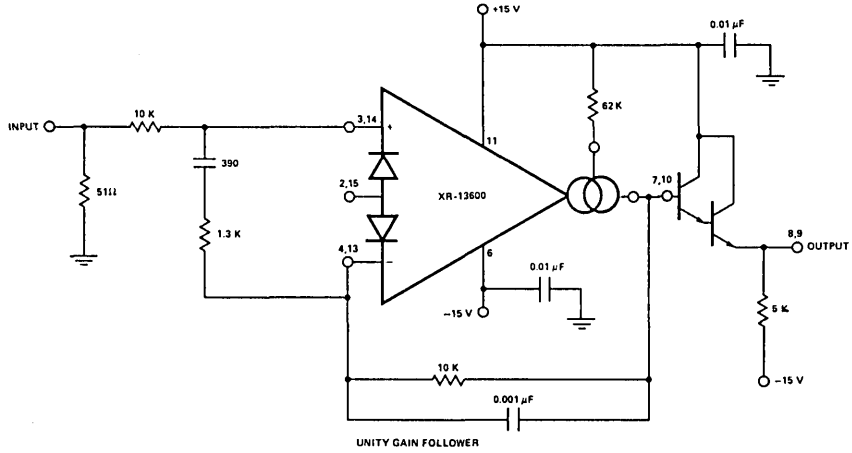
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)







TYPICAL CIRCUIT CONNECTION



CIRCUIT DESCRIPTION

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_B;

$$I_4 + I_5 = I_B \qquad (2)$$

where I_B is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the 1n function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_B}{2}$$

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_B.

LINEARIZING DIODES

For differential voltages greater than a few millivolts, Equation 3 is no longer accurate, and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is the form of current I_S. Since the sum of I_4 and I_5 is I_B and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_B}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_B}{2} + \frac{I_{OUT}}{2}$$

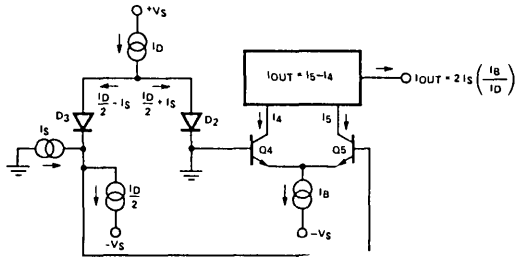


Figure 1. Linearizing Diodes

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} 1n \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} 1n \frac{\frac{I_B}{2} + \frac{I_{out}}{2}}{\frac{I_B}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_B}{I_D}\right) \text{ for } |I_S| < \frac{I_D}{2} \qquad (6)$$

Notice that in deriving Equation 6, no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

CONTROLLED IMPEDANCE BUFFERS

The upper limit of transconductance is defined by the maximum value of I_B (2 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_B, a buffer which has very low input bias current is desirable. A FET follower satisfies the low input current requirement, but is some what non-linear for large voltage wing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_B, the buffer's input current is minimal. At higher levels of I_B, transistor Q_3 biases up to Q_{12} with a current proportional to I_B for fast slew rate.

APPLICATIONS

VOLTAGE CONTROLLED AMPLIFIERS (VCA)

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Therenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

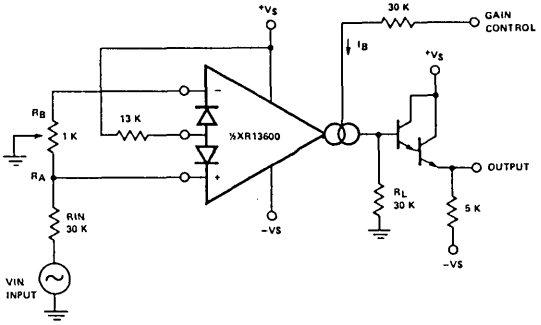


Figure 2. Voltage Controlled Amplifier (VCA) Circuit

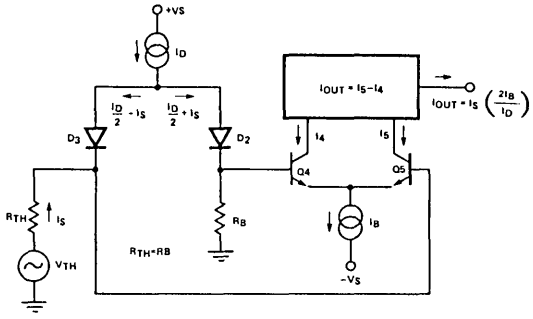


Figure 3. Equivalent VCA Input Circuit

For optimum signal-to-noise performance, I_B should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

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XR-13600

STEREO VOLUME CONTROL

The circuit of Figure 4 uses the excellent matching of the two XR-13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_B \text{ (mA)}$$

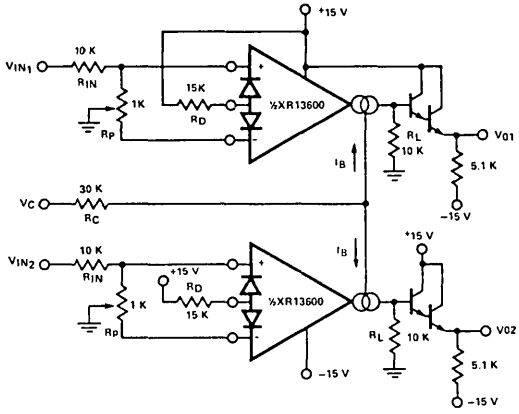


Figure 4. Stereo Volume Control

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_B) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V = 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2(V + 1.4\ V)$ into I_O. The circuit of Figure 6 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that V_O = OV for V_{IN2} = OV. R_M also serves as the load resistor for I_O.

Noting that the gain of the XR-13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_B, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

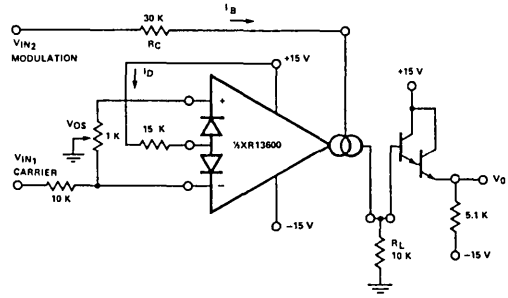


Figure 5. Amplitude Modulator

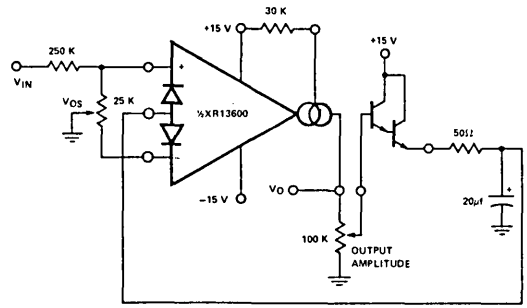


Figure 6. Four-Quadrant Multiplier

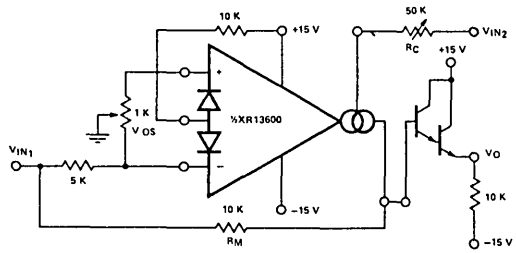


Figure 7. AGC Amplifier

VOLTAGE CONTROLLED RESISTORS (VCR)

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the XR-13600 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2\ I_B$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the XR-13600 input.

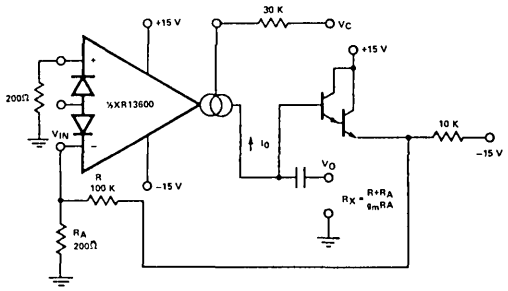


Figure 8. Voltage Controlled Resistor, Single-Ended

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the nose performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the XR-13600.

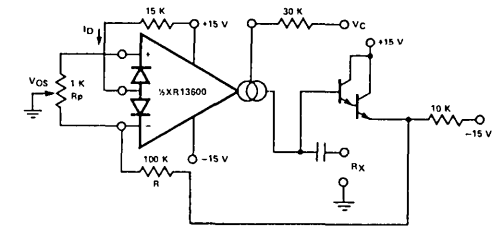


Figure 9. Voltage Controlled Resistor with Linearizing Diodes

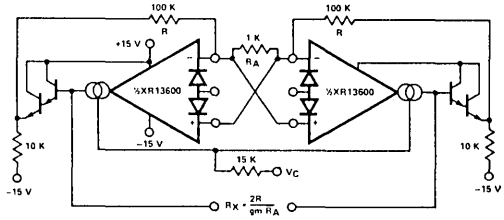


Figure 10. Floating Voltage Controlled Resistor

VOLTAGE CONTROLLED FILTERS

OTA's are extremely useful for implementing voltage controlled filters, with the XR-13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation, where g_m is again 19.2 $\times$ I_B at room temperature.

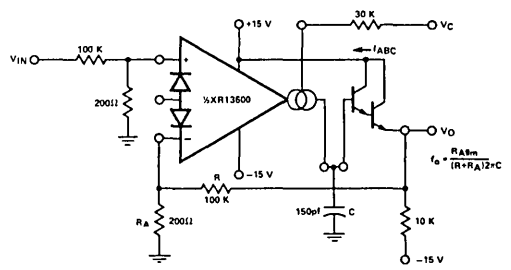


Figure 11. Voltage Controlled Low-Pass Filter

Figure 12 shows a voltage controlled high-pass filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

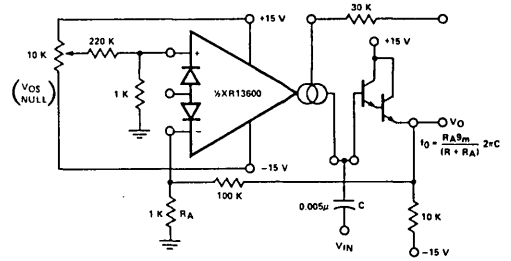


Figure 12. Voltage Controlled High-Pass Filter

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth lowpass filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

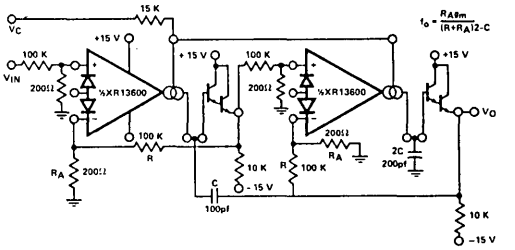


Figure 13. Voltage Controlled 2-Pole Butterworth Low-Pass Filter

VOLTAGE CONTROLLED OSCILLATORS (VCO)

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the XR-13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

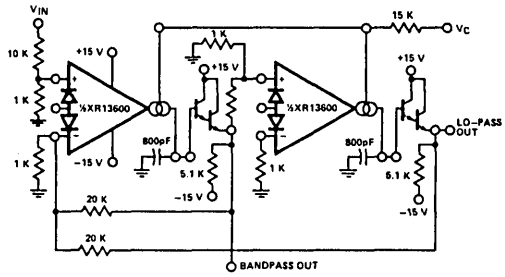


Figure 14. Voltage Controlled State Variable Filter

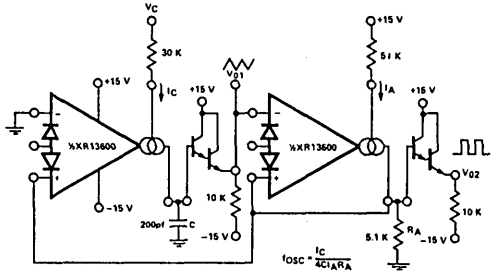


Figure 15. Triangular/Square-Wave VCO

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

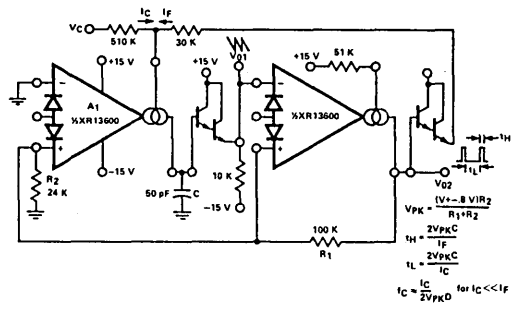


Figure 16. Ramp/Pulse VCO

The voltage-controlled low-pass filter of Figure 11 may be used to design a high-quality sinusoidal VCO. The circuit of Figure 17 employs two XR-13600 packages, with three of the amplifiers configured as low-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

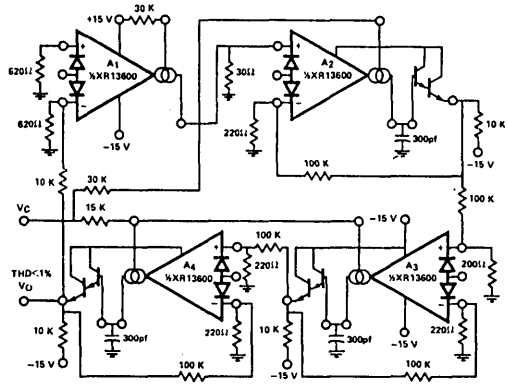


Figure 17. Sinusoidal VCO Using Two XR-13600 Circuits

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

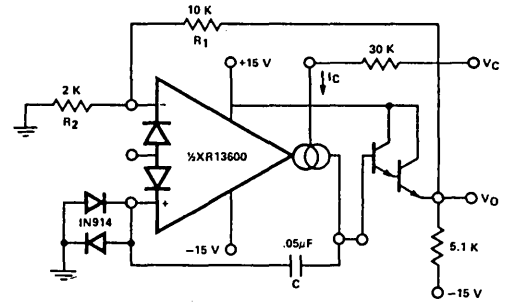


Figure 18. Single Amplifier VCO

ADDITIONAL APPLICATIONS

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches it output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

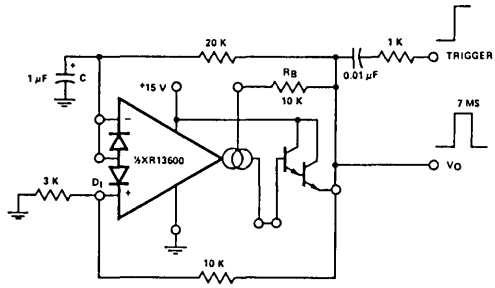


Figure 19. Timer With Zero Stand-By Power

The operation of the multiplexer of Figure 20 is very straight-forward. When A_1 is turned on it holds V_O equal to V_{IN1} and when A_2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A_1 and A_2. The maximum clock rate is limited to about 200 kHz by the XR-13600 slew rate into 150 pF when the ($V_{IN1} - V_{IN2}$) differential is at its maximum allowable value of 5 volts.

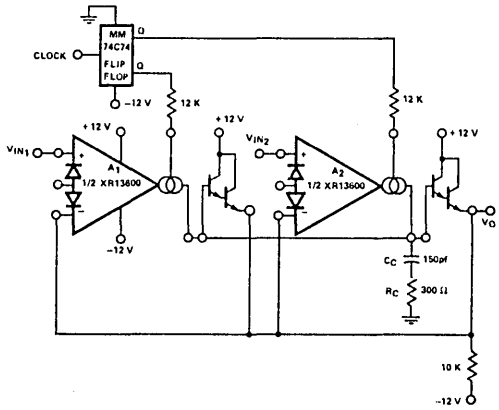


Figure 20. Multiplexer

The phase-locked loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the VCO of Figure 18 to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

The Schmitt trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$ will produce a Schmitt trigger with variable hysteresis.

Figure 23 shows a tachometer or frequency-to-voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H

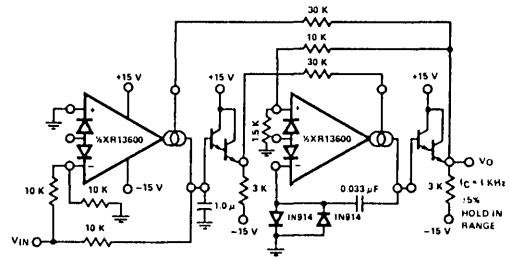


Figure 21. Phase-Locked Loop

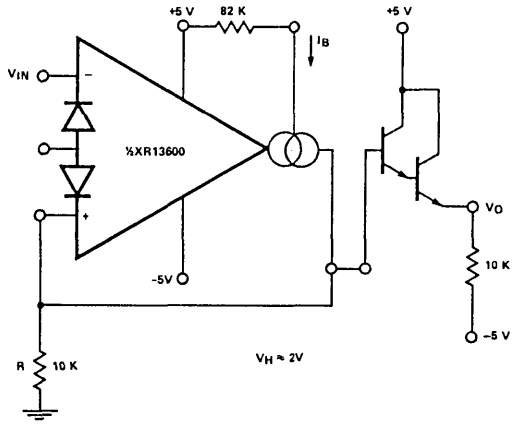


Figure 22. Schmitt Trigger

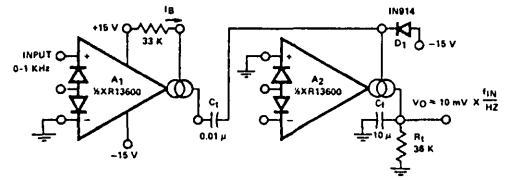


Figure 23. Tachometer

represent the maximum low and maximum high output voltage swing of the XR-13600. D1 added to provide a discharge path for C_t and A_1 switches low.

The sample-hold circuit of Figure 24 also requires that the Darlington buffer used be from the other (A_2) half of the package and that the corresponding amplifier be biased on continuously.

The peak detector of Figure 25 uses A_2 to turn on A_1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A_2 since the A_1 Darlington will be turned on and off with A_1. Pulling the output of A_2 low through D_1 serves to turn off A_1 so that V_O remains constant.

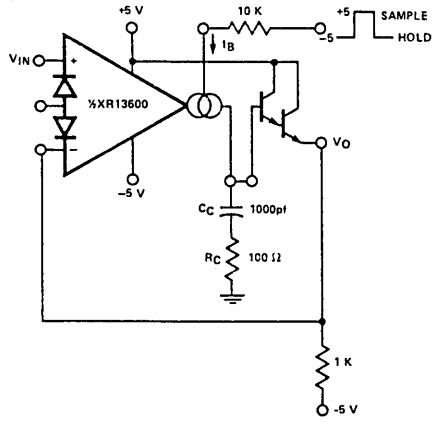


Figure 24. Sample-Hold Circuit

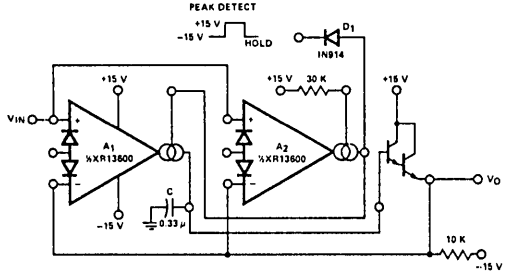


Figure 25. Peak Detector and Hold Circuit

The ramp-and-hold of Figure 26 sources I_B into capacitor C whenever the input to A_1 is brought high, giving a ramp-rate of about IV/ms for the component values shown.

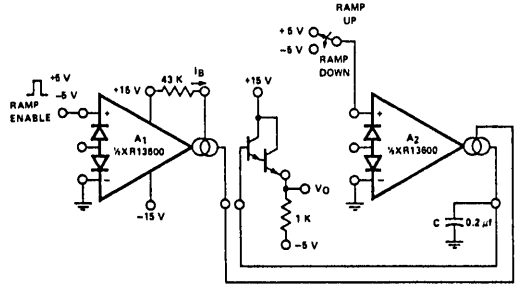


Figure 26. Ramp and Hold Circuit

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A_1 is constant. The output power of amplifier A_1 is monitored by squaring amplifier A_2 and the average compared to a reference voltage with amplifier A_3. The output of A_3 provides bias current to the diodes of A_1 to attenuate the input signal. Because the output power of A_1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A_4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A_4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

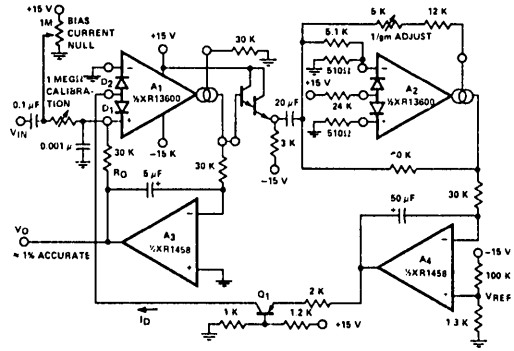


Figure 27. True RMS Converter Circuit

The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 KΩ potentiometer adjusts the output voltage which has a positive TC above 1.2 volts, zero TC at about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A_2 transfer function against the complementary TC of D_1.

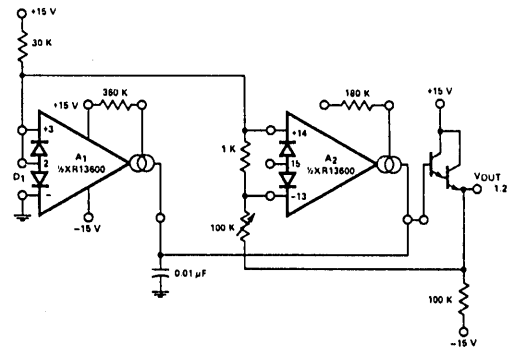


Figure 28. Delta V_{BE} Reference

The log amplifier of Figure 29 responds to the ratio of current thru buffer transistors Q_3 and Q_4. Zero temperature dependence for V_{OUT} is ensured in that the TC of the A_2 transfer function is equal and opposite to the TC of the logging transistors Q_3 and Q_4.

The wide dynamic range of the XR-13600 allows easy control of the output pulse width in the pulse-width modulator of Figure 30.

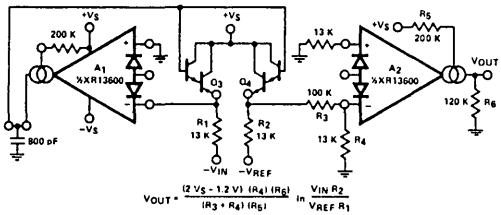


Figure 29. Log Amplifier

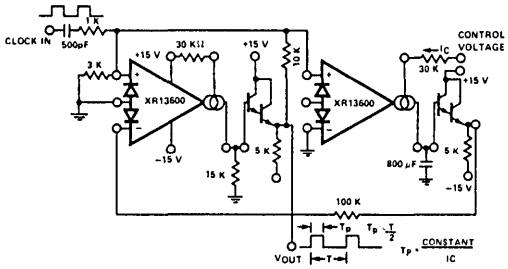


Figure 30. Pulse Width Modulator

For generating I_B over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A_2 is held equal to Oy, the output current of A_1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q_1 and Q_2 is attenuated by the R_1, R_2 network so that A_1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A_1 is:

$$V_{IN1} = \frac{-2KTI_3}{qI_2} = \frac{2KTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2)\,V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q} \ln \frac{I_B}{I_1}$$

Combining and solving for I_B yields:

$$I_B = (I_1) \exp\left[\frac{2(R_1 + R_2)\,V_C}{I_2R_1R_C}\right]$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

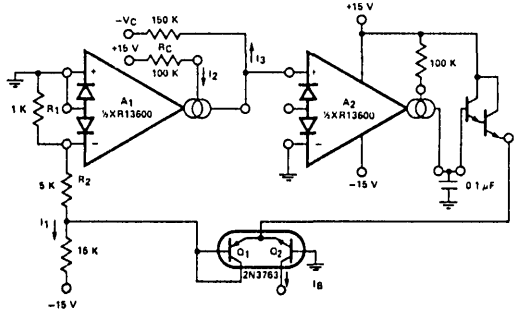
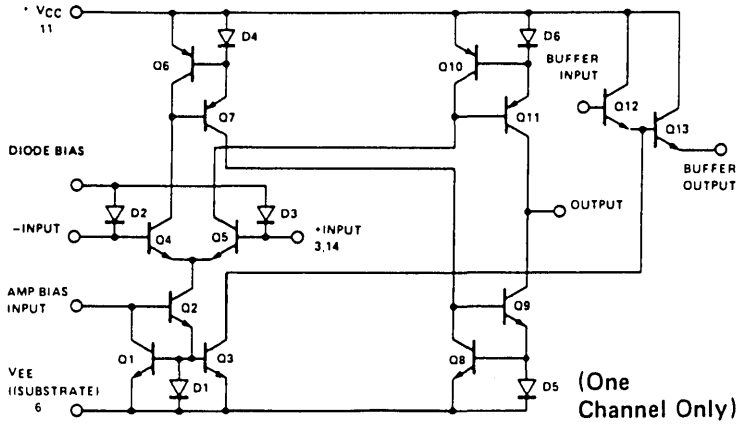


Figure 31. Logarithmic Current Source



EQUIVALENT SCHEMATIC DIAGRAM