Pulse-Width Modulating Regulators

GENERAL DESCRIPTION

The XR-1525A/1527A is a series of monolithic integrated circuits that contain all of the control circuitry necessary for a pulse-width modulating regulator. Included in the 16-Pin dual-in-line package is a voltage reference, an error amplifier, a pulse-width modulator, an oscillator, under-voltage lockout, soft-start circuitry, and output drivers.

The XR-1525A/2525A/3525A series features NOR logic, giving a LOW output for an OFF state. The XR-1527A/2525A/3527A series features OR logic, giving a HIGH output for an OFF state.

FEATURES

8V to 35V Operation
5.1V Reference Trimmed to ±1%
100 Hz to 500 kHz Oscillator Range
Separate Oscillator Sync Terminal
Adjustable Deadtime Control
Internal Soft-Start
Input Under-voltage Lockout
Latching PWM to Prevent Double Pulsing
Dual Source/Sink Output Drivers
  Capable of Over 200 mA
Power-FET Drive Capability

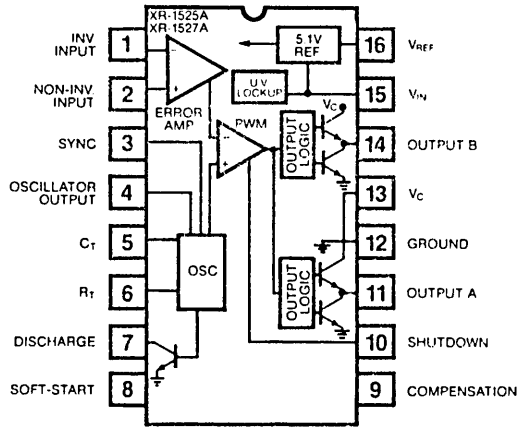
APPLICATIONS

Power Control Systems
Switching Regulators
Industrial Controls

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+ V_{IN})	+40V
Collector Supply Voltage (V_C)	+40V
Logic Inputs	−0.3V to 5.5V
Analog Inputs	−0.3V to +V_{IN}
Output Current, Source or Sink	500 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above T_A = +25°C	8.0 mW/°C
Plastic Package	625 mW
Derate above T_A = +25°C	5.0 mW/°C
Operating Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1525A/27M	Ceramic	−55°C to +125°C
XR-2525A/27AN	Ceramic	−25°C to +85°C
XR-2525A/27AP	Plastic	−25°C to +85°C
XR-3525A/27CN	Ceramic	0°C to +70°C
XR-3525A/27CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The on-chip 5.1-volt reference is trimmed to ±1% initial accuracy, and the common-mode input range of the error amplifier is extended to include the reference voltage. Deadtime is adjustable with a single external resistor. A sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external clock. A positive-going signal applied to the shutdown pin provides instantaneous turnoff of the outputs. The under-voltage lockout circuitry keeps the output drivers off, and the soft-start capacitor discharged, for an input voltage below the required value. The latch on the PWM comparator insures the outputs are active only once per oscillator period, thereby eliminating any double pulsing. The latch is reset with each clock pulse.

The output drivers are totem-pole designs capable of sinking and sourcing over 200 mA.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{IN} = +20V, T_J = Full operating temperature range, unless otherwise specified.

PARAMETERS	XR-1525A/2525A XR-1527A/2527A			XR-3525A XR-3527A			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
VOLTAGE REFERENCE SECTION								
Output Voltage	5.05	5.10	5.15	5.00	5.10	5.20	V	T_J = 25°C
Line Regulation		10	20		10	20	mV	V_{IN} = 8V to 35V
Load Regulation		20	50		20	50	mV	I_L = 0 to 20 mA
Temperature Stability (2)		20	50		20	50	mV	T_J = Full Operating Range
Total Output Variation (2)	5.00		5.20	4.95		5.25	V	Line, Load and Temperature
Output Short Circuit Current		80	100		80	100	mA	T_J = 25°C, V_{ref} = 0V
Output Noise Voltage (2)		40	200		40	200	μV rms	T_J = 25°C, 10 Hz ≤ f ≤ 10 kHz
Long Term Stability (2)		20	50		20	50	mV/kHR	T_J = 125°C
OSCILLATOR SECTION (Note 3)								
Initial Accuracy (2,3)		±2	±6		±2	±6	%	T_J = 25°C, f = 40 kHz
Temperature Stability (2)		±3	±6		±3	±6	%	T_J = Full Operating Range
Input Voltage Stability (2,3)		±0.3	±1		±1	±2	%	V_{IN} = 8V to 35V
Minimum Frequency			100			100	Hz	R_T = 150 kΩ, C_T = 0.1 μF
Maximum Frequency	400			400			kHz	R_T = 2 kΩ, C_T = 1 nF
Current Mirror	1.7	2.0	2.2	1.7	2.0	2.2	mA	I_{RT} = 2 mA
Clock Amplitude (2,3)	3.0	3.5		3.0	3.5		V	
Clock Pulse Width (2,3)	0.3	0.5	1.0	0.3	0.5	1.0	μsec	T_J = 25°C, R_D = 0Ω
Sync Threshold	1.2	2.0	2.8	1.2	2.0	2.8	V	
Sync Input Current		1.0	2.5		1.0	2.5	mA	Sync Voltage = 3.5V
ERROR AMPLIFIER SECTION (V_{CM} = 5.1V)								
Input Offset Voltage		0.5	5.0		2	10	mV	
Input Bias Current		1	10		1	10	μA	
Input Offset Current			1			1	μA	
DC Open-Loop Gain	60	75		60	75		dB	R_L ≥ 10 MΩ
Gain Bandwidth Product (2)	1	2		1	2		MHz	T_J = 25°C
Output Low Voltage		0.2	0.5		0.2	0.5	V	
Output High Voltage	3.8	5.6		3.8	5.6		V	
Common-Mode Rejection Ratio	60	75		60	75		dB	V_{CM} = 1.5V to 5.2V
Supply Voltage Rejection Ratio	50	60		50	60		dB	V_{IN} = 8V to 35V
PULSE-WIDTH MODULATING COMPARATOR								
Minimum Duty Cycle			0			0	%	
Maximum Duty Cycle	45	49		45	49		%	
Input Threshold (3)	0.6	0.9		0.6	0.9		V	Zero Duty Cycle
Input Threshold (3)		3.3	3.6		3.3	3.6	V	Maximum Duty Cycle
Input Bias Current (2)		0.05	1.0		0.05	1.0	μA	
SOFT-START SECTION								
Soft-Start Current	25	50	80	25	50	80	μA	$V_{shutdown}$ = 0V
Soft-Start Voltage		0.4	0.6		0.4	0.6	V	$V_{shutdown}$ = 2V
Shutdown Input Current		0.4	1.0		0.4	1.0	mA	$V_{shutdown}$ = 2.5V
OUTPUT DRIVERS (Each Output) V_C = 20V								
Output Low Voltage		0.2	0.4		0.2	0.4	V	I_{sink} = 20 mA
Output Low Voltage		1.0	2.0		1.0	2.0	V	I_{sink} = 100 mA
Output High Voltage	18	19		18	19		V	I_{source} = 20 mA
Output High Voltage	17	18		17	18		V	I_{source} = 100 mA
Under-voltage Lockout	6	7	8	6	7	8	V	V_{comp} and V_{SS} = High
Collector Leakage (4)			200			200	μA	V_C = 35V
Rise Time (2)		100	600		100	600	nsec	T_J = 25°C, C_L = 1 nF
Fall Time (2)		50	300		50	300	nsec	T_J = 25°C, C_L = 1 nF
Shutdown Delay (2)		0.2	0.5		0.2	0.5	μsec	V_{SD} = 3V, C_S = 0, T_J = 25°C
TOTAL STANDBY CURRENT								
Supply Current		14	20		14	20	mA	V_{IN} = 35V

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3: Tested at f = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0Ω).
Note 4: Applies to XR-1525A/2525A/3525A only, due to polarity of output pulses.

PRINCIPLES OF OPERATION

The different control blocks within the XR-1525A/1527A function as follows:

Voltage Reference Section

The internal voltage reference circuit of the XR-1525A/1527A is based on the well-known "band-gap" reference, with a nominal output voltage of 5.1 volts, internally trimmed to ±1% accuracy. It is short circuit protected and is capable of providing up to 20 mA of reference current. A simplified circuit schematic is shown in Figure 7.

Oscillator Section

The sawtooth oscillator derives its frequency from an external timing resistor/capacitor pair. The timing resistor, R_T, determines the charging current into the timing capacitor, C_T. The magnitude of this current is approximately given by:

$$\frac{V_{ref} - 2V_{BE}}{R_T} \approx \frac{3.7V}{R_T}$$

where R_T may range from 2 kΩ to 150 kΩ. In general, temperature stability is maximized with lower values of R_T. The current source charging C_T creates a linear ramp voltage which is compared to fixed thresholds within. When the capacitor voltage reaches +3.3 volts, the oscillator output (Pin 4) goes high, turning ON the discharge transistor. The capacitor is discharged through the deadtime resistor, R_D. When the voltage on C_T falls to +1.0 volt, the oscillator output goes low, the discharge transistor is turned OFF, and the capacitor is charged through the constant current source as another cycle starts. With large values of R_D (500Ω, maximum), deadtime is increased. The actual operating frequency is thus a function of the charge and discharge times. Figure 2 shows how charge time is related to R_T and C_T, with R_D = 0Ω. Deadtime is a function of R_D and C_T, and can vary between 0.5 to 7 μsec, with R_D = 0Ω, as shown in Figure 3. The equivalent circuit schematic of the oscillator section is shown in Figure 8.

A unit can be synchronized to an external source by selecting its free-running oscillator period to be 10% longer than the period of the external source. A positive-going pulse of at least 300 nsec wide should be applied to the sync terminal for reliable triggering; however, it should not exceed the free-running pulse width by more than 200 nsec. The amplifier of the pulse should be kept between 2 and 5 volts. Multiple units can be synchronized to each other by connecting all C_T pins, and oscillator output pins together; R_T pins and discharge pins on slave oscillators must be left open.

Error Amplifier

The error amplifier of the XR-1525A/1527A is a differential input transconductance amplifier. Its common-mode range covers the reference voltage. Its open-loop gain, typically 75 dB, can be reduced by a load resistor on Pin 9. To ensure proper operation, the output load should be limited to 50 kΩ or greater. An equivalent circuit schematic of the error amplifier is shown in Figure 9.

Soft-Start Circuitry

The soft-start function is provided to achieve controlled turn-on of the pulse-width modulator. When power is applied to the device, the external capacitor, $C_{soft-start}$, on Pin 8 is charged by a 50 μA constant current source. The ramp voltage appearing on this capacitor is fed into the pulse-width modulator, which gradually increases its output duty cycle from zero to the prescribed value. When the shutdown terminal is raised to a positive value, an internal transistor turns ON, and discharges the capacitor, C_S, causing the PWM to turn OFF. When the shutdown terminal is open or pulled low, the transistor turns OFF, and C_S begins charging as before. The turn-on time (time required to charge C_S to +2.7 volts) can be approximated as:

$$T_C \text{ (msec)} = 54\ C_S$$

where C_S is in μF.

Output Section

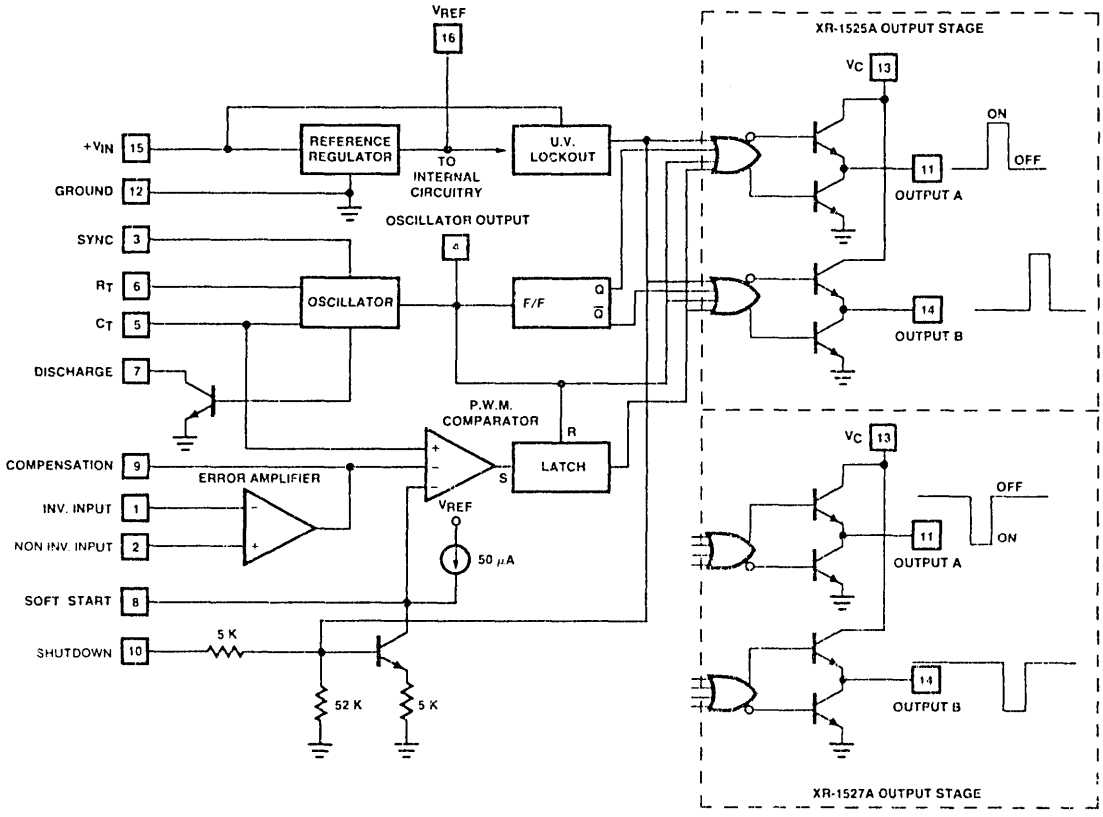
The output drivers of the XR-1525A/1527A are totem-pole designs capable of sinking and sourcing 200 mA. The low source impedance in the high or low states provides ideal interfacing with bipolar as well as FET power transistors. Either push-pull or single-ended output configurations are possible with separate collector supply terminals. The equivalent schematic of the output drivers is shown in Figure 10.

RECOMMENDED OPERATING CONDITIONS

Note 1: Range over which the device is functional and parameter limits are guaranteed.

Collector Supply Voltage (V_C)	+4.5V to +35V
Sink/Source Load Current (Steady State)	0 to 100 mA
Sink/Source Load Current (Peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 kHz
Oscillator Timing Resistor	2 kΩ to 150 kΩ
Oscillator Timing Capacitor	0.001 μF to 0.1 μF
Deadtime Resistor Range	0 to 500Ω

EQUIVALENT SCHEMATIC DIAGRAM



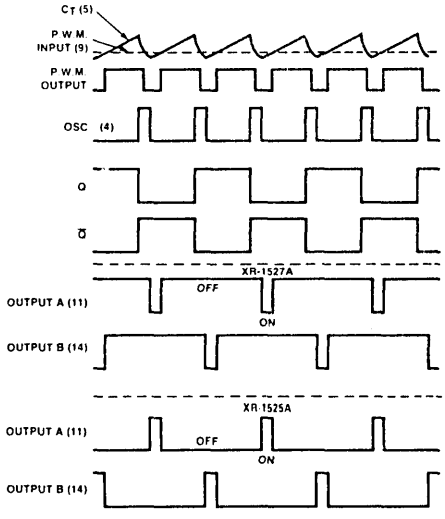


Figure 1: Typical Waveforms—XR-1525A/1527A

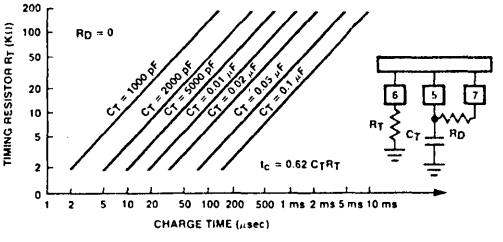


Figure 2. Oscillator Charge Time vs R_T and C_T

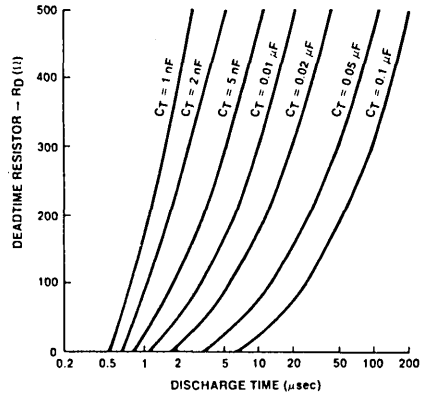


Figure 3. Oscillator Discharge Time vs R_D and C_T

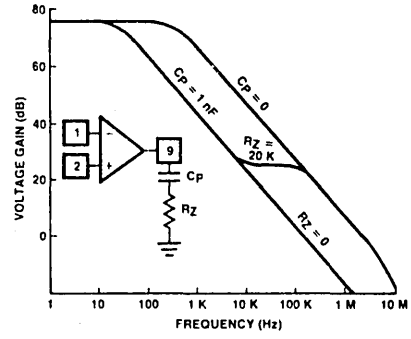


Figure 4. Error Amplifier Open-Loop Frequency Response.

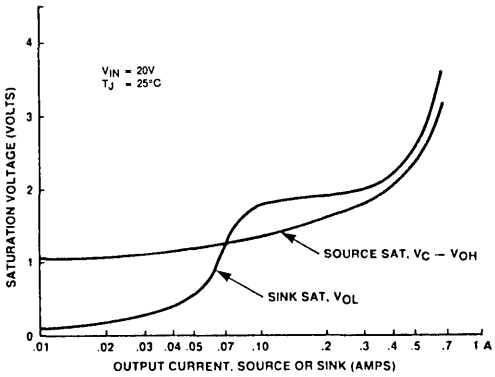


Figure 5. Output Saturation Characteristics

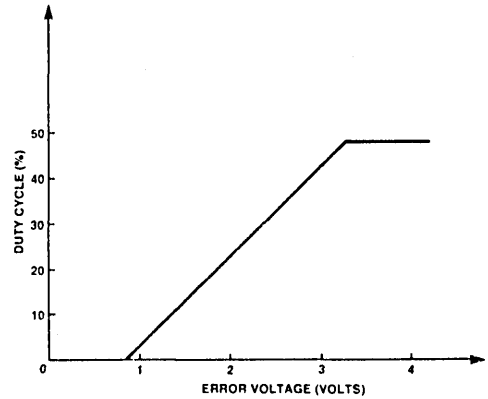


Figure 6. Output Duty Cycle vs Error Voltage

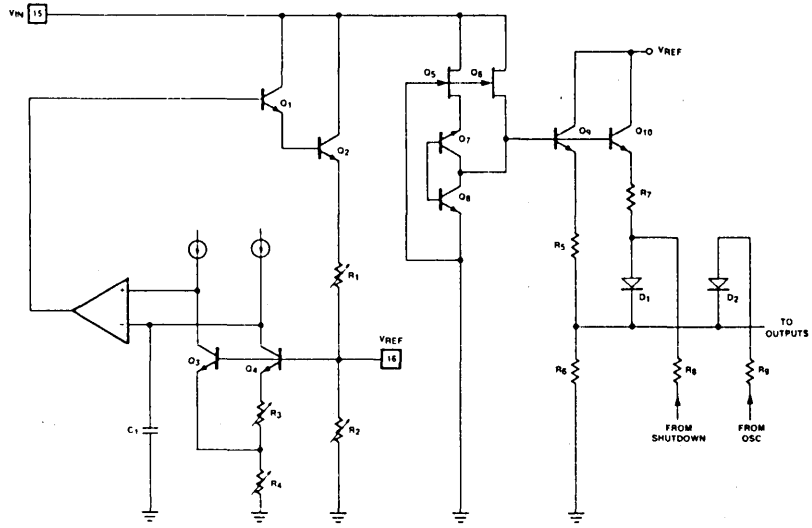


Figure 7. Equivalent Schematic of Voltage Reference Section

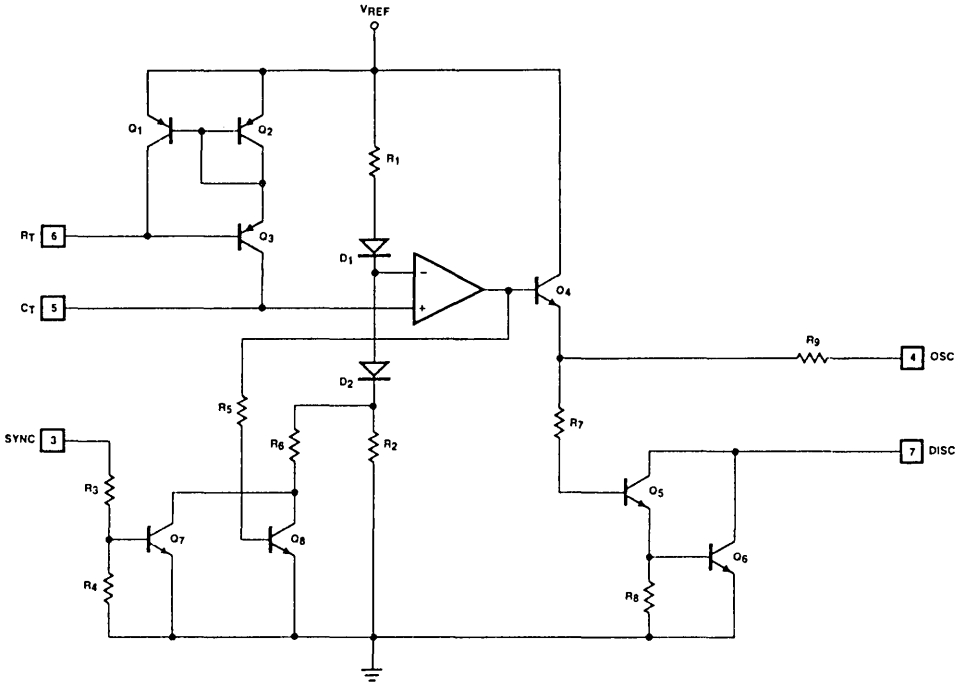


Figure 8. Equivalent Schematic of the Oscillator Section

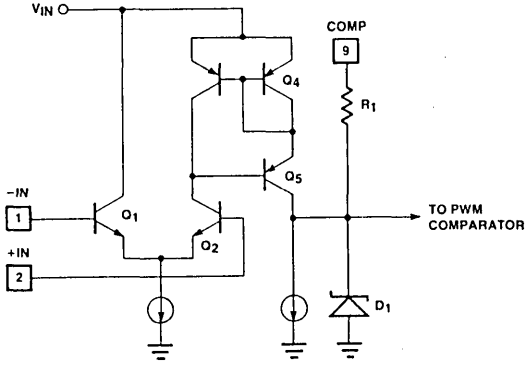


Figure 9. Equivalent Schematic of Error Amplifier Section

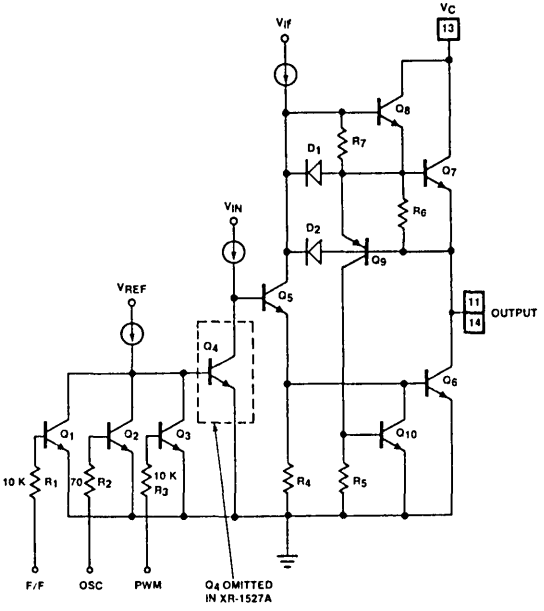


Figure 10. Equivalent Schematic of Output Drivers

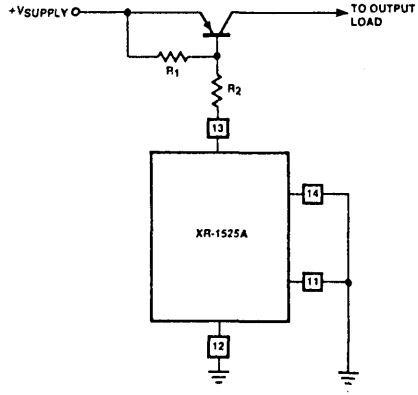


Figure 11. Single-Ended Output for XR-1525A

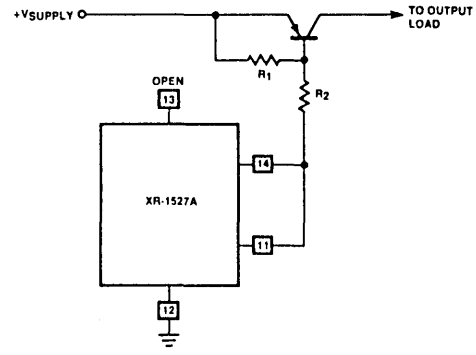


Figure 12. Single-Ended Output for XR-1527A

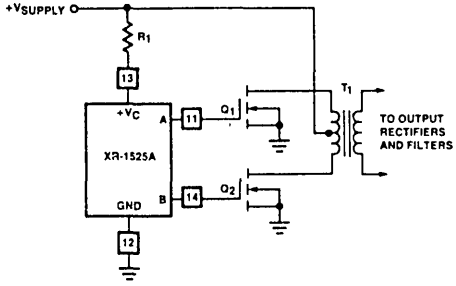


Figure 13. Push-Pull Outputs with XR-1525A

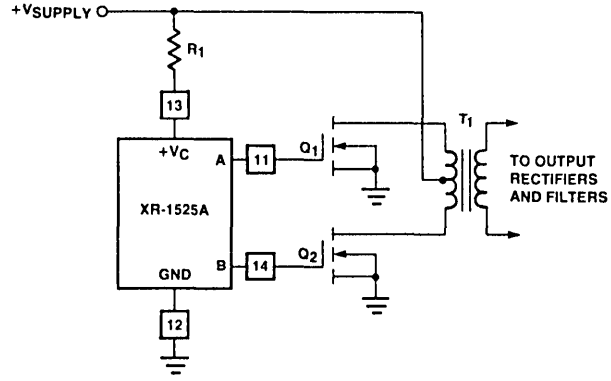


Figure 14. Power FET Push-Pull Outputs with XR-1525A

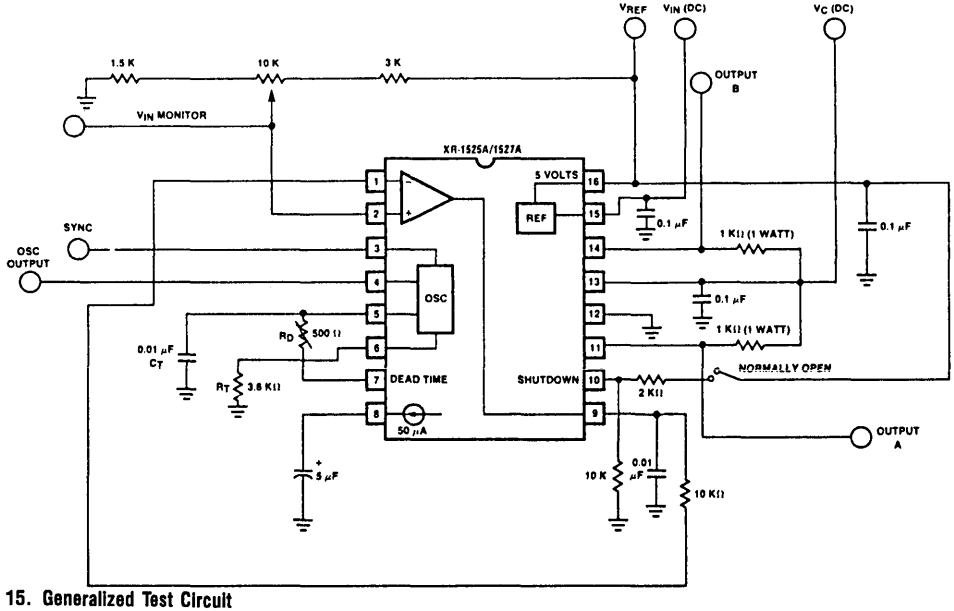


Figure 15. Generalized Test Circuit