FSK Modem Filter

GENERAL DESCRIPTION

The XR-2103 is a Monolithic Switched-Capacitor Filter designed to perform the complete filtering function necessary for a Bell 103 Compatible Modem. The XR-2103 is specifically intended for use with the XR-14412 Modulator/Demodulator to form a complete stand alone two-chip modem. In addition to complete high and low bandpass filters, the XR-2103 contains internal mode switching, auto-zeroing limiter and dedicated duplexer op amp. An on board carrier detect circuit is also included to complete the overall system. Designed for crystal-controlled operation, the XR-2103 operates from a 1.0 MHz crystal or external clock. Buffered clock output is provided for the XR-14412. A self-test circuit is included.

The XR-2103, available in a 20 pin package, utilizes CMOS technology for low power operation with a supply voltage range from 4.75V to 6V.

FEATURES

Single 5 Volt Operation
Complete On Board Output Active Filters
Low Supply Current
Internal Answer/Originate Mode Switching
Programmable Input Receive Gain
Carrier Detect Output
Active Duplexer

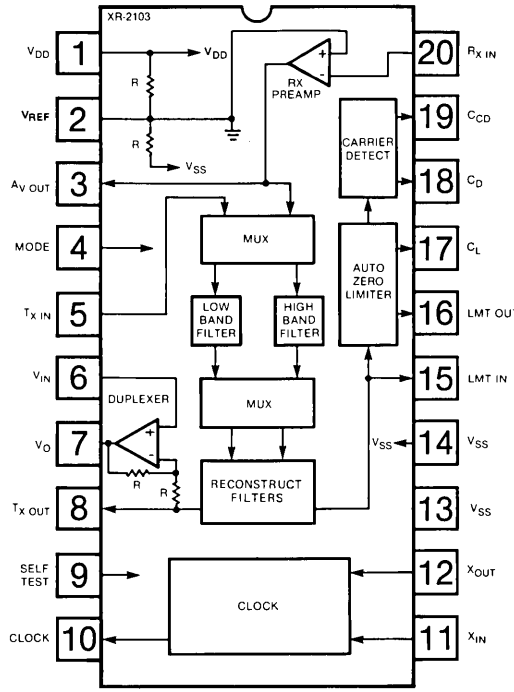
APPLICATIONS

Bell 103 Transmit/Receive Filtering
Complement to XR-14412 or Other
Modulators/Demodulators

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation Plastic Package	650 mW
Derate Above 25°C	5.0 mW/°C
Power Dissipation Ceramic Package	1.0 W
Derate Above 25°C	8.0 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} -0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2103CP	Plastic	0°C to 70°C
XR-2103CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2103 internally consists of four main signal blocks. They are: input and output multiplexers to route the transmit and receive signals to the proper filter and output, according to the mode input; high and low band filters, 6 poles each, to perform precise bandpass filtering; output RC active filters to perform output reconstruction and filtering; carrier detection circuit for system interfacing.

An input amplifier with programmable gain is provided for the receive signals. The XR-2103 contains an internal clock oscillator which accepts either a crystal or an external oscillator of 1 MHz.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5V, V_{SS} = 0V, X_{IN} = 1.0 MHz, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Power Supply Voltage Range	4.75		6	V	V_{SS} = 0
I_{DD}	Power Supply Current		7	10	mA	V_{DD} = 5V
ANALOG SECTION						
RECEIVE AMPLIFIER						
V_{OS}	Offset Voltage	-150		150	mV	
A_{OL}	Open Loop Gain		80		dB	R_L = 100k
I_B	Input Bias Current		1		pA	
SR	Slew Rate		2		V/μs	
	Output Swing	3	4.5		Vp-p	R_L = 100k to GND (Pin 2)
DUPLEXER						
	Isolation		44		dB	R_2 = Line Resistance = 600Ω
	Output Swing	3	4.5		Vp-p	
V_{OS}	Offset Voltage	-150		150	mV	
LIMITER						
	Output Symetery		±1.5	±2.0	%	C_c = 0.1 μf, from 50% Duty Cycle
	Output Swing		4		Vp-p	R_L = 1 meg
	Output Current		100		μA	R_L = 1k
CARRIER DETECT						
V_{th}	Threshold Voltage		-48		dBm	Receive Amplifier Gain =24 dB
	Hysteresis	2	4	6	dB	
t_{on}	Turn On Time		≥100		msec	C_{cd} = 0.1 μf, V_{in} = 48 dBm, Gain = 24 dB
t_{off}	Turn Off Time		≤100		msec	
LOW BAND FILTER						
f_o	Center Frequency	1160	1170	1180	Hz	
BW	Bandwidth		500		Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rej.		15		dB	f = 2 KHz
	Pass Band Ripple			2	dB	p-p 1070 Hz-1270 Hz
	High Band Rejection	40			dB	2025 Hz-2225 Hz
GD	Differential (Group) Delay		200	500	μs	1070 Hz-1270 Hz
	Clock Feedthrough		-60		dBV	62.5 kHz
HIGH BAND FILTER						
f_o	Center Frequency	2105	2125	2145	Hz	
BW	Bandwidth		500		Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rej.		18		dB	f = 1 kHz
	Pass Band Ripple			2	dB	p-p 2025 Hz - 2225 Hz
	Low Band Rejection	40			dB	1070 Hz - 1270 Hz
GD	Differential (Group) Delay		200	500	μs	2025 Hz - 2225 Hz
	Clock Feedthrough		-60		dBV	62.5 kHz
TRANSMIT						
V_{OS}	DC Offset Voltage	-150		+150	mV	
	Output Swing	2.2			Vp-p	R_2 = Line Resistance = 600Ω
	Output Current		1.2		mA	
DIGITAL CMOS LOGIC LEVELS (V_{DD} = 5V, V_{SS} = 0 V)						
V_{ih}	Input Voltage		2.75	3.5	V	'1' Level
V_{il}	Input Voltage	1.5	2.25		V	'0' Level
I_{oh}	Output Current	0.5	1.5		mA	'1' Level CLK OUT
I_{ol}	Output Current	1.0	5.0		mA	'0' Level CLK OUT
I_{oh}	Output Current	0.1	1.5		mA	'1' Level X OUT
I_{ol}	Output Current	0.2	0.9		mA	'0' Level X OUT

OPERATING PRINCIPLES

The XR-2103 contains all the filtering and multiplexing functions necessary for a Bell 103 type (300 baud) FSK modem. A complete modem requires only the XR-2103, the XR-14412, and telephone line interfacing hardware. A description of the main functional blocks follows.

Bandpass Filtering: Two six pole, 500 Hz bandwidth switched capacitor filters, designed for Bell 103 standard center frequencies of 1170 Hz (low band) and 2125 Hz (high band), constitute the main portion of the device. Both filters feature +4 dB passband gain, 50 dB dynamic range, and more than 40 dB opposite band rejection. Filter response curves are depicted in Figure 3. On board multiplexing allows using these filters for both transmitting and receiving. Active low pass filters reconstruct the time sampled output signals, characteristic of switched capacitor filters, and attenuate the unwanted energy above 15 kHz.

Duplexer: An operational amplifier is employed as an active two to four wire converter (duplexer). The two phone wires are "split" into transmit and receive components for proper processing; the transmit output from Pin 8 is applied to the lines through a resistor and the received signal is drawn from the line and routed into a preamplifier. Transmit energy appears as a common mode signal, hence does not appear on the duplexer output. The received signal, meanwhile, is amplified by two. Isolation is maximized when the transmit injection resistor (between Pins 6 and 8) is equal in magnitude to the phone line impedance (600 Ω nominal). Transmit signal levels are typically -9 dBm.

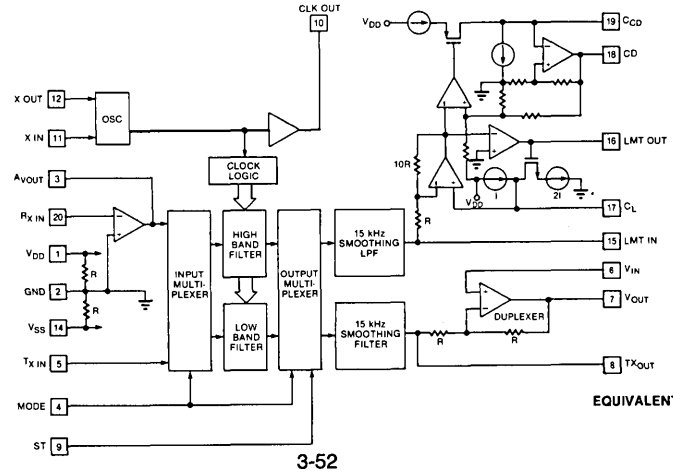
Received Carrier Amplifier: An operational amplifier, with its inverting input on Pin 20 and output on Pin 3, serves as a received carrier amplifier. Duplexer output (Pin 7) is routed to Pin 20 through a 100 kΩ or larger resistor. Gain, typically 5 (14 dB), equals the ratio of the feedback resistor (Pin 3 to Pin 20) to the input resistor (Pin 7 to Pin 20). The non-inverting input is internally biased to one half supply. The amplifier features open loop gain of 80 dB, output swings of 4.5 Vp-p, and a slew rate of 2V/μs. This pin-out allows flexible signal processing capabilities: for example, an input low pass filter for eliminating aliasing is easily achieved.

Auto-Zeroing Limiter: An automatic offset zeroing comparator (limiter) compensates for errors caused by system offset voltages and currents, and converts the received carrier into an accurate 50% duty cycle waveform. The resultant square wave on Pin 16 is at digital logic levels and can interface directly with the modulator/demodulator circuit.

Carrier Detector: An on board carrier detection circuit simplifies total system interfacing. Carrier detect output (Pin 18) pulls low when a suitable signal is received. With 14 dB of gain in the receiver preamplifier, the threshold level is -38 dBM and has 4 dB of hysteresis. Turn on/off delay time is externally programmable by a capacitor from Pin 19 to ground. A 0.1 μF unit yields 100 ms; delay is directly proportional to capacitance.

Clocking: Filter frequency accuracy is directly related to the clock frequency. The device operates within specifications with a 1 MHz clock, provided by either a 1 MHz crystal or by sharing the 1 MHz clock signal from the XR-14412. The device will operate at other clock frequencies, but the filter center frequencies will differ. The crystal and a parallel 10 MΩ resistor are attached between Pins 11 and 12. The crystal should be series resonant with a shunt capacitance less than 9 pF. Pin 10 is the buffered clock output for interconnection with other devices.

Self Test: An on board self test diagnostic activates an analog loop-back mode: the transmit carrier is routed through the proper filter and back through the receive limiter, allowing performance verification of all systems. T_X OUT and R_X IN are disabled when self test is high.



EQUIVALENT SCHEMATIC DIAGRAM

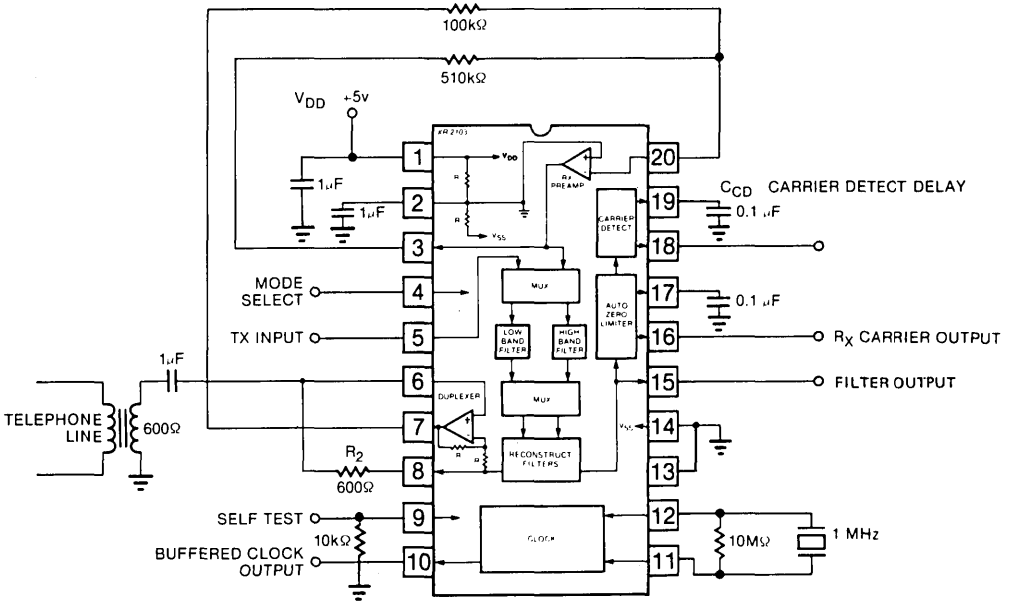


Figure 1. Basic Applications Circuit

Carrier detect threshold is -38dBm in this configuration.

LOGIC INPUT \ STATE	0	1
MODE	ANSWER	ORIGINATE
ST	NORMAL OPERATION	SELF TEST MODE

Figure 2. Control Inputs

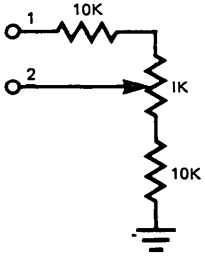


Figure 3. Reference Voltage Trimming for Performance Optimization

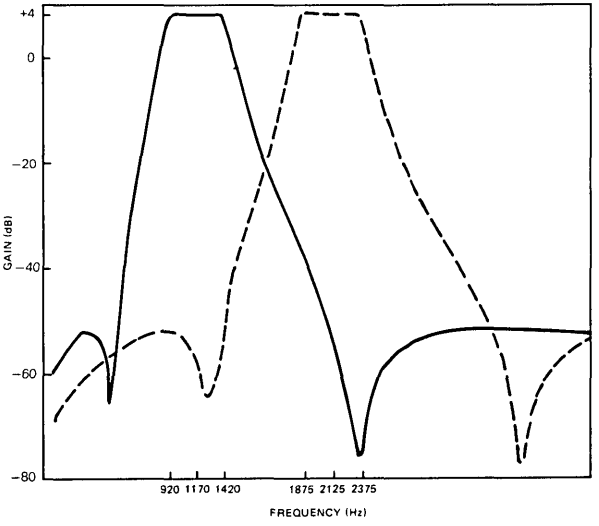


Figure 4. Filter Characteristics

APPLICATIONS

The Bell 103 compatible modem of Figure 5 consists of the XR-2103 FSK modem filter and the XR-14412 FSK modulator/demodulator. Designed for full duplex 300 baud operation, the circuit requires only telephone line and computer interfacing. The entire system uses a single 5V supply, and performs both answer and originate functions. Answer/Originate selection is controlled by the mode input; low inputs select answer, high selects originate.

The telephone line is connected via an isolation transformer to the duplexer input (Pin 6) of the XR-2103. A resistor, equal to the line resistance, attaches from Pin 6 to the transmit output (Pin 8) and couples the transmit signal to the line. The received signal is removed from the line via the duplexer (also called a "two to four wire converter" or "hybrid"). Duplexer output is coupled through the receive carrier preamplifier into the multiplexer, where the proper band pass filter is selected. Transmit energy is seen as a common mode signal and does not appear on the duplexer output.

If the system is in the originate mode (mode pin pulled high), the received signal passes through the high band filter. Then, the sampled signal is reconstructed by an on board RC active low pass filter and is fed into the limiter and carrier detect circuit. Carrier detect output (Pin 18) pulls low after a 100 ms delay, controlled by the 0.1 μF capacitor on the C_{CD} pin (Pin 19). The limiter circuit compensates for circuit imperfections (offset voltages, etc.), and outputs a 50% duty cycle waveform to the demodulator input (Pin 1) of the XR-14412. The demodulated data appears on Pin 7 of the XR-14412.

Transmit data is applied to the modulator input (Pin 11) of the XR-14412. Depending on mode, answer or originate, the data modulates either the high or low band. The modulated signal exits Pin 9 and is applied to the transmit multiplexer input (Pin 5) of the XR-2103; is filtered, reconstructed, and sent into the duplexer and the phone line.

One shared time base is employed: here, the oscillator of the XR-2103 serves both devices. Buffered output is routed from Pin 10 of the XR-2103 into Pin 4 of the XR-14412.

With suitable telephone line coupling and data system interfacing, this modem realizes its goals of high performance and reliability at low cost.

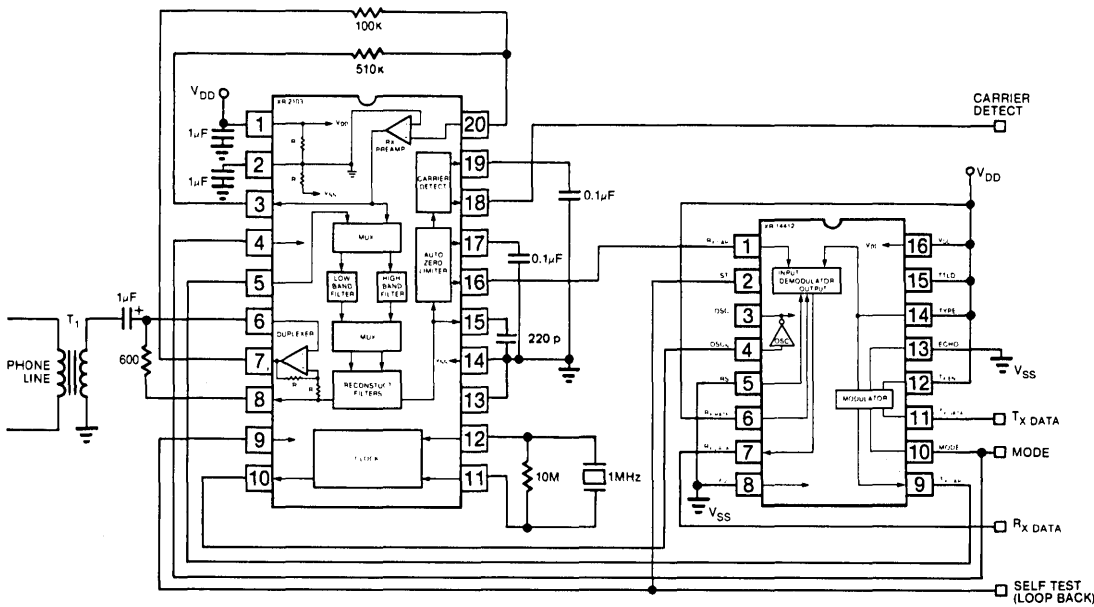


Figure 5. Bell 103 Compatible Modem