PSK Modem Filter

GENERAL DESCRIPTION

The XR-2120 is a self-contained bandpass filter set designed for realization of Bell 212A compatible 1200 bits/sec PSK modems. The XR-2120 utilizes CMOS technology and switched capacitor circuit techniques to minimize external components to a single crystal or frequency source. Contained in the device are two complete bandpass filters centered around the Bell standard 1200 Hz and 2400 Hz send and receive frequencies. These filters also provide compromise line equalization. Additional features included are digitally programmable transmit and receive gains as well as input anti-aliasing and complete output smoothing filters. Separate V_{SS} pins for transmit, receive, and digital sections are provided to minimize crosstalk.

The XR-2120 features guaranteed filter group delay specifications, within ±100μS of nominal. The XR-2120C is a relaxed version of the XR-2120 with group delay specified within ±150μS. The devices are available in a 22 pin (0.4 inch wide) plastic or ceramic package, and operate over a wide range of supply voltages.

FEATURES

On-board Crystal Oscillator With Buffered Output
Internal Anti-aliasing Filters
Complete On-board Output Active Filters
Digitally Programmable Transmit and Receive Gains
MODE Input Internally Switches Filters
for Answer/Originate
Single or Split Supply Operation
Center Frequencies Movable with Input Clock
High-Impedance Inputs (100 kΩ min)
1% Center Frequency Accuracy
Separate CLK IN and CLK OUT Pins

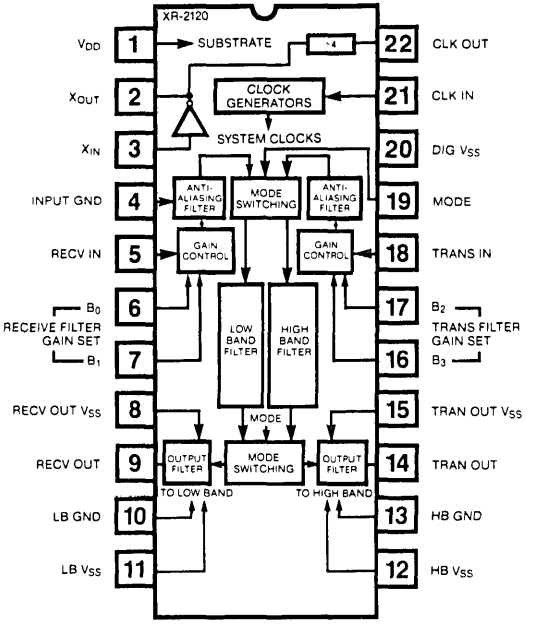
APPLICATIONS

Bell 212A Transmit/Receive Filtering
Answer Back Signal Filtering

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} - 0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2120CN	Ceramic	0°C to +70°C
XR-2120CP	Plastic	0°C to +70°C
XR-2120N	Ceramic	0°C to +70°C
XR-2120P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2120 is comprised of four main signal blocks: The digitally programmable gain amplifier, an input anti-aliasing switched capacitor filter, switched capacitor bandpass filters at 1200 Hz and 2400 Hz, and output RC active filters. These sections serve to: (1) amplify and condition incoming signals, (2) remove noise which can cause aliasing problems in the bandpass filters, (3) provide very precise bandpass filtering and phase compensation, and (4) perform output reconstruction and filtering. To perform these necessary filtering and phase compensation functions, a total of 48 poles are used in the XR-2120.

The programmable gain stages provide 4 selectable gains for transmit or receive. Separate clock output and input pins are provided for flexibility.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V, V_{SS} = −5 V, X_{IN} = 4.032 MHz (CLK IN = 1.008 MHz), T_A = 25°C, unless otherwise specified. Input gain = 0 dB (B1/B3 = B0/B2 = 0).

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL SECTION						
CLK OUT	CLK OUT Drive Capability			50	pF	
I_I	Digital Input Current	−1.0		1.0	μA dc	
V_{IL}	Digital Input Voltage	V_{SS}		V_{SS}+2	V	For "0" Level
V_{IH}		V_{DD}-2		V_{DD}	V	For "1" Level
ANALOG SECTION						
f_{OL}	Filter Center	1190	1200	1210	Hz	Low Band
f_{OH}	Frequencies	2380	2400	2420	Hz	High Band
BW	3 dB Bandwidth	900	950		Hz	Either Band
R_i	Input Impedance	100k			Ohms	
C_i	Input Capacitance			10	pF	
f_{SI}	Anti-Aliasing Filter Sampling Frequency		504		kHz	
f_{SB}	High/Low Band Sampling Frequency		126		kHz	
	Tran/Recv Output Drive Capability	10k		50	Ohms pF	
	Output Clock Feedthrough			2	mV rms	at 126 kHz
e_{o100}	Output Noise		160		μV rms	In Passbands (100 Hz BW)
e_{o1000}	Output Noise		700		μVrms	In Passbands (1kHz BW)
ei_{range}	Dynamic Range of Filters		70		dB	Note 1
Vo_{sw}	Output Voltage Swing	6.0	6.8		V pp	Note 2
2ndHarm	2nd Harmonic Content		-60		dB	f_{IN} = 1200 Hz Referenced to Fundamental
T_{SW}	Mode Switching		10		ms	
I_{DD}	Supply Current		9	27	mA	
V_{SUP}	Supply Voltage Range	±4.75 9.5	±5 10	±7.5 15.0	V V	Dual Supplies V_{DD} Reference to V_{SS}
A_V	Passband Gain					Input Gain = 0 dB
	Low Band	3.2	4.2	5.2	dB	1200 Hz
		−1.4	0	1.4	dB	900 - 1500 Hz (Note 3)
	High Band	2.8	3.8	4.8	dB	2400 Hz
		−1.7	0	1.7	dB	2100 - 2500 Hz (Note 3)
		0	1.2	2.2	dB	2500 - 2800 Hz (Note 3)

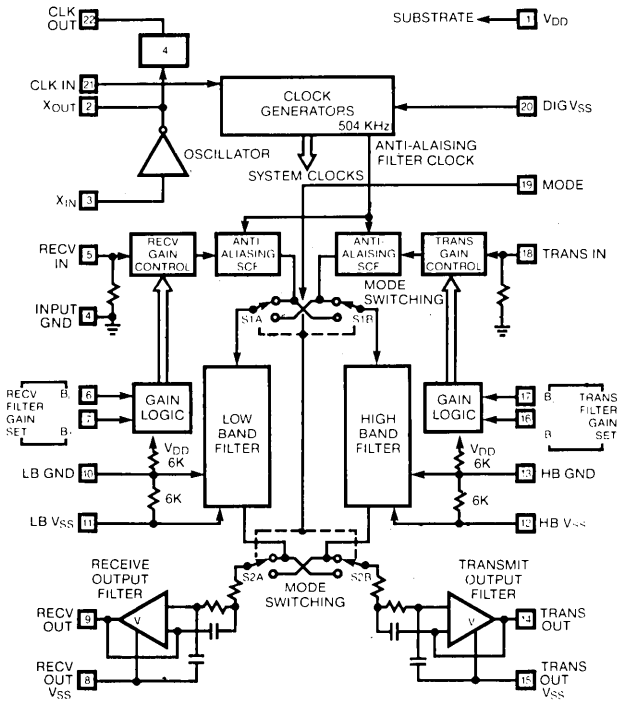
Note 1 Dynamic range is defined as $ei_{range} = 20 \text{ Log } (Vo_{sw}/e_o)$.
Note 2 Vo_{sw} is the maximum output swing before output clipping occurs.
Note 3 Gain measurements are relative to passband center frequency gain normalized to 0 dB.

ELECTRICAL CHARACTERISTICS Continued

FILTER RESPONSE

SYMBOL	PARAMETER	XR-2120			XR-2120C			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
GD	Group Delay Low Band Filter	5060	5160	5260	5010	5160	5310	μs	900 Hz (See Figure 7)
		5100	5200	5300	5050	5200	5350	μs	1kHz
		5160	5260	5360	5110	5260	5410	μs	1.1kHz
		5200	5300	5400	5150	5300	5450	μs	1.2kHz
		5215	5315	5415	5165	5315	5465	μs	1.3kHz
		5255	5355	5455	5205	5355	5505	μs	1.4kHz
		5260	5360	5460	5210	5360	5510	μs	1.5kHz
	High Band Filter	5270	5370	5470	5220	5370	5520	μs	2.1kHz (See Figure 8)
		5040	5140	5240	4990	5140	5290	μs	2.2kHz
		5140	5240	5340	5090	5240	5390	μs	2.3kHz
		5015	5115	5215	4965	5115	5265	μs	2.4kHz
		5000	5100	5200	4950	5100	5250	μs	2.5kHz
		4920	5020	5120	4870	5020	5170	μs	2.6kHz
		4800	4900	5000	4750	4900	5050	μs	2.7kHz

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-2120 in a split supply configuration. In this mode, Pins 4, 10, and 13, are simply tied to ground. For single supply operation, Pins 10 and 13 internally bias to half supply and should be externally bypassed with 2.2 μF capacitors. Pin 4 does not internally dc bias, however, Pin 10 or 13 can provide it with a half supply bias point. In this connection, a 10 kΩ resistor should be used between Pin 4, and Pin 10 or 13, with Pin 4 bypassed with a 2.2 μF capacitor.

Signal flow is illustrated as shown in Figure 2. The transmit or receive signal will follow a path through four internal blocks. First it passes through a digitally programmable gain stage. The gain, as a function of a 2-Bit digital input, is shown in Figure 3. Next, the signal passes through a two-pole anti-aliasing low-pass filter at 12 kHz. This is used to remove noise around the main filter switching frequency of 126 kHz. The anti-aliasing filter is also a sampled-data filter, but is switched at a much higher rate of 504 kHz. It is necessary, therefore, to ensure that wideband noise above 252 kHz is not present at the inputs. In noisy environments a single noise pole RC filter at 30 kHz is usually sufficient for filtering input noise. The third signal block is the main bandpass filtering section at 1200 Hz or 2400 Hz, depending on the mode selected. The last section is the output smoothing filter; a two-pole RC active filter used to reconstruct the signal from its sampled data form.

The mode input pin is used to direct the transmit and receive signals to the appropriate filter section. Figure 4 shows mode selection logic convention.

The XR-2120 is designed to be operated with a 4.032 MHz crystal between the X_{IN} and X_{OUT} pins. The 4.032 MHz is divided by four and output on the CLK OUT pin, Pin 22. For normal operation, the CLK OUT is tied to the CLK IN pin, Pin 21; however, the bandpass center frequencies can be decreased by providing a divider between these two pins. An external CLK can be used by inputing a 1.008 MHz clock into the CLK IN pin, or a 4.032 MHz clock into the X_{IN} pin.

Figure 5 shows circuitry suitable for translating TTL signals to the CMOS levels required by all XR-2120 digital inputs. The amplitude and group delay characteristics of the XR-2120 are shown in Figures 6 through 8.

The XR-2120 may also be used in CCITT V.22 applications by adding guard tone notch filters as shown in Figure 9 or 10. This type of filter, when used with the XR-2120, will produce at least 60 dB of attenuation to either 550 Hz or 1800 Hz signals.

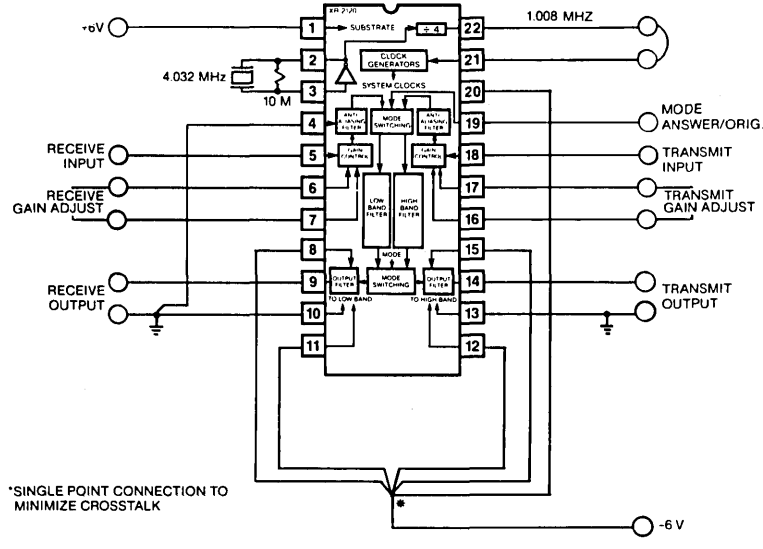


Figure 1: Typical Split Supply Connection.

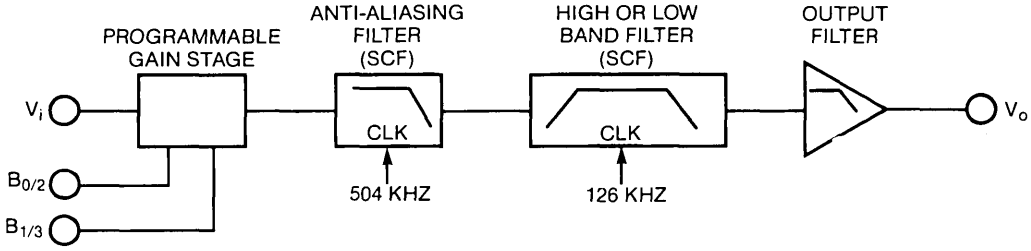


Figure 2: Signal Path

B1 / B3	B0 / B2	INPUT GAIN (dB)	
0	0	0	
0	1	6	
1	0	10	1 = Logic High
1	1	14	0 = Logic Low

Figure 3: Gain Programming (Nominal Gain Shown in Fig. 6)

MODE PIN	TRANSMIT	RECEIVE	TERMINOLOGY
1	Low Band	High Band	Originate
0	High Band	Low Band	Answer

Figure 4: Mode Selection Logic

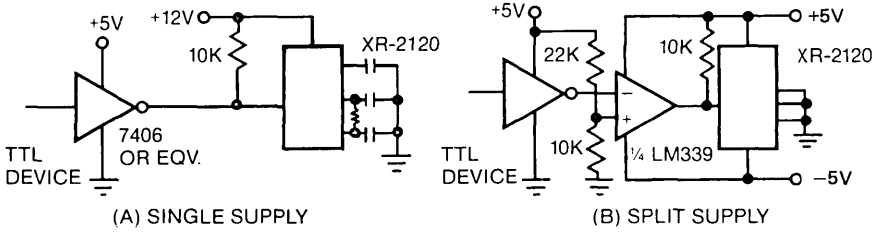


Figure 5: **TTL Interfacing of Digital Inputs.**

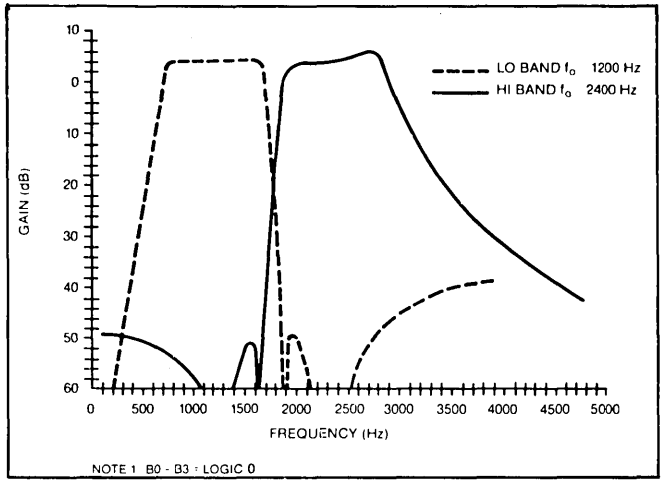


Figure 6: High and Low Band Amplitude Response.

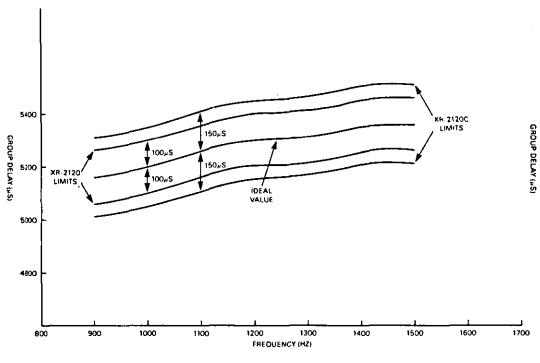


Figure 7: Low Band Group Delay Characteristics

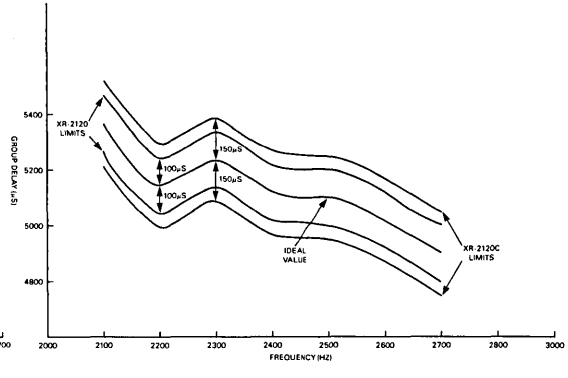


Figure 8: High Band Group Delay Characteristics

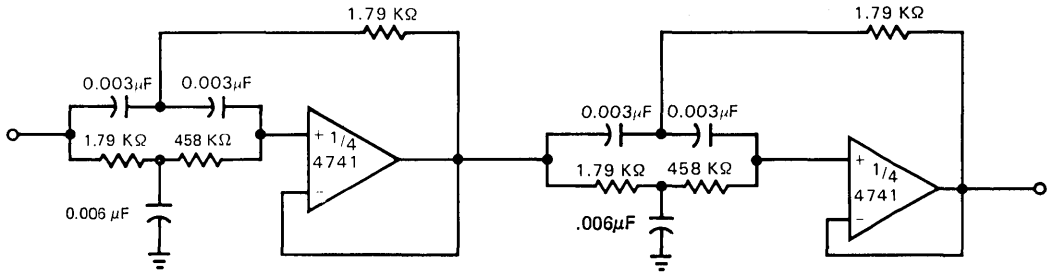


Figure 9. V.22 1800 Hz Notch Filter

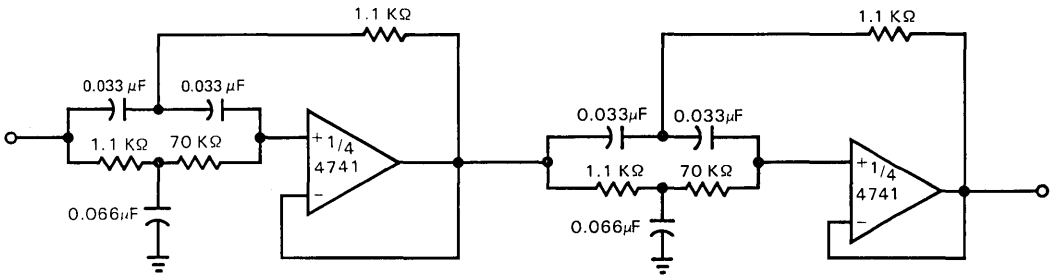


Figure 10. V.22 550 Hz Notch Filter