Bell 212A Type Modulator

GENERAL DESCRIPTION

The XR-2121 is designed to provide the complete modulator function for a Bell 212A type modem. The circuit accepts a synchronous serial data stream and generates either a 300 BPS frequency shift keyed (FSK) or a 1200 BPS differential phase shift keyed (DPSK) carrier signal. An on-board digital-to-analog converter provides a synthesized sine wave output. Also provided on the transmitted carrier output is an inverting amplifier with external feedback resistor to provide a carrier amplitude adjust.

The XR-2121 contains an internal 17 bit scrambler. This scrambler which is used during DPSK operation has a disable input for sending non-scrambled carriers.

A 1200 Hz transmit clock output is provided for 1200 BPS operation, although the XR-2121 will also accept an external transmit clock. For test or other purposes, a 600 Hz baud clock output is also supplied.

The XR-2121 is constructed using silicon gate CMOS technology. The main clock frequency input is 1.8432 MHz. The XR-2121, available in a 22 Pin (0.4 inch wide) package, is designed to operate from +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK
300 BPS FSK
Digital Modulation Techniques for DPSK
External Transmit Clock Input
600 Hz Dibit Clock Output
Complete Scrambler Function with Disable Input
Transmit Carrier Level Adjust
1.8432 MHz Clock
±5 Volt Operation

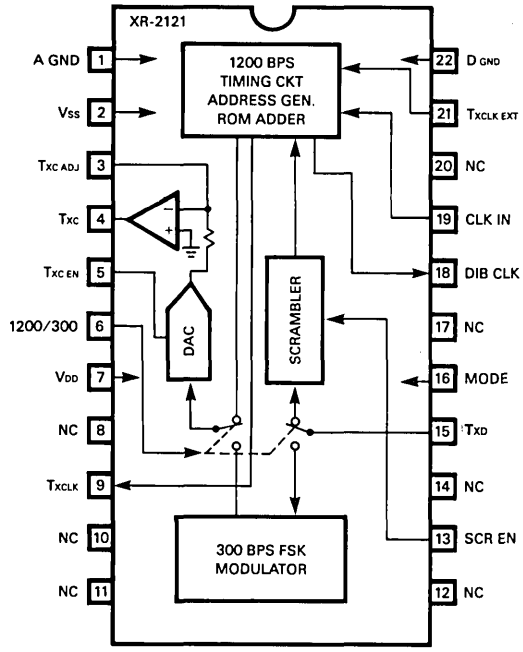
APPLICATIONS

Bell 212A Type Modulator
Bell 103 Type Modulator

ABSOLUTE MAXIMUM RATINGS

Power Supply	
V_{DD}	-0.3 to +7V
V_{SS}	+0.3 to -7V
Input Voltage	V_{SS} -0.3V to V_{DD} +0.3V
DC Input Current	±10 mA
Power Dissipation	1.0 W
Derate Above 25°C	5 mW/°C
Storage Temperature Range	-65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2121CN	Ceramic	0°C to 70°C
XR-2121CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2121 basically has two types of operation, 1200 BPS DPSK or 300 BPS FSK. For 1200 DPSK the XR-2121 generates carrier frequencies of 1200 Hz or 2400 Hz, depending on mode selection (originate or answer). The carrier frequencies are imposed with phase shifts to carry the data to be transmitted (T_{XD}) over the telephone network. The phase shifts correspond to the incoming data grouped in pairs (dibits) and are one of four values — 0°, 90°, −90°, 180°.

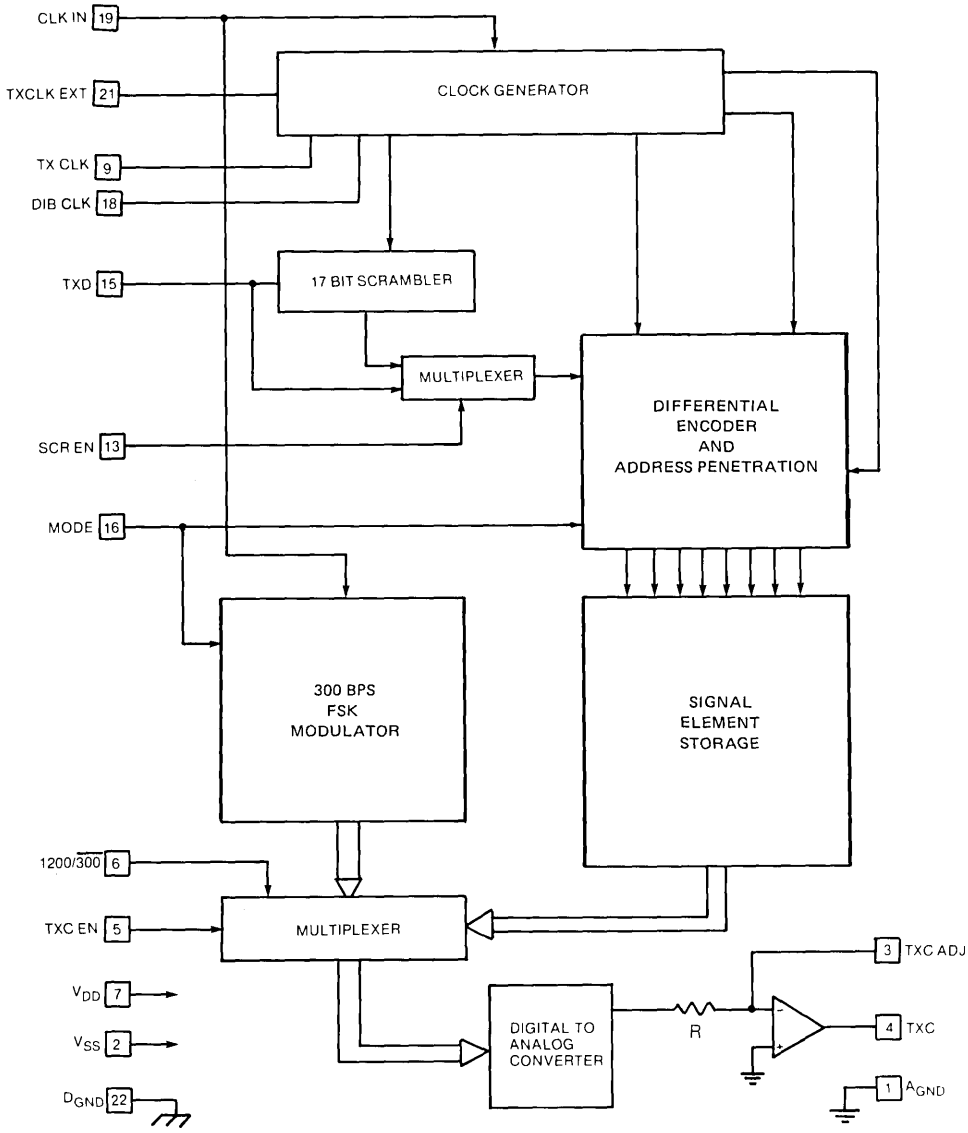
During 300 BPS FSK operation, the XR-2121 generates one of two pairs of frequencies to represent the T_{XD}. These pairs are either 1070 Hz/1270 Hz or 2025 Hz/2225 Hz depending on mode selection.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ±5%, V_{SS} = -5 V ±5%, CLK IN = 1.8432 MHz ±0.01%, T_A = 0°-70°C unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{DD}	Positive Supply Current		2.5	4	mA	
I_{SS}	Negative Supply Current		-1.5	-2.5	mA	
DIGITAL INPUTS/OUTPUTS						
V_{OH}	Output High Voltage	2.4			V	I_O = 1 mA
V_{OL}	Output Low Voltage		0.4	0.8	V	I_O = -1.5 mA
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{OH}	Output Drive Current	0.5	1.5		mA	V_{OH} = 3.5 V
I_{OL}	Output Drive Current	2.0	4.0		mA	V_{OL} = 0.5 V
I_{IN}	Input Current			10	μA	
ANALOG SECTION						
V_{TXC}	Transmit Carrier Amplitude		-4		dBM	R_{EXT} = 10k
V_{TXC2H}	Transmit Carrier Amplitude 2nd Harmonic Content		-40		dB	$R_L \geq$ 10k

3



EQUIVALENT SCHEMATIC DIAGRAM

PRINCIPLES OF OPERATION

The XR-2121 is designed to perform all the necessary functions for the modulator section of a Bell 212A type modem. It has been specifically designed to operate with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer to form the complete Bell 212A type modem signal processor. This data sheet will cover just the XR-2121 and its functions with Application Note AN-28 covering the complete system.

The XR-2121 has two basic types of operation; that of a 1200 BPS differential phase shift keyed (DPSK) or 300 BPS frequency shift keyed (FSK) modulator.

The 1200 BPS section of the XR-2121 converts a serial synchronous data stream (T_{XD}) into a DPSK encoded carrier suited for transmission over a standard telephone switched network. The incoming data, T_{XD}, is clocked into the XR-2121 by either an internally generated transmit clock, T_X CLK, or an externally applied clock, T_X CLK EXT. The internal T_X CLK is derived from the main 1.8432 MHz clock, and is precisely 1200 Hz. If an external transmit clock is applied to the T_X CLK EXT input, T_X CLK will become phase locked to T_X CLK EXT. Figure 1 shows the relationship between T_{XD} and T_X CLK (1A) and T_X CLK and T_X CLK EXT (1B).

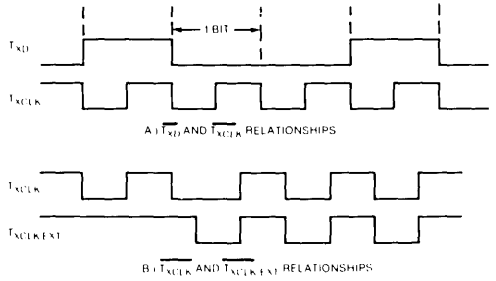


Figure 1. Transmit Data & Clock Relationships

As seen in Figure 1, data is clocked into the XR-2121 on the falling edge of T_X CLK.

1200 BPS data entering the XR-2121 is passed through a scrambler circuit, as shown in Figure 2.

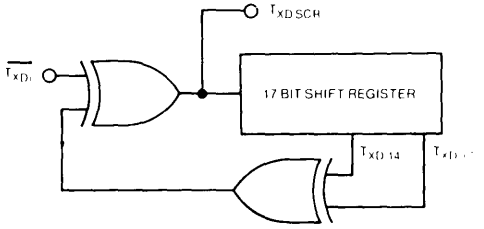


Figure 2. 17 Bit Psuedo Random Scrambler

The output of the scrambler produces a psuedo-random output which can be described by the following equation:

$$T_{XD\,SCR} = T_{XDI} \oplus T_{XD-14} \oplus T_{XD-17}$$

$\oplus$ = exclusive – or operation

The main purpose of the scrambler is to assure that the transmitted carrier will not have extended periods of 0° phase shifts. This condition would cause the receiving modem's demodulator to loose lock and be unable to extract clock information from the received carrier. This condition is discussed further within the XR-2122 data sheet.

The scrambled data is fed into the actual modulator section of the XR-2121. This section phase encodes a constant frequency carrier to represent the incoming serial data, T_{XD}.* This type of phase encoding phase shift the carrier every two data bits. Figure 3 shows the relationship between the transmitted data, its clock, and the resultant phase encoded carrier. As seen in this figure, although the data rate is 1200 BPS, the baud rate is only 600. This is because phase changes only occur every two data bits or dibits. Table 1 gives the phase changes for the four possible dibit values.

*The transmit carrier frequencies for 1200 BPS operation are either 1200 Hz for originate mode or 2400 Hz for answer mode.

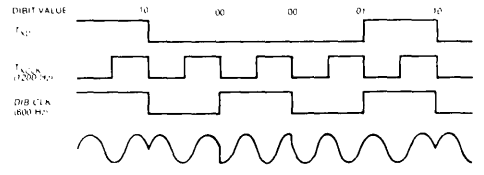


Figure 3. $\overline{T_X\ CLK}/\overline{T_{XC}}$ Timing

DIBIT	PHASE CHANGE
0 0	+90°
0 1	0°
1 0	180°
1 1	−90°

Table 1. Carrier Phase Change vs Dibit Value

It should be noted that the phase changes are relative values. That is, each phase change as shown in Table 1 is relative to the previous carrier phase.

Figure 3 shows the T_{XC} being phase shifted, however, the XR-2121 does not introduce abrupt changes as shown there. This figure was drawn in this fashion for clarity. The XR-2121 uses digital echo modulation techniques. This technique allows incremental or slowly changing phase changes. Using this method also allows precise shaping of the frequency spectrum. The spectrum analyzer photograph in Figure 4 shows the carrier spectrum for each carrier frequency. It can be seen from the photo that separation of about 40 dB between the two spectrums is possible even before bandpass filtering. The frequency spectrums are designed for square root raised cosine shaping.

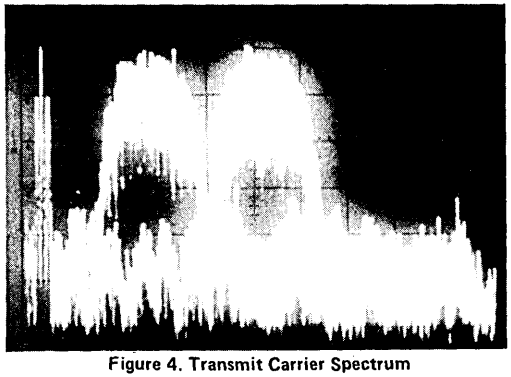


Figure 4. Transmit Carrier Spectrum

For 300 BPS operation frequency shift keying, FSK, encoding techniques are used. For this operation bit asynchronous serial data is fed into the XR-2121 data input. Being asynchronous, no transmit clock is used. The scrambler is bypassed for 300 BPS operation.

FSK encoding uses pairs of frequencies to represent input data changes. Figure 4 shows the incoming data, T_{XD}, and carrier output relationships.

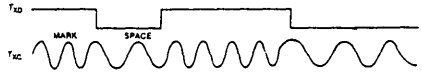


Figure 5. FSK Data Carrier Relationships

The pairs of frequencies used for the two different modes are shown in Table 2. The higher frequency in each pair is known as the mark frequency with lower the space.

MODE	CARRIER FREQUENCIES (MARK/SPACE)
Answer	2225 Hz/2025 Hz
Originate	1270 Hz/1070 Hz

Table 2. FSK Carrier Frequencies

Unlike 1200 BPS operation, for 300 BPS, the baud rate is the same as the data rate, 300. This is of course because every input data change causes a carrier frequency shift.

The outputs of both 1200 BPS and 300 BPS sections are fed into a multiplexer which routes the proper one to the output section depending on speed selection. The output circuitry consists of a seven bit digital-to-analog converter (DAC) and an output operational amplifier. The op amp is configured as an inverting amplifier with the DAC feeding an input resistor and the feedback resistor placed externally. This allows T_{XC} amplitude adjustment at this point. Pin 5, T_{XC} EN, can be used to disable transmission if desired.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	AGND	This is analog or signal ground. It should not carry logic or heavy currents.
2	V_{SS}	Power input for the negative power supply which is typically -5.0 volts.
3	TXCADJ	This is the inverting input of the output op amp. A resistor (R_{EXT}) from this pin to pin 4 (T_{XC}) sets the output amplitude of the T_{XC} (see Figure 6).
4	T_{XC}	This is the transmit carrier output.
6	1200/$\overline{300}$	Speed select input to set either 1200 BPS DPSK or 300 BPS FSK operation.
7	V_{DD}	Power input for the positive power supply which is typically +5.0 volts.
9	TXCLK	The transmit clock is output on this pin. It is internally generated from the main clock input (pin 19) and is used internally to clock T_{XD} into the XR-2121.

13	SCR EN	The data scrambler can be enabled or disabled by this pin during 1200 BPS operation.
15	$\overline{TXD}$	This is the serial data input.
16	MODE	Answer or originate modes are selected by this pin.
18	DIB CLK	The 600 Hz dibit clock is output on this pin. It may be used during system testing such as digital loopback to provide an alternating 1010... data pattern.
19	CLK IN	This is the main clock input and should be 1.8432 MHz ±0.01%.
21	$\overline{TXCLK\ EXT}$	An external transmit clock may be applied to this input during 1200 BPS operation ∓0.01%.
22	DGND	This is the ground for the logic circuitry of the XR-2121.

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2121.

PIN	NAME	FUNCTION LOGIC HIGH	LOGIC LOW
5	TXC EN	Carrier Enabled	Carrier Disabled
6	1200/$\overline{300}$	1200 BPS Operation	300 BPS Operation
13	SCR EN	Scrambler Enabled	Scrambler Disabled
16	MODE	Answer	Originate

Table 3. Control Input Conditions

APPLICATIONS

A typical connection of the XR-2121 is shown in Figure 6.

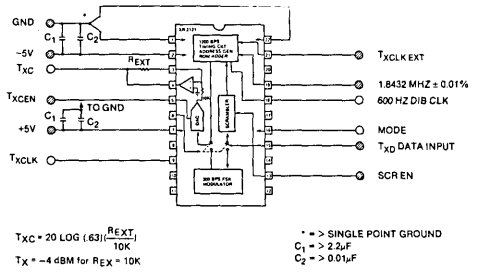


Figure 6. XR-2121 Typical Connection

The synchronous data stream is fed into T_{XD} with the T_{XC} output being either a DPSK or FSK encoded carrier. In a complete system the T_{XC} would go to the transmit filter input. Application Note AN-28 shows the XR-2121 in a complete modem signal processor.

Several output waveforms have been included to help understand the XR-2121 operation. Figure 6 shows frequency spectrums for FSK for both answer and originate modes. It can be seen to consist of two 300 Hz wide spectrums centered around 1170 Hz and 2125 Hz. Figure 7 and 8 show the higher harmonic contents of the FSK spectrums. These figures show the second harmonic content to be more than 50 dB down from the fundamental. This is very desirable in the originate mode as second harmonics not attenuated by the transmit filter will pass unattenuated through the receive and cause degraded performance.

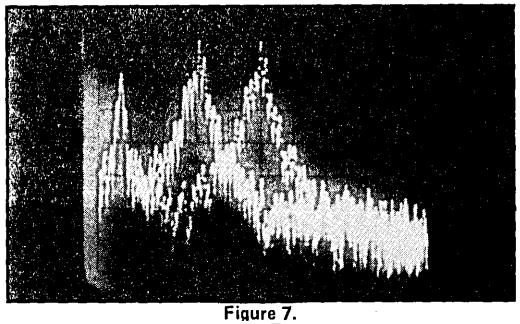


Figure 7.

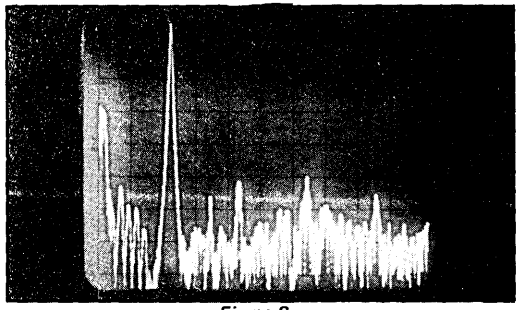


Figure 8.

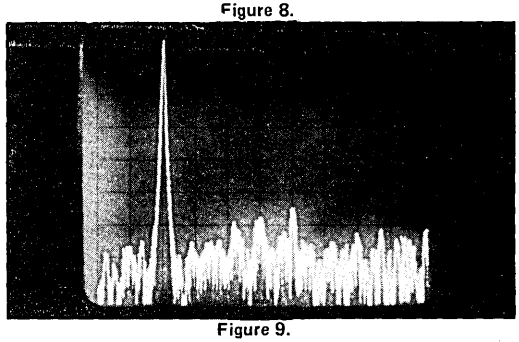


Figure 9.

Figure 9 and 10 show the carrier being enabled and disabled using the $T_{XC\ EN}$ pin (pin 5) for PSK and FSK respectively. It shows about 10 ms necessary for the carrier to be either fully enabled and settled, or disabled. These photos were taken with a transmit filter similar to the XR-2120 at the output of the XR-2121 to produce a clearer picture.

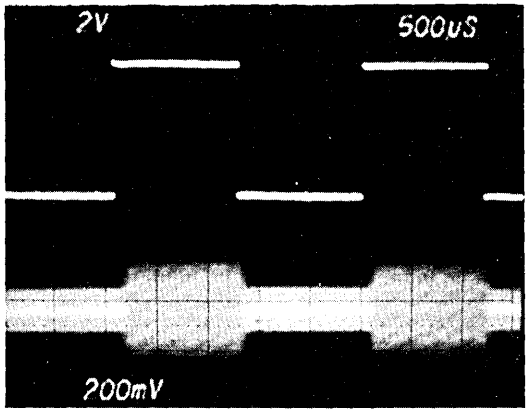


Figure 10.

For further application information on the XR-2121, Application Note AN-28 shows a complete modem signal processor utilizing the XR-2121 with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer.

Bell 212A Handshake

The Bell 212A modem specifications require auto speed selection on auto answer modems. Auto speed selection requires detection and decoding of the Bell 212A handshake protocol. This detection and decoding is automatically performed by the XR-2122, Bell 212A type demodulator. Some additional logic / circuitry is required to perform the handshake properly. This logic / circuitry may be digital, analog, or microprocessor-based.

Figure 12A and 12B illustrates the timing requirements for the Bell 212A handshake.

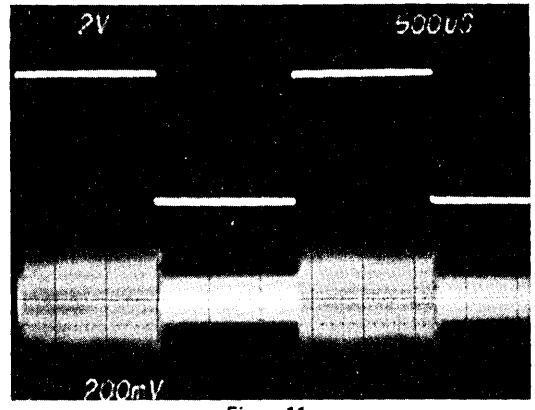
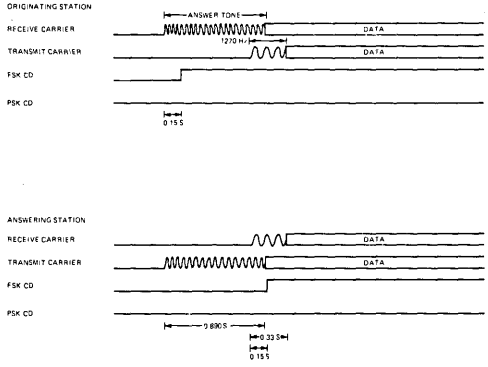


Figure 11.



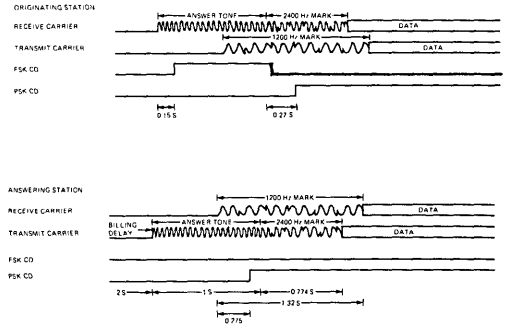


Figure 12A. Figure 12B. V.22 Handshake (with V.25 Auto Answer)

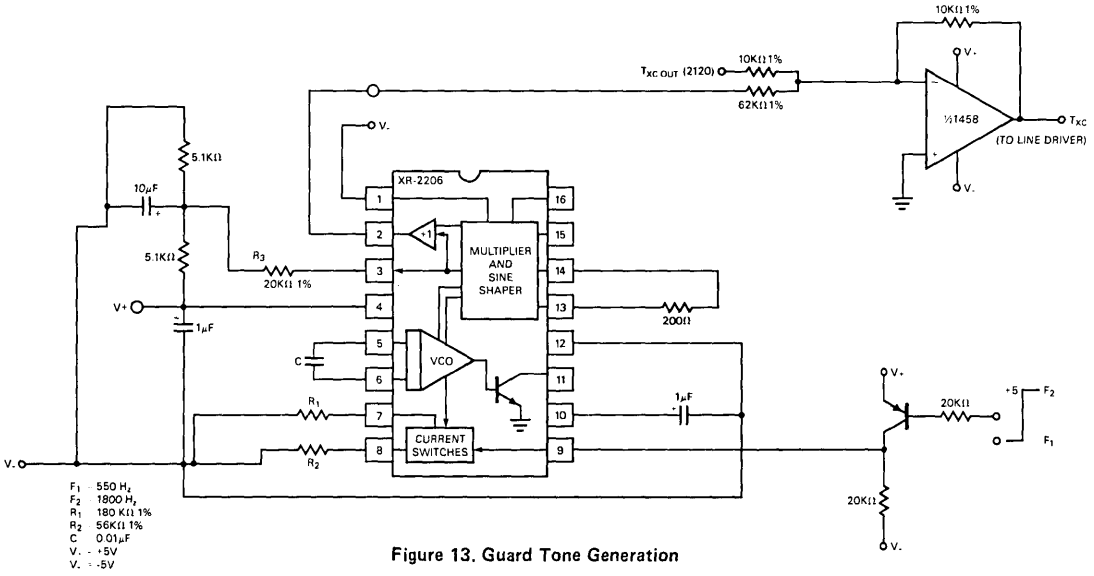


Figure 13. Guard Tone Generation

V.22 Guard Tone Generation

Figure 13 illustrates implementation of the V.22 guard tone generation. V.22 specifies use of the 1800 Hz guard tone in conjunction with the Originate carrier. The 550 Hz guard tone is a national option. Specifications for guard tone generation require the amplitude of the guard tone to be 6 ±1 dBM lower than the transmitted carrier which is typically 9 dBM. The circuit of Figure 13 allows choice of implementation of either guard tone via TTL logic levels: 5 V giving 1800 Hz and 0 V producing 550 Hz. The 20 kΩ resistor to pin 3 sets the voltage at pin 2 to 1.2 V peak. This voltage is then summed and attenuated at the line driver (XR-1458) to give the -16 dBM output required.

Transmit Output Amplifier

To ensure transmit amplitude accuracy for the XR-2121, an external amplifier is recommended. The input to this amplifier should be from pin 3, $T_{XC\ ADJ}$. Figure 14 shows a typical implementation of this transmit amplifier.

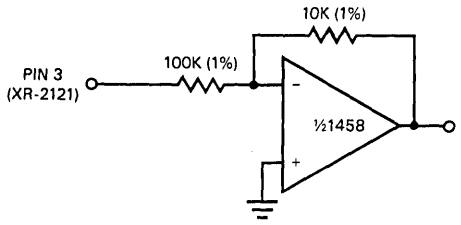


Figure 14. Transmit Carrier Output Amplifier