Bell 212A Type Demodulator

GENERAL DESCRIPTION

The XR-2122 is designed to perform the complete Bell 212A type modem demodulator function. Both 1200 BPS differential phase shift keyed (DPSK) and 300 BPS frequency shift keyed carrier demodulation is performed by the XR-2122. The 1200 BPS portion utilizes coherent demodulation, while the 300 BPS uses phase-locked loop techniques. For 1200 BPS operation, an internal 17 bit descrambler provides the descrambled output with the non-descrambled output also available.

Automatic speed selection is performed by a handshake circuit. Carrier detect outputs are supplied for FSK data, PSK data, and conventional energy detection.

A non-committed operational amplifier is supplied to provide receive carrier sensitivity tailoring. An automatic gain control circuit (AGC) assures wide dynamic input carrier range.

The XR-2122 is constructed using silicon gate CMOS technology. The XR-2122 is designed to operate off of a 1.8432 MHz clock input. Available in a 28 Pin package, the XR-2122 is designed for +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK Coherent Demodulation
300 BPS FSK Demodulation
Eye Diagram Output
Internal 17 Bit Descrambler
Non-descrambled Demodulation Output Available
FSK, PSK and Energy-type Carrier Detect Outputs
Automatic Speed Selection
Non-committed Op Amp for Input AGC Amplifier
AGC Input Circuit for Wide Dynamic Range

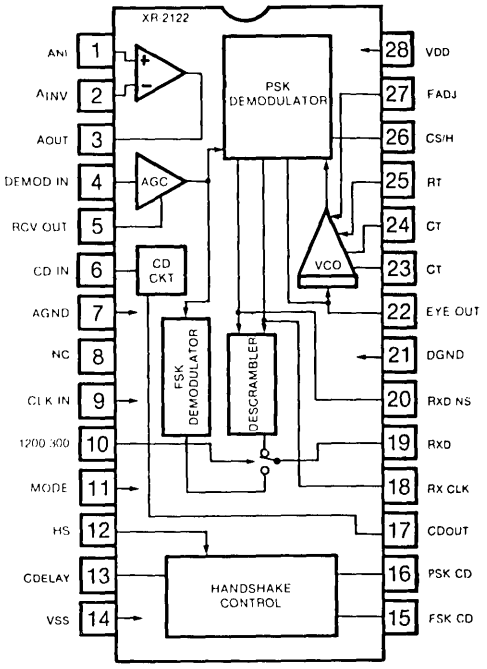
APPLICATIONS

Bell 212A Type Demodulator
Bell 103 Type Demodulator

ABSOLUTE MAXIMUM RATINGS

Power Supply	
V_{DD}	-0.3 to 7 V
V_{SS}	0.3 to -7 V
Input Voltage	V_{SS} -0.3V to V_{DD} +0.3V
DC Input Voltage	±10 mA
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2122CN	Ceramic	0°C to 70°C
XR-2122CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

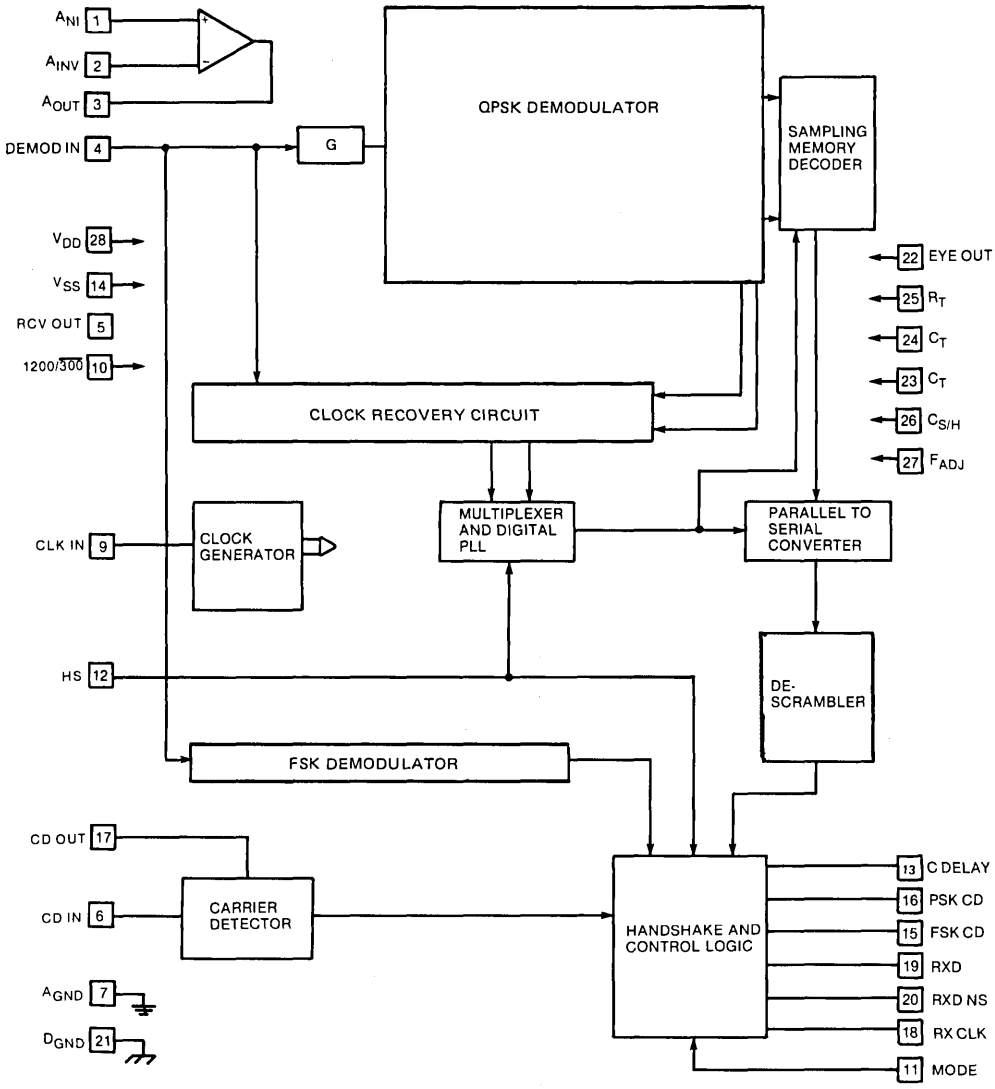
The XR-2122 provides two basic types of operation; demodulation for either 1200 BPS DPSK or 300 BPS FSK encoded incoming carriers. For either speed, the incoming carrier is passed through a gain stage (uncommitted op amp) and an AGC circuit to condition the signal. For 1200 BPS, the signal is processed using coherent demodulation techniques (Costas Loop).

For 300 BPS, a digital phase-locked loop type of demodulator is used providing low bias and jitter distortion without adjustments.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, T_A = 0-70°C, CLK IN = 1.8432 MHz ± .01%, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{DD}	Quiescent Positive Supply Current		8	12	mA	Normal Operation
I_{SS}	Quiescent Negative Supply Current		-8	-12	mA	Normal Operation
DIGITAL CHARACTERISTICS						
I_{IN}	Input Current			10	µA	$V_{IN} = V_{DD}$ or GND
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA
V_{OL}	Output Loss Voltage		0.4	0.8		I_{OL} = 2 mA
ANALOG CHARACTERISTICS (Circuit Configuration of Figure 11)						
A_{VG}	Amplifier Open Loop Gain		60		dB	
$V_{DEMOD\ IN}$	Typical Input Voltage to DEMOD IN		-6		dBM	
$Z_{DEMOD\ IN}$	DEMOD IN Input Impedance		15		KΩ	
$Z_{CD\ IN}$	CD IN Input Impedance		50		KΩ	
CD ON	CD On Level		-32	-30.5	dBM	
CD OFF	CD Off Level	-35.5	-34		dBM	
$T_{d\ CD}$	CD Off/On Delay Time	10	17	24	ms	
$T_{dlh\ FSK}$	FSK CD Off/On Delay Time	105	150	205	ms	
$T_{dhl\ FSK}$	FSK CD On/Off Delay Time	10	17	24	ms	
$T_{dlh\ PSK}$	PSK CD Off/On Delay Time	200	270	350	ms	C Delay = 0.47 µF
$T_{dhl\ PSK}$	PSK CD On/Off Delay Time	10	17	24	ms	
f_{VCO}	VCO Frequency Answer Mode Originate Mode		 4.8 9.6		 KHz Khz	



EQUIVALENT SCHEMATIC DIAGRAM

PRINCIPLES OF OPERATION

The XR-2122 is designed to perform the complete demodulator function in a Bell 212A type modem system. It has been specifically designed to complement the XR-2120 filter, XR-2121 modulator, and XR-2125 data buffer to form a four chip Bell 212A type modem signal processor. This four chip set is known as the XR-212AS and is covered in depth in Application Note AN-28. This data sheet will deal specifically with the XR-2122 and its functions.

The XR-2122 performs two different types of demodulation; 300 BPS frequency shift keyed (FSK) and 1200 BPS differential phase shift keyed (DPSK) encoded carriers.

First consider the 1200 BPS type of demodulation. For this demodulator operation, the XR-2122 accepts a DPSK encoded carrier (R_{XC}) typically from the telephone switched network, and demodulates it to produce a serial received data output. This serial data stream is synchronous, that is a clock, R_X CLK, is used for synchronization purposes.

The DSPK encoded receive carrier, R_{XC}, is first applied to an automatic gain control circuit, AGC. This circuit, shown in Figure 1, provides a constant voltage output for a wide dynamic range input signal.

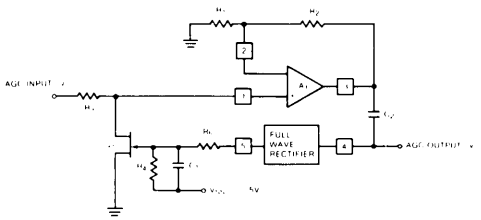


Figure 1. AGC Circuit

Operation of the AGC is as follows. V_O is internally set to about 1.5 volt peak-to-peak. The gain (non-inverting) of A_1 is set by R_2 and R_1, and is R_2/R_1 for $R_2 >> R_1$. With the gain of A_1 set and a constant V_O, the input voltage to A_1's non-inverting input will be a constant voltage: $V_{NI} = (V_O) \div (R_2/R_1)$. FET Q_1 acts as a variable resistor to form a voltage divider with R_3 for the input signal. Q_1's resistance is controlled by the feedback path from A_1's output, through C_2, the full-wave rectifier and filter network R_4-R_5-C_1. The feedback will control the resistance of Q_1 in such a way that the voltage divider action it produces with R_3 will produce the precise voltage at V_{NI} of A_1, which, when multiplied by A_1's gain, will produce the correct V_O. Values are given in the applications section for a typical circuit which will accept an input dynamic range of -40 dBM to 0 dBM.

The output of the AGC, which is really a constant amplitude R_{XC}, is fed to two different circuits. One is for carrier recovery and one for clock recovery. The carrier recovery circuit is a Costas Loop. The error voltage outputs of the Costas Loop are fed to a sampling memory decoder which will produce dibits, or pairs of bits, which are extracted from each R_{XC} phase change. Figures A, B, and C show the eye diagram at the output of the Costas Loop with the receive clock, R_X CLK. The eye diagram is the prime indicator of demodulation quality in a cohert type demodulator. The R_X CLK sets the point where the eye is sampled, which should be at the point of zero intersymbol interference, or, in other words, at the eye's maximum opening. The three photographs were taken at Pin 22, eye out, with a complete modem signal processor utilizing the XR-2121 modulator, XR-2120 filter, and XR-2125 data buffer. The eye opening, or quality of demodulation, changes with different line (telephone) quality. The three photos show the eye and R_X CLK for:

A) Back-to-back operation, or two modems directly tied together, A1 is originate and A2 is answer mode.
B) A 3002, C2 conditioned phone line. B1 is originate and B2 is answer mode.
C) A 3002 C0 unconditioned phone line. C1 is originate and C2 is answer mode.

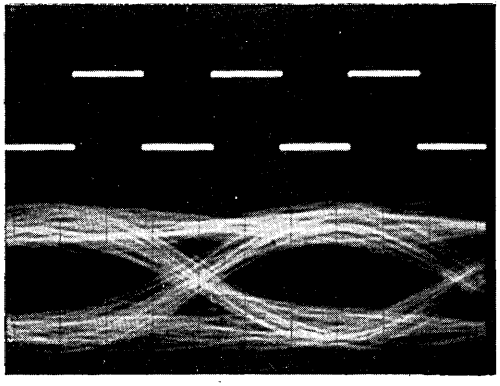


Figure. A1

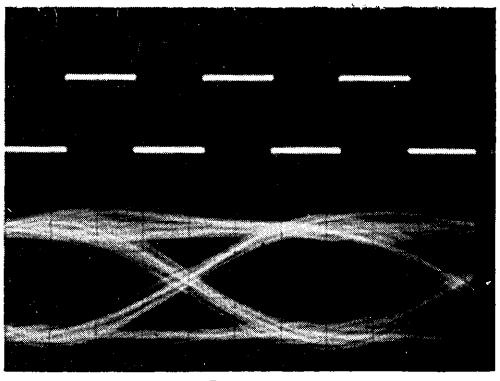


Figure. A2

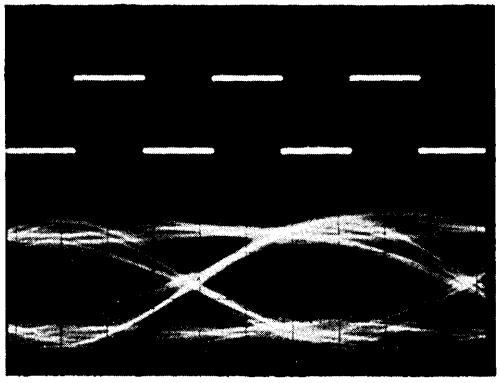


Figure. B1

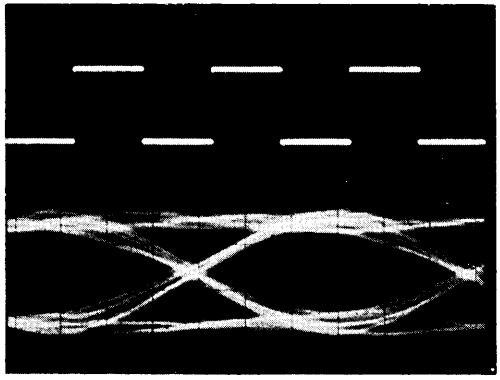


Figure. B2

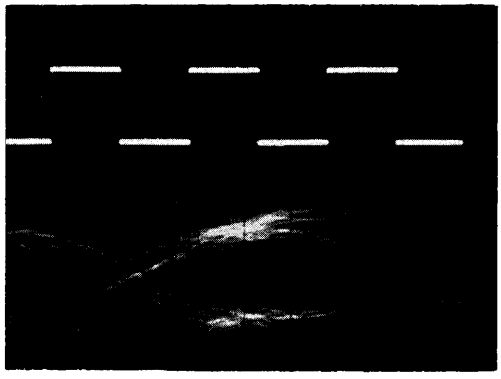


Figure. C1

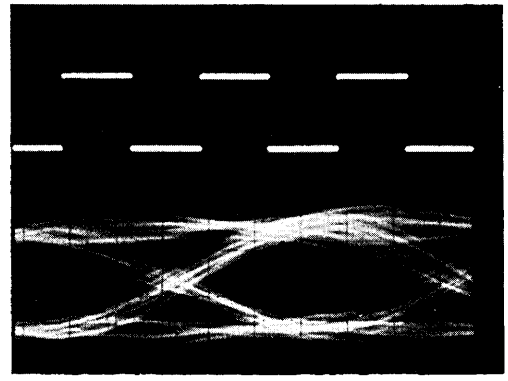


Figure. C2

More information is given on this subject in Application Note AN-28. DPSK encoding introduces a phase shift to a constant frequency carrier every two data bits, or dibits (see XR-2121 modulator data sheet). Table 1 shows the four possible dibits for phase changes of R_{XC}. The XR-2122 conversely produces two data bits for each phase change. The two carrier frequencies are 1200 Hz and 2400 Hz; Table 2 shows the Mode/Frequency convention.

R_X CAR PHASE SHIFT	OUTPUT DIBIT
90°	0 0
0°	0 1
180°	1 0
-90°	1 1

Table 1. Dibit Values for R_{XC} Phase Changes

MODE	RECEIVE CARRIER FREQUENCY
Answer	1200 Hz
Originate	2400 Hz

Table 2. Carrier Frequency Assignments

The mode is controlled by a logic level on pin 10. The dibits are returned to serial form by a parallel to serial converter. Next, the serial data stream is descrambled; the circuitry for this function is shown in Figure 2.

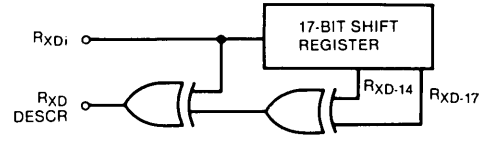


Figure 2. 17 Bit Psuedo Random Descrambler

The descrambler is necessary as all Bell 212A type modems use a scrambled data format for the 1200 BPS speed. This is used to insure that certain data patterns which would cause few, or no phase changes, ever exist. The output of the descrambler can be described by:

$$R_{XD\ DESCR} = R_{XDI}\ (1 \oplus R_{XD\ -14} \oplus R_{XD\ -17})$$

For timing purposes during 1200 BPS operation, a clock must be extracted from the received carrier, R_{XC}. This clock represents a baud period and is 600 Hz. It is used internally for sampling and multiplied by two, 1200 Hz, and output on pin 18, R_X CLK. The timing relationship between R_X CLK and output data, R_{XD}, is shown in Figure 3.

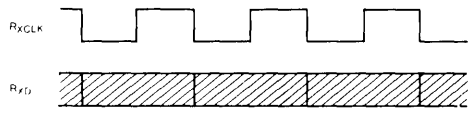


Figure 3. R_{XD}/R_X CLK Relationships

As seen in Figure 3, R_{XD} changes on the falling edge of R_X CLK.

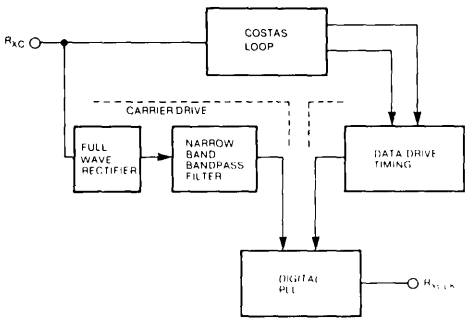


Figure 4. Timing Recovery Circuit

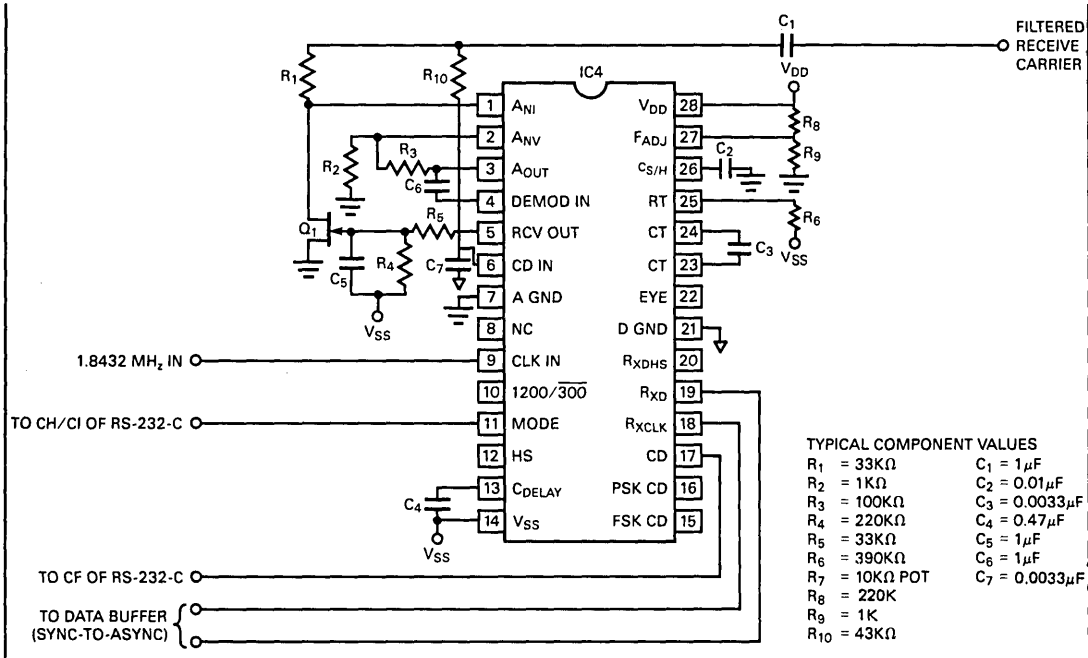
Clock recovery is accomplished from both the received carrier, R_{XC}, and data drive timing. Initially, the clock is recovered from R_{XC} for quick response and then assisted by the Costas Loop for data drive. A digital phase-locked loop, PLL, locks the two types of R_X CLK's together for a more stable clock. This clock is used internally for sampling and timing, and outputted on pin 18, R_X CLK, for sampling use externally.

The demodulation for the 300 BPS operation accepts an FSK encoded carrier and produces an asynchronous serial data output. Since it is asynchronous, no R_X CLK is used. The R_{XC} from the AGC output is fed to a digital phase-locked loop, PLL. The error voltage of the PLL is low pass filtered using switched capacitor filter techniques and compared against a reference voltage to produce the demodulated output.

The output of the two demodulators, FSK and DPSK, are fed into a handshake and control logic section. The primary purpose of this section is to decide whether the incoming carrier, RXC, is FSK or DPSK encoded, or, in other words, which speed the carrier modulation is: 300 BPS or 1200 BPS. This produces an auto speed control circuit. During the initial handshake routine, the XR-2122 will first look for an FSK R_{XC}. It does this by an FSK mark sensor which looks for five consecutive errors. If this condition occurs, operation will automatically be switched to 1200 BPS DPSK. The handshake circuit produces three carrier detect, CD, outputs; an FSK CD (pin 15), PSK CD (pin 16), and an energy level type CD (pin 17) which will respond to all in-band signals.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	A_{NI}	This is the input op amp non-inverting input. This op amp is typically used in the AGC circuit.
2	A_{INV}	The inverting input of the input op amp.
3	A_{OUT}	The output of the input op amp.
4	DEMOD	The input to both 300 BPS and 1200 BPS demodulators. Also the AGC output.
5	R_{CV} OUT	This pin is used to drive the gate of an external FET used in the AGC circuit.
6	CD IN	The input to the carrier detect circuitry.
7	A_{GND}	Analog ground for the linear circuitry of the XR-2122. This ground should not carry logic current to avoid ground noise.
9	CLK IN	The master clock input, typically 1.8432 MHz ±0.01%.
10	1200/$\overline{300}$	Speed select input for selecting 1200 BPS DPSK or 300 BPS FSK operation.
11	MODE	Mode selection for answer or originate mode.
12	HS	Handshake enable/disable input. The handshake is primarily an auto speed selection circuit with a full description with the text section.
13	C_{DELAY}	Provides carrier detect turn-off and turn-on timing programming.



TYPICAL COMPONENT VALUES

R_1 = 33KΩ	C_1 = 1μF
R_2 = 1KΩ	C_2 = 0.01μF
R_3 = 100KΩ	C_3 = 0.0033μF
R_4 = 220KΩ	C_4 = 0.47μF
R_5 = 33KΩ	C_5 = 1μF
R_6 = 390KΩ	C_6 = 1μF
R_7 = 10KΩ POT	C_7 = 0.0033μF
R_8 = 220K	
R_9 = 1K	
R_{10} = 43KΩ	

FIGURE 11. TYPICAL CONNECTION DIAGRAM

14	V_{SS}	Power supply input for the negative power supply. This supply is -5.0 ± 0.25 volts and should be well by-passed with decoupling capacitors.
15	FSK CD	This is the FSK CD output.
16	PSK CD	Provides the DPSK CD output.
17	CD	The energy-type CD output.
18	R_X CLK	Receive clock output which is a 1200 Hz square wave derived from the incoming DPSK encoded carrier, R_X CLK. Used for external timing of R_{XD}.
19	R_{XD}	Serial receive data output for either 1200 BPS DPSK or 300 BPS FSK.
20	R_{XD} NS	This provides a receive data output before the internal descrambler.
21	D_{GND}	The ground for the digital logic of the XR-2122. This pin should be connected to A_{GND} at the power supply - single point ground.
22	EYE	The Costas Loop eye diagram output is available at this pin.
23/24	C_T	The Costas Loop voltage controlled oscillator, VCO, timing capacitor is connected between these pins.
25	R_T	The Costas Loop VCO timing resistor.
26	$C_{S/H}$	Sample and hold capacitor is connected between this pin and analog ground, A_{GND}.
27	F_{ADJ}	Costas Loop VCO fine tuning input.
28	V_{DD}	Power supply input for the positive supply. This supply is +5.0 ± 0.25 volts and should be well bypased with decoupling capacitors.

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2122.

PIN	NAME	FUNCTION LOGIC HIGH	LOGIC LOW
10	1200/$\overline{300}$	1200 BPS DPSK Operation	300 BPS FSK Operation
11	MODE	Answer Originate	Originate
12	HS	Handshake Function/Enable	Handshake Function/Disabled

Table 3. Control Input Conditions

APPLICATIONS

The XR-2122 is shown in a typical connection in Figure 11.

In a complete modem system the received carrier, R_{XC}, would come from the receive filter such as the XR-2120. For the XR-2122 it would be either a FSK or DPSK encoded carrier typically from the telephone network. The data output, R_{XD}, would be either a 300 BPS serial bit asynchronous or 1200 BPS serial synchronous data stream. In a full application (AN-28), the R_{XD} output would go through the XR-2125 data buffer. For the 1200 BPS operation, the data buffer will convert the XR-2122 synchronous data into a character asynchronous format with a character length of 9 or 10 bits.

The input signal range of the R_{XC} is -40 dBM to 0 dBM for the AGC values given.

Figure 13 shows R_8 and R_9 replaced by potentiometer P_1.

Potentiometer P_1 adjusts an internal DC offset in the Costas Loop, or 1200 BPS section of the XR-2122. For optimum system performance, it should be adjusted for maximum eye opening at pin 22, EYE OUT (see Figure 12). Figure 13 shows the test set-up for observing the eye output of 1200 BPS and determining the demodulation quality.

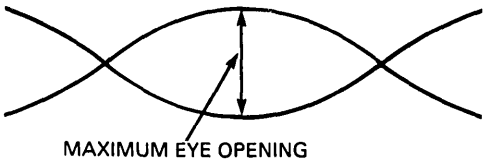


Figure 12. Eye Diagram Characteristics

Further, more complete applications information on the XR-2122 is given in Application Note AN-28 which covers the device used in a complete system.

Bell 212A Handshake Protocol

The XR-2122 performs the sensing for the Bell 212A handshake protocol. With the handshake pin, pin 12, pulled high (+5 V), the XR-2122 will perform energy and sensing and indication, and auto speed adjust. These functions can be utilized to complete the Bell 212A handshake. Timing parameters are illustrated in Figure 14A and 14B.

Since the XR-2122 will change speeds internally, overriding the speed selection pin (pin 10), the designer must provide a means for selecting the required handshake protocol carrier from the modulator, the XR-2121. This selection can be achieved in hardware or software.

3

Addendum:

Handshake:

The handshake pin (HS), pin 12, must be low when the device is first powered up. The reason for this is that at power up, the digital portions of the XR-2122 will reset to an initial state. The HS pin being high will prevent this from occurring. It is best to have the HS pin low for 2 seconds to allow the reset to completely finish.

AGC:

The requirements for the AGC Field Effect Transistor that is tied to pin 1 (A_{N1}) is as follows:

V_{GS} (gate-source cut-off voltage) =
−0.8 V minimum, −4.0 V maximum
$V_{DS(on)}$ (drain-source on voltage =
0.5 V at I_D = 5 mA maximum
$r_{ds(on)}$ (drain-source on resistance) =
60 ohms maximum
BV_{GSS} (gate-source breakdown voltage =
−30 V minimum

The 2N4681 meets these requirements and is used for all demonstrations in EXAR's labs.

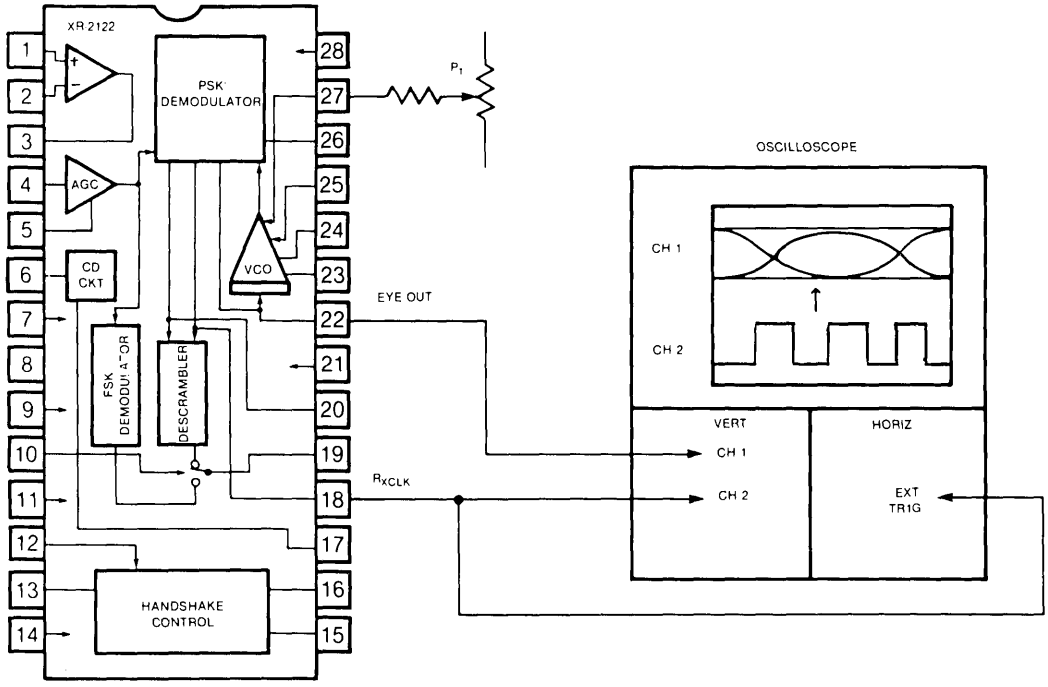


Figure 13. Set-up for Eye Diagram Output

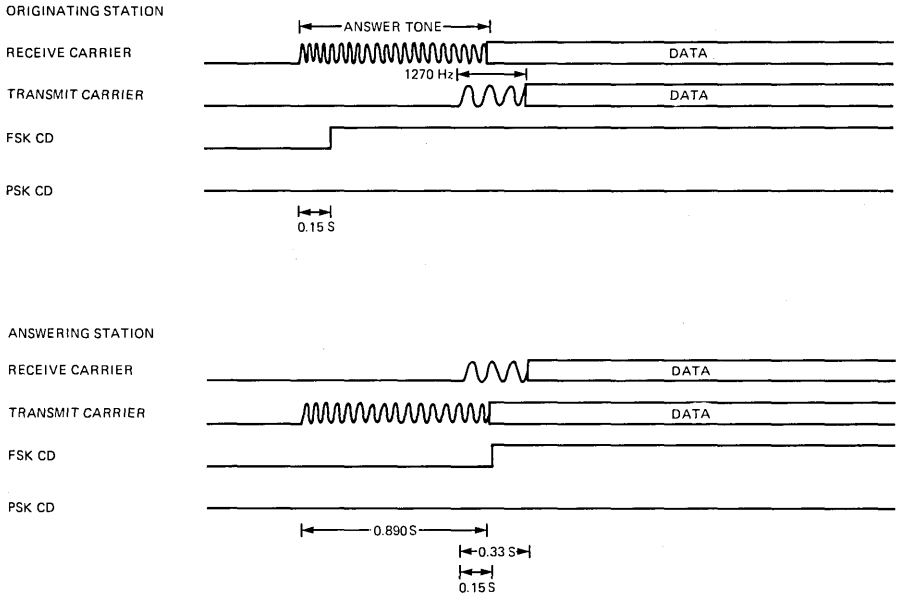


Figure 14A. 212A Handshake 300 BPS

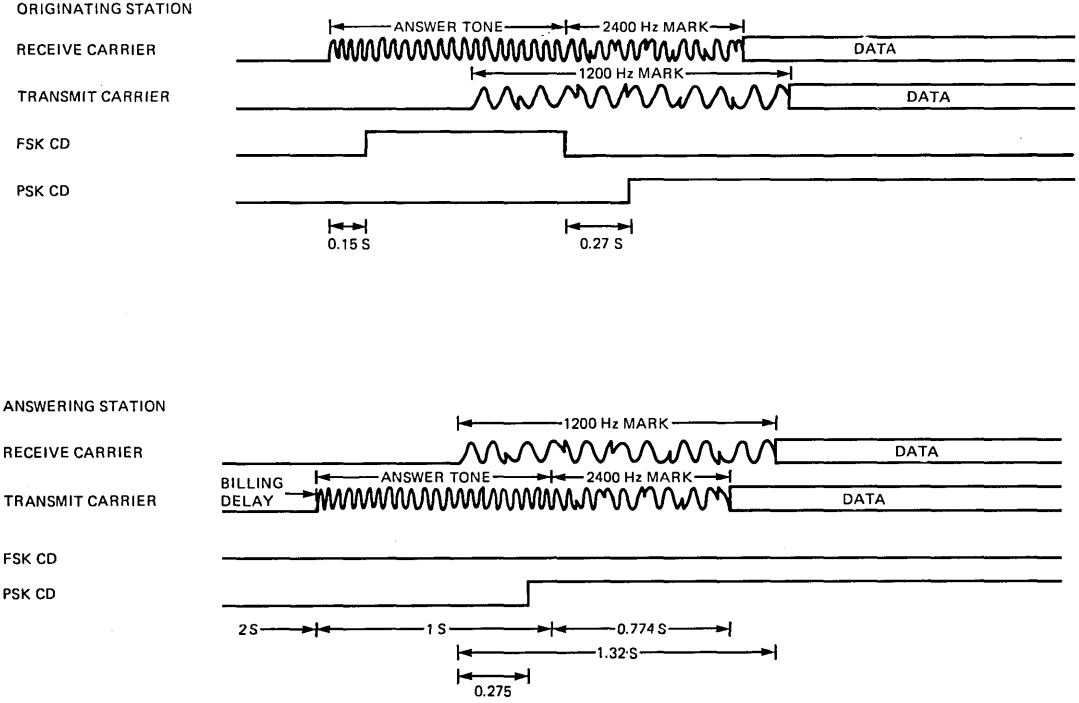


Figure 14B. 212A Handshake 1200 BPS