EXAR XR-2123/2123A

PSK Modulator/Demodulator

GENERAL DESCRIPTION

This series of devices provide the modulator and demodulator for phase-shifted keyed modulated signals. The devices have an on-chip digital-to-analog converter, allowing digital external programming of Bell 212A, CCITT V.22 or V.26 functions.

The XR-2123 provides the modulator and demodulator functions. It is adequate for Bell 212A (1200 BPS only) and Bell 201 standards. The XR-2123 requires a synchronous-to-asynchronous converter and scrambler-descrambler for the digital portion of the modem for 212A applications. Level shifters and filtering is required for the analog portion.

The XR-2123A provides the ±7 Hz carrier capture range needed for V.22 and V.26. It is externally identical to the XR-2123.

The XR-2123 and XR-2123A utilize CMOS technology for power operation while providing single 5 volt operation. Both devices come in a 28 pin DIL pin package in either plastic or ceramic.

FEATURES

Single +5 Volt Operation
Low Power Consumption (typ. 10 mw)
1200 BPS Full Duplex
2400 BPS Half Duplex
Programmable for US or European Standards (CCITT)
Dibit PSK (DPSK) Operation
Cyrstal Controlled
Synthesized Sine Wave Modulator Output
Adjustable Modulator Output Amplitude
Input Protection

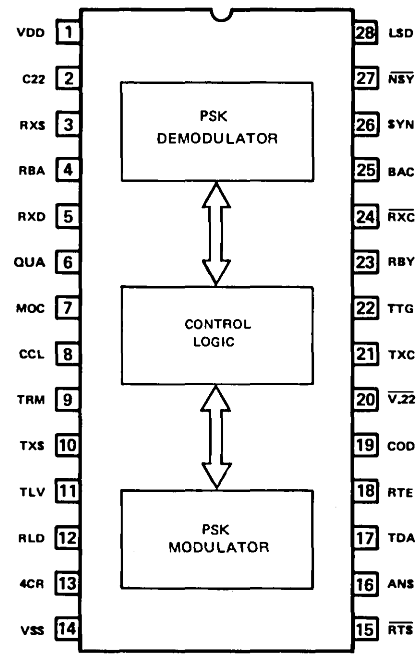
APPLICATIONS

Bell Standard 201 or 212A Modems
CCITT Standard V.22 or V.26 Modems

ABSOLUTE MAXIMUM RATINGS

Power Supply	5.5 V
Power Dissipation	1.0 W
Derate Above 25°C	5 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
All Input Voltage	-0.5 V to (V_{DD} to 0.5 V)
DC Current Into Any Input	± mA

FUNCTIONAL BLOCK DIAGRAMS



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2123CN	Ceramic	0°C to +70°C
XR-2123CP	Plastic	0°C to +70°C
XR-2123ACN	Ceramic	0°C to +70°C
XR-2123ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2123 and XR-2123A provide the complete modulation and demodulation of DPSK modem systems. The modulator transmits a sampled sine wave in dibit phase-shifted keyed format (DPSK). The phase shifts and carrier frequencies are controlled with logic inputs. With these controls, a Bell 212A/CCITT V.22 or a Bell 201/CCITT V.26 can be created.

The XR-2123 and XR-2123A require a separate scrambler/descrambler and synchronous-to-asynchronous converter.

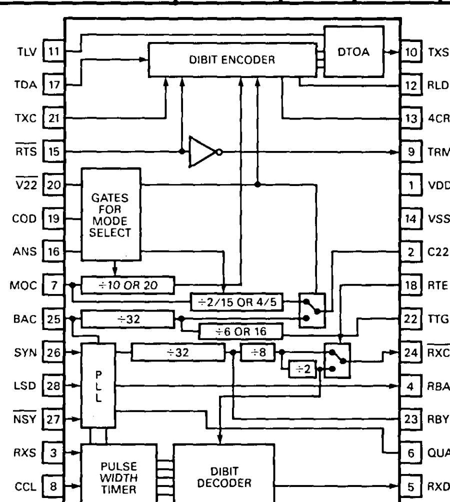
ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5V, V_{SS} = 0V, T_j = 0°C to 70°C

Digital Inputs: RXS, MOC, CCL, $\overline{RTS}$, ANS, TDA, RTE, COD $\overline{V22}$, TXC, BAC, SYN, $\overline{NSY}$, LSD

Digital Outputs: C22, RBA, RXD, QUA, TBA, 4CR, TTG, RBY, $\overline{RXC}$

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 MA
V_{OH}	Output High Voltage	4.6			V	I_{OH} = 1.0 MA
V_{IL}	Input Low Voltage	-0.5		11	V	
V_{IH}	Input High Voltage	3.5		5	V	
I_{IL}	Input Leakage Current				pA	
I_{DD}	Power Supply Current		2.5	4	MA	
C_I	Input Capacitance					
t_R	Low to High Logic Transition Time		20		nS	C_L = 10 pF
t_F	High to Low Logic Transition Time		20		nS	C_L = 10 pF
V_{TXS}	Transmitted Carrier Signal Level		-9		dBm	$V_{PIN\ 11}$ = 1 V



XR-2123A FUNCTIONAL BLOCK DIAGRAM

THEORY OF OPERATION

A system using a XR-2123 or XR-2123A would require both additional analog and digital circuitry. The digital circuitry required for the XR-2123, XR-2123A is a scrambler/descrambler which is a pseudo-random pattern generator. Figure 1 showns a hardware approach of doing the scrambler/descrambler. If the modem is intended to be operated asynchronously, a synchronous-to-asynchronous converter is needed. With the XR-2123 or XR-2123A the XR-2125 can be used. If additional features are desired, a microprocessor can be used to implement both the scrambler/descrambler and the synchronous-to-asynchronous converter.

A counter circuit is needed to provide the baud clock (BAC), which needs to be synchronized with the 4.608 MHz master clock (MOC).

The analog portion of the modem circuit consists of two parts, the bit carrier recovery and the baud carrier recovery. The bit carrier occurs at either 1200 or 2400 Hz. A modem filter, such as the XR-2120, can be used to remove out-of-band signals. The signal is passed through an automatic gain control (AGC), and then through a level shifter. The signal from the level shifter is applied to Pin 3 of the XR-2123 or XR-2123A (RXS).

The baud carrier recovery is similar. After the AGC, the signal is applied to a precision full wave rectifier. The baud rate is always 600 Hz for Bell 212A (1200 BPS) or V.22. By rectifying the signal, the 600 Hz carrier appears as an amplitude modulation. After the rectifier, the signal is applied to a 600 Hz bandpass filter with an approximate Q of 20. The phase shift through this portion is very important. It must be -180° of phase shift from input to output. This is to place the baud clock in the correct reference with the recovered bit carrier. This signal is then level-shifted and applied to Pin 26, SYN. Figure 2 shows the signals after the XR-2120 after the full wave precision rectifier, after the 600 Hz bandpass filter, and after the level-shifter.

Bell 201/CCITT standard V.26 implementation with the XR-2123A requires an additonal filter and a mixer stage in the analog portion. V.26/201 is a synchronous data transmission and does not require a synchronous-to-asynchronous converter. A scrambler/descrambler is also not required, making the digital portion of the modem circuit very simple. A counter circuit to divide down the 4.608 MHz clock (MOC) for the baud clock (BAC) is the only digital circuit needed.

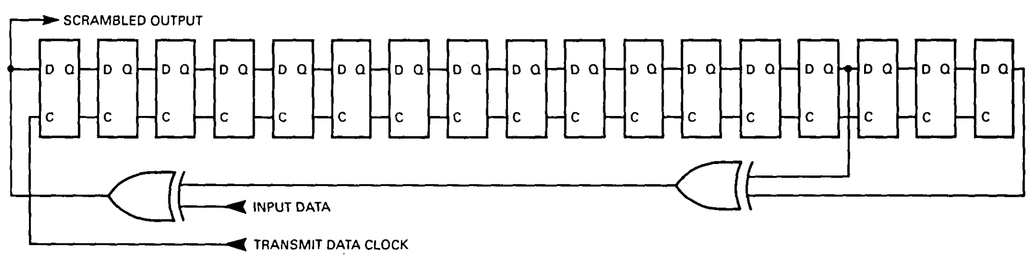


Figure 1A. Scrambler

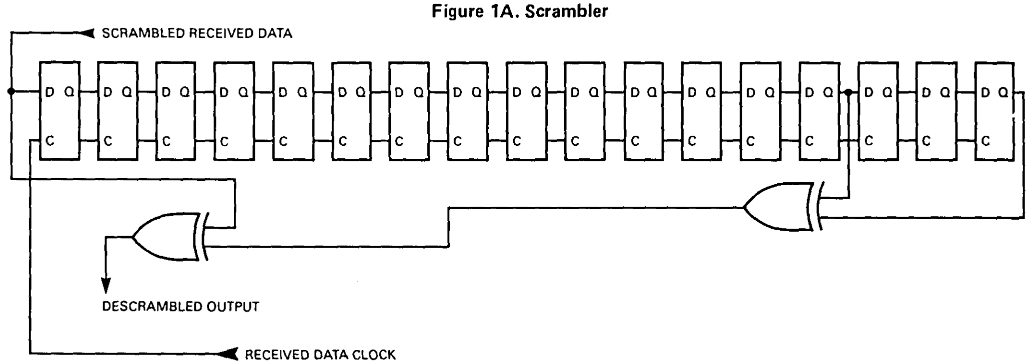


Figure 1B. Descrambler

The receive portion of the analog circuit will be discussed first. The received signal is filtered through an 1800 Hz bandpass filter with −3 dB points at 760 and 2860 Hz. This can be constructed with discrete components or with a programmable filter. After the filter, the signal is passed through an automatic gain control (AGC), A mixer is then used to bring the 1800 Hz received signal up to 9 kHz. This signal is filered through a 9 kHz bandpass filter. This filter should have a Q of approximately 9. The signal is limited and applied to Pin 3, RXS.

The baud carrier can be seen as a amplitude modulation on the 9 kHz signal. This is filtered off using a 1200 Hz bandpass filter. The Q of this filter should be approximately 2. The phase shift through this filter is very important. At 1200 Hz, the phase of the output referenced to the input should be −90°. After the 1200 Hz bandpass filter, the signal is applied to a level shifter and applied to Pin 26, SYN.

Figure 3 shows the signal after the mixer, after the 9000 Hz filter and after the 1200 Hz filter. Figure 4 shows one method of utilizing the XR-2123A for a V.26/ 201 modem. To create the optional 75 baud reverse direction, the XR-2206 and XR-2211 can be used.

The transmit output, Pin 10, of the XR-2123A or XR-2124 requires a low pass filter with a −3 dB point of 3500 Hz. Either the XR-1008 low pass filter or a discrete component filter can be used.

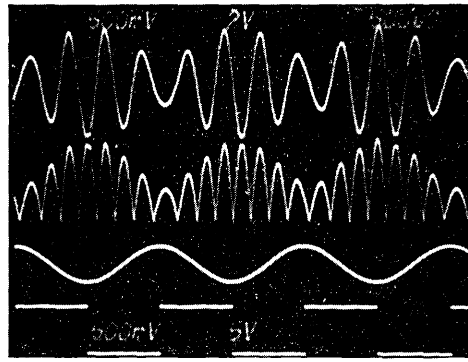


Figure 2. Showing received signal after the XR-2120, after full wave precision recitifier, after the 600 Hz bandpass filter, and after the level shifter.

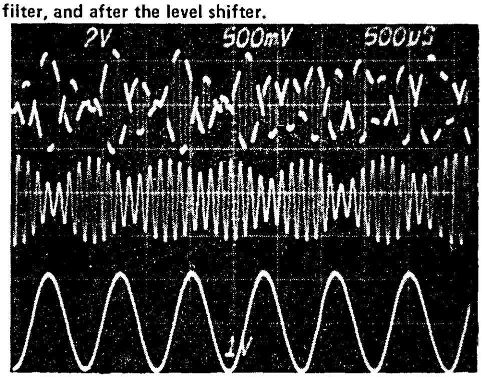


Figure 3. Showing the output of the mixer, the output of the 9000 Hz filter, and the output of the 1200 Hz bandpass filter (baud clock recovery).

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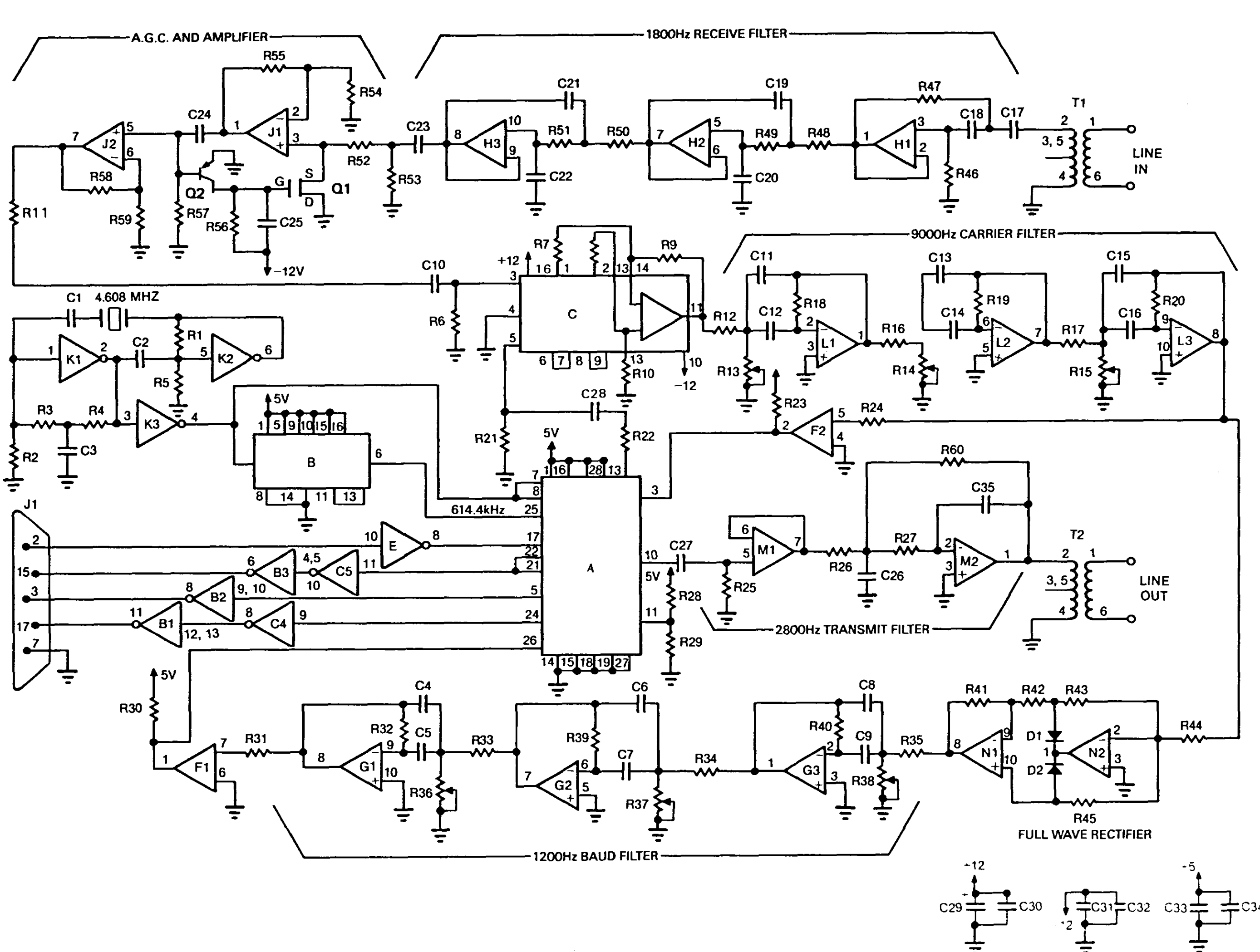


Figure 4. CCITT V.26 2400 BPS Modem Application Schematic

INTEGRATED CIRCUITS

A	XR-2123	EXAR
B	XR-1488	EXAR
C	XR-2208	EXAR
D	DM-74193	National
E	XR-1489	EXAR
F	LM-339-N	Texas Instruments
G	XR-4741	EXAR
H	XR-4741	EXAR
J	XR-1458	EXAR
K	F-7404	Fairchild
L	XR-4741	EXAR
M	XR-1458	EXAR
N	XR-4741	EXAR

CAPACITORS

C1	82 pf	C19	.01 µf
C2	.0022 µf	C20	.001 µf
C3	.033 µf	C21	.01 µf
C4	033 µf	C22	100 pf
C5	.033 µf	C23	2.2 µf
C6	.033 µf	C24	2 µf
C7	.033 µf	C25	10 µf
C8	.033 µf	C26	.033 µf
C9	.033 µf	C27	1 µf
C10	.1 µf	C28	.1 µ
C11	.0033 µf	C29	4.7 µf
C12	.0033 µf	C30	.1 µf
C13	.0033 µf	C31	4.7 µf
C14	.0033 µf	C32	.1 µf
C15	.0033 µf	C33	4.7 µf
C16	.0033 µf	C34	.1 µf
C17	.1 µf	C35	.0068 µf
C18	.1 µf		

RESISTORS

R1	1.2K	R21	2K	R41	10K
R2	2.2K	R22	100K	R42	10K
R3	2.2K	R23	10K	R43	10K
R4	2.2K	R24	10K	R44	10K
R5	2.2K	R25	1M	R45	10K
R6	2K	R26	3.32K	R46	5.76K
R7	24K	R27	2.2K	R47	2.74K
R8	24K	R28	1K	R48	2.61K
R9	50K	R29	1K	R49	75K
R10	50K	R30	10K	R50	7.87K
R11	200K	R31	10K	R51	249K
R12	43.2K	R32	82.2K	R52	120K
R13	1K POT	R33	29.1K	R53	10K
R14	1K POT	R34	29.1K	R54	1K
R15	1K POT	R35	29.1K	R55	68K
R16	43.2K	R36	500Ω POT	R56	1M
R17	43.2K	R37	500Ω POT	R57	10K
R18	109K	R38	500Ω POT	R58	4.7K
R19	109K	R39	82.2K	R59	1K
R20	109K	R40	82.2K	R60	6.8K

TRANSISTORS

Q1	2N4861	Q2	2N4403

TRANSFORMERS

T1	T2220
T2	T2220

DIODES

D1	IN914
D2	IN914

CONNECTOR

J1	RS232

Figure 4A. V.26 2400 BPS Modem System Components List

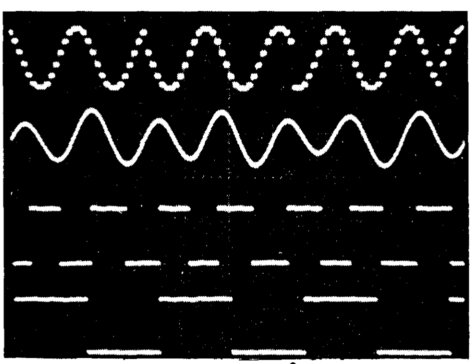
Modulation

The data to be modulated is applied to Pin 17, TDA. This must be synchronized to the transmitter bit timing clock, Pin 22, TTG. This internally creates a dibit signal which then selects the amount of phase shift needed to be encoded properly. This is coherent phase modulation which means the only phase reference is the phase of the signal before the transition.

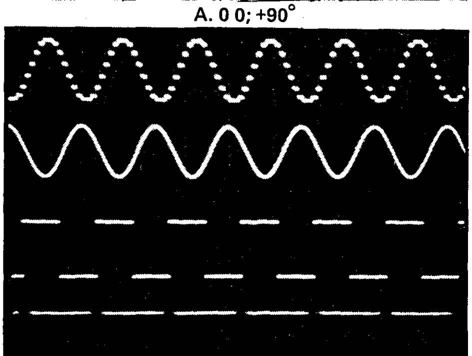
To encode the data, a counter, which accesses the digital-to-analog converter, is preset to a particular point depending on the phase change needed. Figure 5 shows four possible phase shifts with the four bit patters (00, 01, 10, 11) and the ouput of the XR-2120 filter. It should be noted that the baud rate stays at 600 Hz whether in originate (2400 Hz carrier) or in answer mode (1200 Hz data carrier).

The amplitude of the transmitted signal is controlled by the TLV, transmitter level, Pin 11. This is a DC input, typically set for 0.8 VDC. The input draws approximately 15 μA, and can be controlled with a resistor divider or a digital-to-analog converter for adapting to poor lines. Figure 6 shows the relationship between V_{TLV} and V_{TXS}.

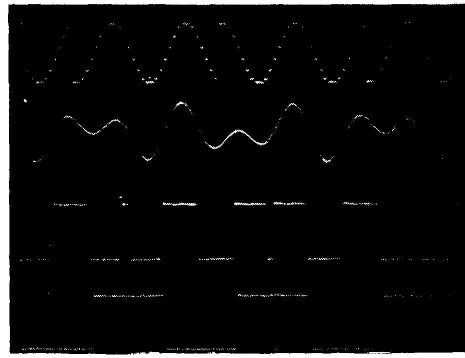
Figure 5. TXS, Transmit Output Output of 2120, Output of Limiter Recovered Baud Clock



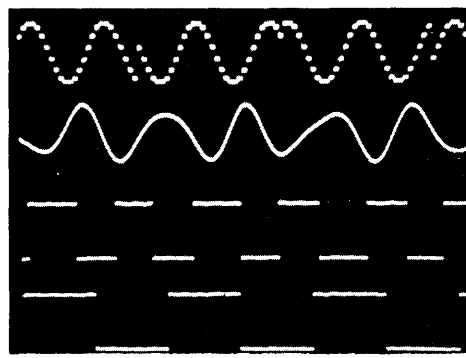
A. 0 0; +90°



B. 0 1; 0°



C. 1 0; 180°



D. 1 1; 270°

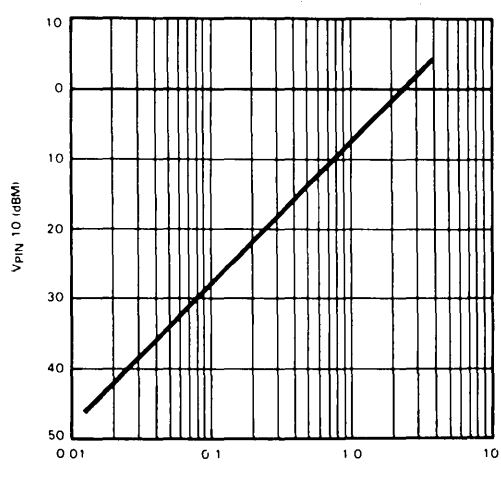


Figure 6. TXS vs. VTLV

Demodulation

The demodulator uses a pulse width measuring technique which compares the pattern received on RXS within the window set by the baud clock, applied to the synchronizer pin, SYN This is a coherent demodulation technique, so no reference phase is needed. The carrier clock, CCL, is used to time the widths of the received pulses. As it was shown in Figure 5, the phase changes produce a distinctive pulse pattern. The clock frequency applied to the carrier clock pin, CCL, is changed for each carrier frequency used. The greater the carrier frequency, the greater the carrier clock frequency.

The V.26 demodulation is the same internally. With a 1800 Hz bit carrier and a 1200 Hz phase carrier, only 1½ cycles of the 1800 Hz carrier exist within the window created by the baud clock. This does not provide enough pulses to provide an accurate measurement. Also, the baud clock is not easily recovered with the received waveform. When the received signal is mixed up to 9000 Hz, the phase carrier appears as an amplitude modulation. This can be easily detected with the full wave precision rectifier and a 1200 Hz bandpass filter.

The quality pin, Pin 6, on the XR-2123A is error jitter of the phase-lock loop. It is latched so that it remains high a minimum of approximately 1 ms. This can be used as an indication of the quality of the line in use. If the quality pin is high often, the possibility of errors is greater.

The received bit timing clock is used to synchronize the data at Pin 5, RXD. This clock is found on Pin 24, RXC. Figure 7 shows the relationship between $\overline{\text{RXC}}$ and RXD. If the XR-2125 was used, $\overline{\text{RXC}}$ is tied to Pin 9, RXC IN, and RXD is tied to RXD IN, Pin 10.

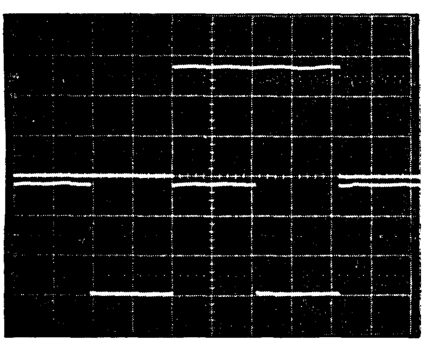


Figure 7. Top Trace RXD, Bottom Trace $\overline{\text{RXC}}$

PIN DESCRIPTIONS

Pin	Name	Description
1	VDD	+5 V_{DC} ±0.25 V
2	C22	Carrier clock for Bell 212/V.22. This output clock is used by the demodulator for timing the pulse widths of the received signal. When in the originate mode, the frequency of the pin is 614.4 kHz. When the XR-2123 or XR-2123A is set in the answer mode, the frequency at this pin is 1.2288. This allows the counter circuit in the demodulator to arrive at the same total count for a given baud rate. This pin is controlled by V.22, ANS, and COD pins on the device as shown.

	V.22	ANS	COD	C.22
1200 Hz	0	1	1	1.2288 MHz
2400 Hz	0	1	0	0.6144 MHz
See Select Mode	1	X	X	9600 Hz Mode

When V.22 is high, C.22 produces a 9600 Hz clock. This clock is not normally used for V.26 and is NOT applied to Pin 8, CCL.

Pin	Name	Description
3	TXS	Received signal input. This is the received signal input after level shifting (0-5 V). This signal carries the bit data.
4	RBA	Received baud timing. This output provides a clock at the baud rate chosen. For V.22 and Bell 212, it is at 600 Hz. For V.26, it is at 1200 Hz. It is derived from BAC and also phase locked to the signal applied to Pin 26, SYN.
5	RXD	Received data. This output is the demodulated data from the signals applied to pins 3 and 26 (RXS and SYN respectively).

3

6 2123/A QUA — The quality of demodulation. This pin shows the amount of error in the timing relationship between SYN and RBA. If the recovered baud carrier has too much noise, this pin will be high for a minimum of approximtely 1 ms. Please read the demodulation section of this data sheet for more detail.

7 MOC — Modulator clock input. This is the master clock. For V.22, Bell 212A and V.26, this clock is 4.608 MHz.

8 CCL — Carrier clock. This input is for the clock which measures the time that RXS, Pin 3, is high within one window. This input is always 512 times the received bit carrier. For example if

f_{RXS} = 1200 Hz f_{CCL} = 614.4 kHz

f_{RXS} = 2400 Hz f_{CCL} = 1.228 MHz

f_{RXS} = 9000 Hz f_{CCL} = 4.608 MHz

For V.22 and Bell 212 applications, CCL is applied from the output C.22, Pin 2, of the device. When V.26 is needed, CCL is tied to the master clock, Pin 7. The received frequency of 9000 Hz for V.26 is explained in the demodulation section.

9 TRM — Transmit mode. This output indicates the state of the modulator. When high, the device is transmitting. When low, carrier output is clamped. It is controlled by Pin 15, $\overline{RTS}$. When $\overline{RTS}$ is low, TRM is high. When $\overline{RTS}$ is high, TRM is low.

10 TXS — Transmitted signal. This is the output of the internal digital-to-analog converter. The modulated 8-level sine wave can be seen at this pin. This output is usually applied to the XR-2120 modem filter.

11 TLV — Transmitter level. This input controls the amplitude of the transmitter output, Pin 10. It typically draws approximately 15 μA and can be adjusted using a resistor divider circuit. Although not critical, this input should be relatively free of any AC component since it will cause an amplitude modulation of the TXS output.

12 RLD — Received data. This tells the terminal that the data to be transmitted has been received by the modem. It is at the baud rate of the mode the device is set in. It is counted down from BAC, Pin 25. When RLD goes high, this marks the end of the dibit set.

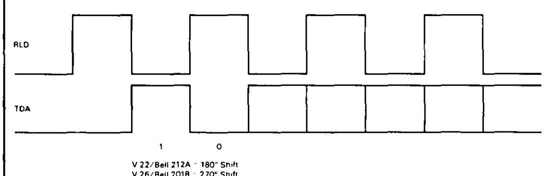


Figure 8. RLD Timing

13 4CR — Four times the carrier frequency. This output is used for the V.26 mixer in the demodulator circuit. For V.22 and Bell 212A it is not used.

14 V_{SS} — Ground.

15 $\overline{RTS}$ — Request to send. This input controls the transmitter output and the TRM, transmit mode output. The following chart describes the possibilities:

RTS	TRM	TXS
0	1	carrier
1	0	clamped to DC level

16 ANS — Answer tone. This input controls the frequency of the transmitter output. It is used along with $\overline{V.22}$ and COD. The details about using this pin is found under those two pins.

17 TDA — Transmitted data. This input is where data to be transmitted is applied. It should be synchronized to the transmit clock, Pin 22, TTG. By comparing the data applied to this pin and Pin 12, RLD, the various phase shifts can be predicted for troubleshooting purposes.

18 RTE — Rate. Control $\overline{\text{RXC}}$, Pin 24, and Pin 22, TTG. When set at a logic 1 level, the frequency at the two outputs is twice what is normally seen there. The block diagram shows the dividers controlled by RTE.

19 COD

20 $\overline{\text{V22}}$ V.22 mode

ANS answer tone

Code. These three inputs determine the mode of the modulator and demodulator of the device. Also, with these pins the 2100 Hz tone for handshaking can be created. The following truth table applies to these pins:

$\overline{\text{V.22}}$	ANS	COD	APPLICATION
0	0	0	Transmit and receive at 2400 Hz (high ch.) This is for analog loop back.
0	0	1	Transmit and receive at 1200 Hz (low ch.) This is for analog loop back.
0	1	0	Transmit at 2400 Hz (high ch.) Receive at 1200 Hz (low ch.)
0	1	1	Transmit at 1200 Hz (low ch.) Receive at 2400 Hz (high ch.)
1	0	0	Answer Tone at
1	0	1	2100 Hz.
1	1	0	V.26 mode Phase shifts have an initial 90° skew.
1	1	1	V.26 mode Phase shifts have an initial 45° skew.

21 TXC — Transmitter bit timing. This input is usually tied to Pin 22, TTG, timing for transmitter. For V.22/Bell 212A (1200 BPS), the frequency at Pin 21 is 1200 Hz. For V.26, the frequency is 2400 Hz. Note: this assumes that Pin 18, RTE, is low in both cases.

22 TTG — Timing for transmitter. This output is applied to pin 21 for all standard uses (V.22, Bell 212A, Bell 201, and V.26). It is counted down from BAC clock input. Please read the descriptions for TXC and RTE for details.

23 RBY — Received byte timing. This output is a square wave at a frequency 16 times the received baud timing. It is not normally used.

24 $\overline{\text{RXC}}$ — Received bit timing. This output is synchronized to the recovered baud carrier. It is usually used to perform the asynchronous-to-synchronous conversion.

25 BAC — Baud clock. This input is used to create the modulation and demodulation baud clock. Internal countdown circuitry sets the baud rate at either 600 Hz or 1200 Hz. For V.22/Bell 212A operation, a 307.2 kHz clock is applied to BAC. For V.26 operation, a 614.4 kHz clock is applied.

26 SYN — Synchronization. This input is where the recovered baud carrier is applied. This clock is internally applied to a phase lock loop which has BAC as the local oscillator. The error voltage is shown as the difference between $\overline{\text{RXC}}$ and RBA. This error output can be found on the quality pin, QUA, Pin 6.

27 $\overline{\text{NSY}}$ — New synchronization. This input will force the received data output to a high state. The synchronization takes place when the $\overline{\text{NSY}}$ pin is changed from high to low.

28 LSD — Line signal detector. When high, the receiver is operating normally. When this input is low, the receiver is clamped. This can be tied through an inverter to the signal applied to the $\overline{\text{NSY}}$ input.

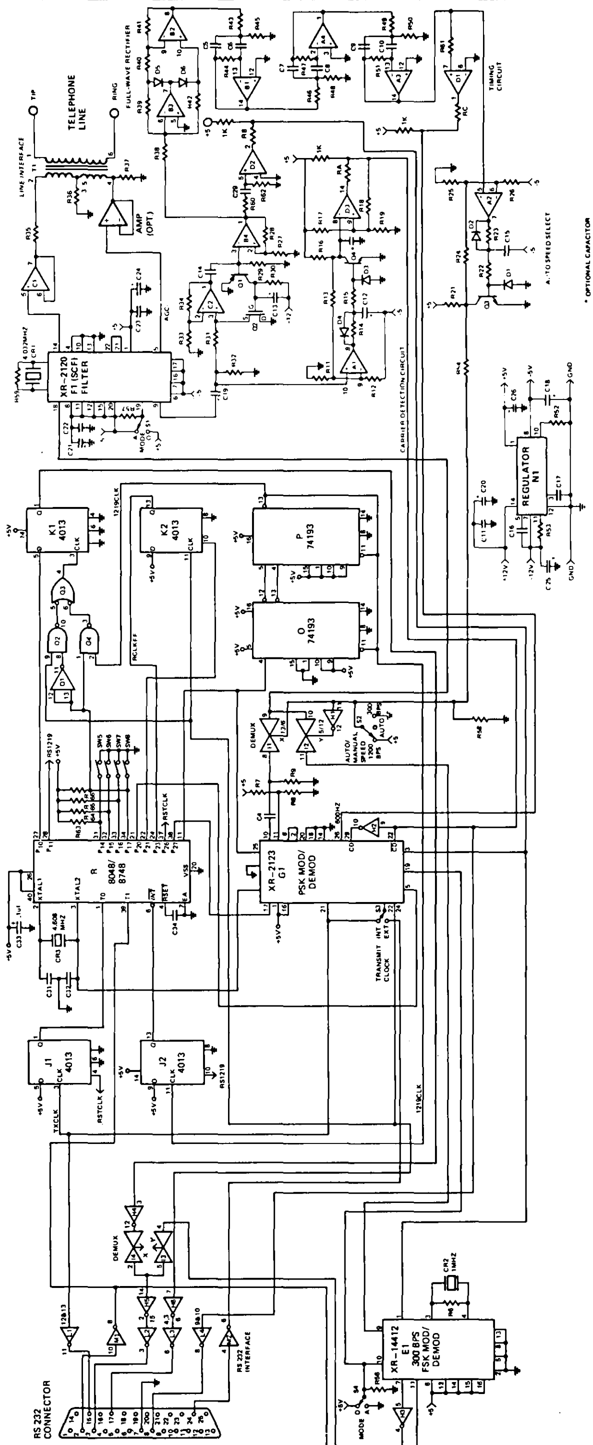


Figure 9. Bell 212A Modem Application Schematic