Pulse-Width Modulator Control System

GENERAL DESCRIPTION

The XR-2230 is a high-performance monolithic pulse width modulator control system. It contains all the necessary control blocks for designing switch mode power supplies, and other power control systems. Included in the 18-Pin dual-in-line package are two error amplifiers, a sawtooth generator, and the necessary control logic to drive two open-collector power transistors. Also included are protective features, such as adjustable dead-time control, thermal shutdown, soft-start control, and double-pulse protection circuitry.

The device provides two open-collector output transistors which are driven 180° out-of-phase, and are capable of sinking 30 mA. These outputs can be used to implement single-ended or push-pull switching regulation of either polarity in transformerless or transformer-coupled converters.

FEATURES

Thermal Shutdown
Adjustable Dead-time
Dual Open-Collector
  30 mA Output Transistors
Double-Pulse Protection Circuit
Soft-Start Control
High-Speed Remote Shut-Down Input
Two High-Performance Error Amplifiers
  with ±5V Input Common-Mode Range

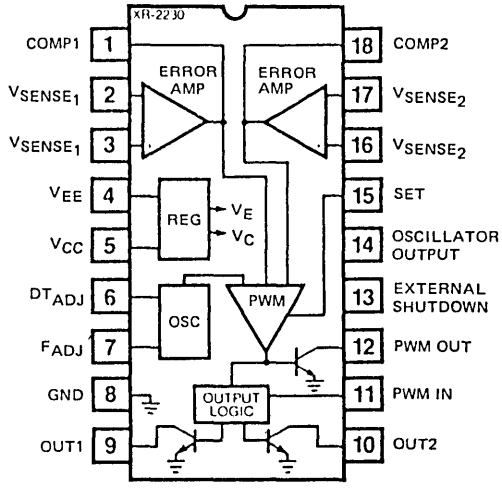
APPLICATIONS

Switching Regulators
Motor-Speed Controllers
Pulse-Width Modulated Control Systems

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	−0.5 to +18V
Negative Supply Voltage	+0.5 to −18V
Input Voltage	−18 to +18V
Output Voltage	−0.5 to +18V
Power Dissipation ($T_A \leq 25°C$)	400 mW
Operating Temperature	−10°C to +85°C
Storage Temperature	−55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2230CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2230 PWM circuit contains two high-performance error amplifiers with wide input common-mode range, and large voltage gains. Typically, one amplifier (Pins 16, 17, 18) is used for current sensing and the other (Pins 1, 2, 3) is used as an error amplifier to sense the output voltage. The XR-2230 requires a split supply between ±8 volts and ±15 volts, however, it can be operated from a single supply with proper external biasing on the ground pin and input pins of the error amplifiers. The output drivers capable of sinking 30 mA at a saturation voltage of about 0.3V can be used in a push-pull configuration, or can be paralleled for a single-ended configuration with a duty cycle between 0% to over 90%.

The XR-2230 features a self-protecting thermal-shutdown circuitry which turns off the output drivers when the junction temperature exceeds 130°C. The on-board regulator stabilizes the oscillator frequency to 0.1%/V for reliable performance.

XR-2230

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = +12V, V_{EE} = -12V, f_{OSC} = 20 kHz, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
SUPPLY SECTION						
V_{CC}	Positive Supply Voltage	+10			V	
V_{EE}	Negative Supply Voltage			−10	V	
I_{CC}	Positive Supply Current	7.0	11.0	15.0	mA	
I_{EE}	Negative Supply Current	−2.0	−6.0	−2.0	mA	
OSCILLATOR SECTION						
f_{OSC}	Frequency Range	10		100	kHz	
	Initial Accuracy			15	%	R_T = 30 kΩ, C_T = 4700 pF
	Supply Voltage Stability		0.1		%/V	V_{CC} = +10V ≈ +15V
	Low Supply Voltage	−20		+20	%	V_{CC} = +18V, V_{EE} = −8V
	Temperature Stability		0.01		%/°C	
V_{OSC}	Sawtooth Peak Voltage	3.0	3.5	4.0	V	
δ	Duty Cycle Range	10		90	%	f_{OSC} = 20 kHz
VOLTAGE ERROR AMPLIFIER						
V_{OS}	Input Offset Voltage		2	10	mV	
I_{BIAS}	Input Bias Current		−.5	−30	μA	
A_{VO}	Open-Loop Gain	60	90		dB	
f_{-3dB}	Closed-Loop Bandwidth		25		kHz	A_{VCL} = 40 dB
CMMR	Common-Mode Rejection Ratio	60			dB	V_{ICM} = ±4.5V
V_{OM}	Output Voltage Swing	±5			V	R_L = 10 kΩ, V_{CC} = +8V, V_{EE} = −8V
SR	Slew Rate	2	4		V/μs	A_{VCL} = 14 dB, R_F = 10 kΩ
	Input Voltage Range		±5		V	
CURRENT ERROR AMPLIFIER						
V_{OS}	Input Offset Voltage		4	20	mV	
I_{BIAS}	Input Bias Current		−1.0	−60	μA	
A_{VO}	Open-Loop Gain	60	90		dB	
$f_{-3\ dB}$	Closed-Loop Bandwidth		25		kHz	A_{VCL} = 40 dB
CMRR	Common-Mode Rejection Ratio	60	90		dB	V_{ICM} = ±4.5V
V_{OM}	Output Voltage Swing	±5			V	R_L = 10 kΩ
		±4			V	V_{CC} = +8V, V_{EE} = −8V
SR	Slew Rate	4	8		V/μs	A_{ACL} = 14 dB, R_F = 10 kΩ
	Input Voltage Range		±5		V	
MODULATOR SECTION						
	Set Input Open Voltage	3.1	3.6	4.1	V	
	(Pin 15)	2.8	3.3	4.3	V	V_{CC} = +8V, V_{EE} = −8V
	Modin Input Open Voltage	3.1	3.6	4.1	V	
	(Pin 11)	2.8	3.3	4.3	V	V_{CC} = +8V, V_{EE} = −8V
	Inhibit Input Current (Pin 13)	−50	−10		μA	
t_d	Inhibit Propagation Delay		60		ns	
	Out1, Out2, Output Voltage			0.3	V	I_O = 30 mA, T_A = 25°C
	(Pins 9 and 10)			0.4	V	T_A = −10 ≈ +85°C
	Low Supply Voltage			0.3	V	I_O = 27 mA, T_A = 25°C
t_f	Out1, Out2 Fall Time		30		ns	
	Modout Output Voltage			0.3	V	I_O = 16 mA, T_A = 25°C
	(Pin 12)			0.4	V	T_A = −10 ≈ +85°C
	Under Low Supply Voltage			0.3	V	I_O = 24 mA, T_A = 25°C
	Oscillator Output Voltage			0.4	V	I_O = 3 mA, T_A = 25°C
	(Pin 14)			0.6	V	T_A = −10 ≈ +85°C
	Thermal Shutdown Temp.		130		°C	

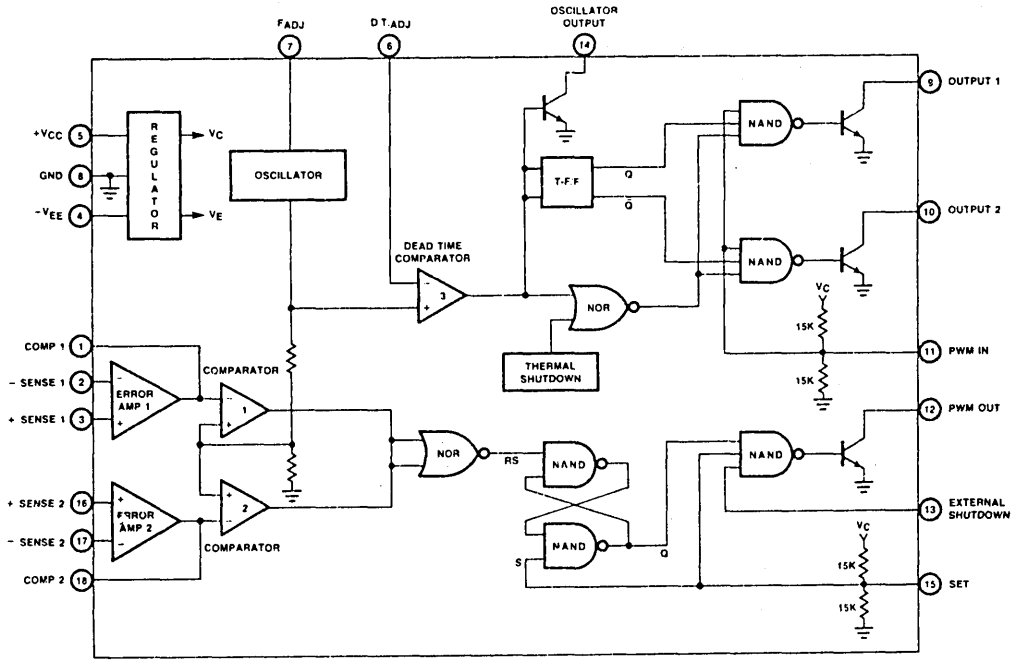


Figure 1. Equivalent Schematic Diagram

PRINCIPLES OF OPERATION

The heart of the XR-2230 is the sawtooth generator. As seen in Figure 1, this sawtooth drives one input of each of the three system comparators. Comparators one and two have their other inputs tied to the outputs of the error amplifiers. These comparators will now produce, at their outputs, square waves which will have a duty cycle proportional to the voltage at the inputs to the error amplifiers, or pulse width information. The pulse width information is fed into the NOR gate and used to provide the reset information to the pulse-width modulation flip-flop (PWM). The PWM flip-flop information is fed in to the NAND gate with the external shutdown and PWM flip-flop set input. The information from the NAND gate drives an open-collector transistor to provide the pulse-width modulation output, Pin 12. The PWM output will be a square wave with a frequency set by the sawtooth generator, and a duty cycle equal to either comparator, one or two, whichever is shorter. If the external shutdown, Pin 13 is driven low, the PWM output will remain low or go to zero duty cycle. The set input of the PWM flip-flop, Pin 15, is normally connected to the buffered sawtooth generator output, Pin 14, so that a reset pulse is provided every cycle. Each output transistor is driven by a three input NAND gate. These inputs consist of:

1. Pulse width information from the PWM input, Pin 11, which is used to control the off time of the output transistors. The PWM input is normally tied to the PWM output so that the output transistor's off time is a function of the error amplifier's input voltage.

2. Pulse-steering information from flip-flop two, which will determine which output transistor receives the PWM input signal. Flip-flop two will toggle once every cycle of the sawtooth generator's output, which will make the output transistor's toggle frequency one-half that of the sawtooth generator's.

3. Information from dead-time and thermal shutdown circuitry. The dead-time is an externally adjustable time between one output transistor turning off and the other turning on. This is used to protect external circuitry. This dead-time is controlled by an external voltage applied to Pin 6, which is internally compared with the sawtooth waveform. The thermal shutdown circuitry will drive the input to the NAND gate low, if the junction temperature exceeds 130°C. This will make both outputs low.

The circuit control blocks and functions operate as follows:

Error Amplifiers—These are high-gain op amps which are used to sense output conditions, voltage and current, and provide a dc voltage to comparators one and two. This will in turn adjust the PWM output duty cycle and ultimately that of the output transistors to correct for errors in the output voltage or overcurrent conditions. The amplifier's outputs are provided for tailoring the closed-

loop gain or frequency response of the system. Figure 2 shows the relationship between output duty cycle, Pins 11 and 12 connected, and the voltage at Pins 1 or 18. Amplifier two is approximately twice as fast as Amplifier one, and should, therefore, be used to sense output current.

External Shutdown, Pin 13—A low level signal applied to this pin will turn both outputs on. If not used, this input should be left open-circuited. The impedance at this node is approximately 1 MΩ.

Oscillator Output, Pin 14—This is an open-collector output which will be a square wave with a frequency set by the sawtooth generator. The duty cycle of this output will vary from 10 to 90%, and is a function of the dead-time setting. This pin is normally connected to Pin 15, set to provide reset pulses for the PWM flip-flop.

Set, Pin 15—This is the set input for the PWM flip-flop. A low-going signal at this pin will cause the flip-flop to be reset. The impedance at this pin is approximately 7.5 kΩ. This pin is normally connected to the oscillator output, Pin 14.

PWM Out, Pin 12—This is an open-collector output which provides a square wave with a duty cycle determined by the error amplifiers. This output is normally connected to PWM IN, Pin 11.

PWM In, Pin 11—This is the input which controls the duty cycle of the output transistors. A low level on this pin will drive both output transistors on. The impedance into this pin is approximately 7.4 kΩ.

Output Transistors, Pins 9 and 10—These pins provide the open-collector output transistors which are capable of sinking 30 mA, typically. They are alternately turned off, 180° out-of-phase, at a rate equal to one-half the frequency of the oscillator.

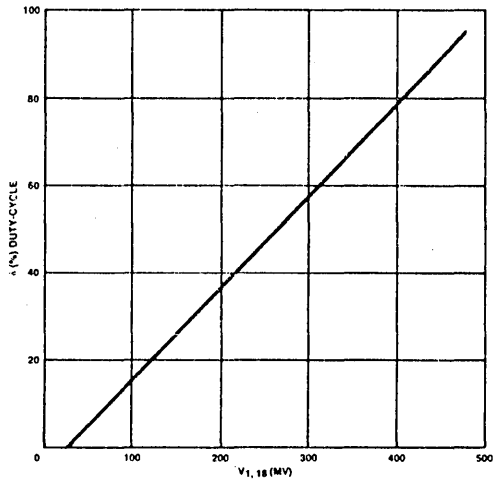


Figure 2. Modulation Duty Cycle vs Error Voltage

F_{ADJ}, Pin 7—A resistor, R_{ext} to $+V_{CC}$, and a capacitor, C_{ext}, to ground from this pin, set the frequency of the sawtooth and oscillator output, by the relationship:

$$F_{OSC} = \frac{2.68}{R_{ext} \times C_{ext}}$$

The sawtooth waveform a signal varying from zero volts to +5V, will be present at Pin 7. Normal values of R_{ext} will range from 1 kΩ to 100 kΩ. Figure 3 shows the oscillator period as a function of various R_{ext} and C_{ext} values.

The dead-time (minimum time from one output turning on to the other turning off) is controlled by the voltage applied to Pin 6.

Dead-time Control, Pin 6—Figure 4 shows output deadtime as a function of $V_{PIN\ 6}$. The maximum duty cycle of each output is also controlled by the dead-time, and may be determined by the following expression:

$$\text{Duty Cycle Max (\%)} = \left(1 - \frac{.35}{V_{PIN\ 6}}\right) \times 50\%$$

$$V_{PIN\ 6} < 3.5V$$

The impedance into this pin is approximately 10 kΩ.

APPLICATIONS INFORMATION

The soft-start function may be implemented as shown in Figure 7. This configuration will reduce the output duty cycle to zero, and gradually increase to its normal operating point, whenever power is applied to the circuit, or after an external shutdown command has been given. This is used to keep the magnetics in the circuit from saturating.

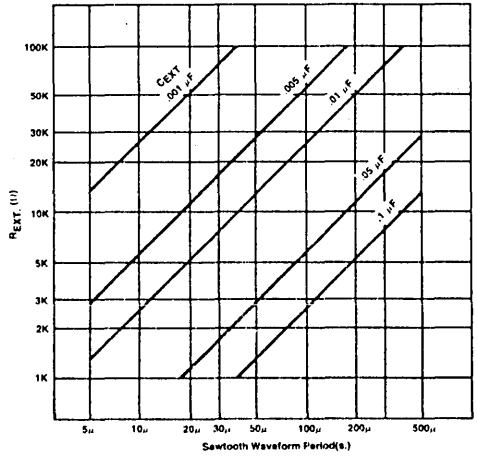


Figure 3. Oscillation Period vs R_{EXT} and C_{EXT}

The time for the duty cycle to start will be approximately equal to $R_1 \times C_1$.

A typical step-down switching regulator configuration is shown in Figure 8. Only one output transistor is used, so that the maximum duty cycle will be limited to 45%. If a larger duty cycle range is needed, the two outputs may be externally NOR'd as shown in Figure 9. This configuration will allow up to 90% duty cycles.

Figure 10 shows a detailed timing diagram of circuit operation.

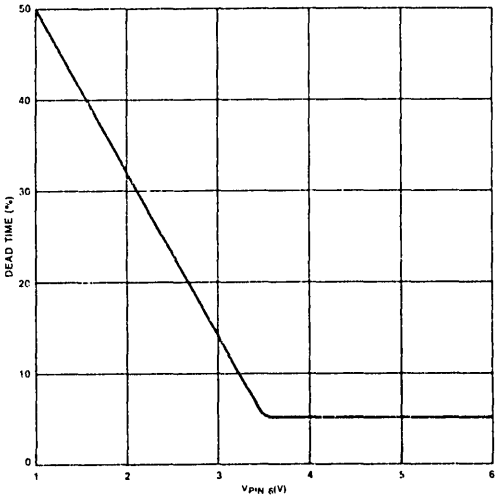


Figure 4. Dead Time vs Dead Time Adjustment Voltage

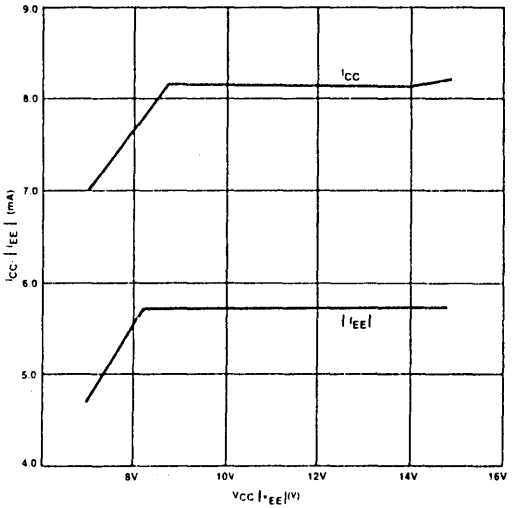


Figure 5. Supply Current vs Supply Voltage

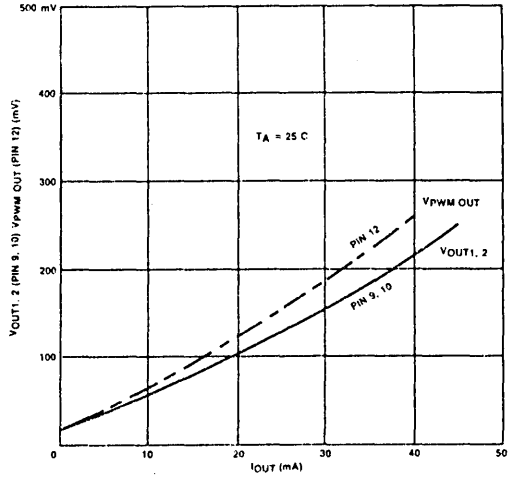


Figure 6. Output Saturation Voltage vs Load Current

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	UNIT
V_{CC}	Positive Supply Voltage	$+10 \approx +15$	V
V_{EE}	Negative Supply Voltage	$-10 \approx -15$	V
R_R	Minimum Feedback Resistance	10	kΩ
A_V	Minimum Voltage Gain	14 5	dB V/V

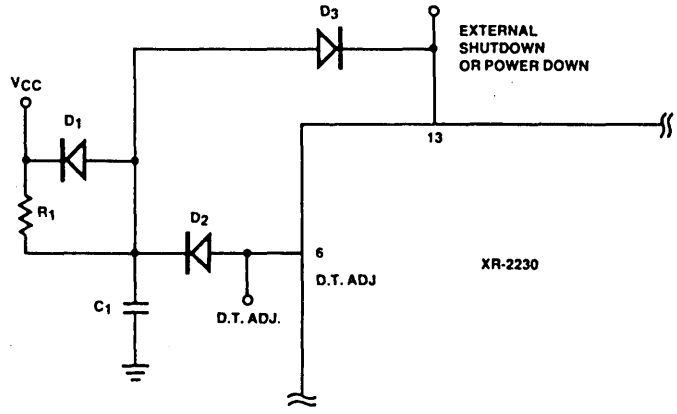


Figure 7. Soft Start Connection

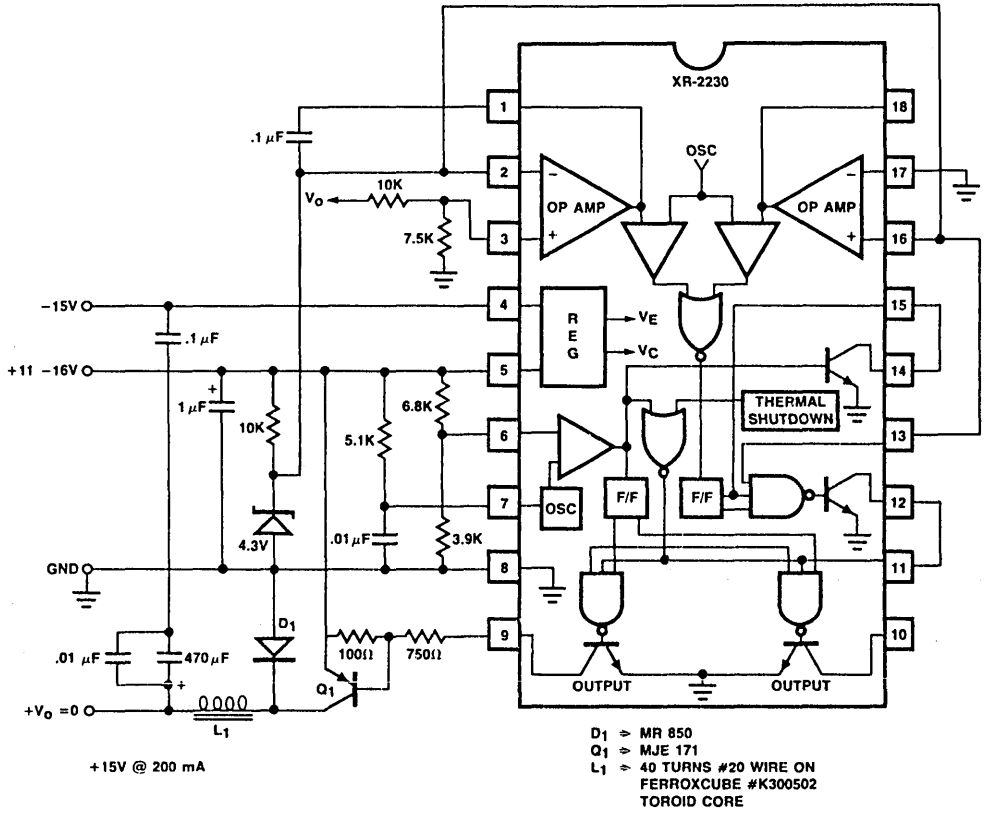


Figure 8. +10V Step-Down Regulator

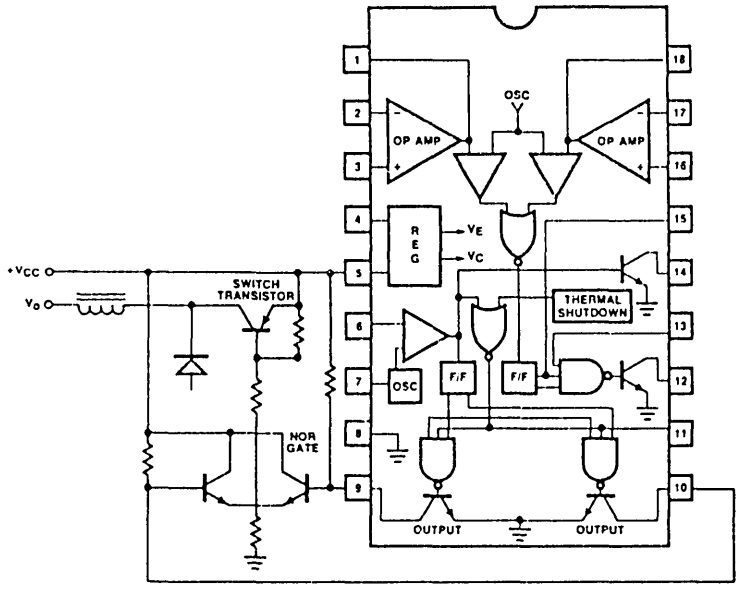


Figure 9. Outputs Nor'd for up to 90% Duty Cycle's

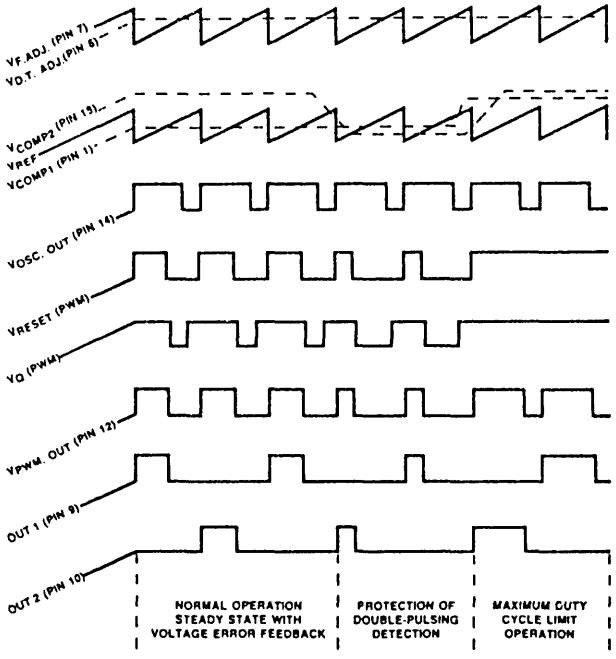


Figure 10. Timing Waveform Diagram