Long Range Timer

GENERAL DESCRIPTION

The XR-2242 is a monolithic timer/controller capable of producing ultra-long time delays from milliseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 8 bit binary counter and a control flip-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

Three output pins are provided on the device: the time base (RC) on Pin 8, 2 RC on Pin 2, and the counter output (128 RC) on Pin 3.

FEATURES

Timing from micro-seconds to days
Wide supply range: 4.5V to 15V
TTL and HCMOS compatible outputs
High accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

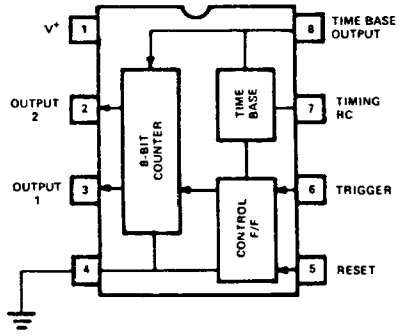
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature Range	−65° to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to +125°C
XR-2242CN	Ceramic	0°C to +70°C
XR-2242CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The timing cycle for the XR-2242 is initiated by applying a positive-going trigger pulse to Pin 6. The trigger input actuates the time-base oscillator, enables the counter section, and sets the output to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications the output terminal (Pin 3) is connected back to the reset terminal. In this manner, after 128 clock pulses are applied to the circuit, this output goes to "high" state and resets the circuit thus completing the timing cycle. Thus, subsequent to triggering, the output at Pin 3 will produce a total timing pulse of 128 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, R = 10 kΩ, C = 0.1 μF, unless otherwise noted.

PARAMETERS	XR-2242M MIN	XR-2242M TYP	XR-2242M MAX	XR-2242C MIN	XR-2242C TYP	XR-2242C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
TIME BASE SECTION								See Figure 3
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ 0°C ≤ T ≤ 70°C
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts
Max Frequency	100	130			130		kHz	R = 1 kΩ, C = C = 0.007 μF
Recommended Range of Timing Components								See Figure 5
Timing Resistor, R	0.001		10	0.001		5	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	Low-Leakage Capacitor Required.
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								Measured at Pin 5, $V_{TR} = 0$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.5	1.0			1.0		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 2 and 3
Rise Time		180			180		nsec.	$R_L = 3K\Omega$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} \leq 15V$

*Timing error solely introduced by XR-2242, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in first stage counter output at pin 2.

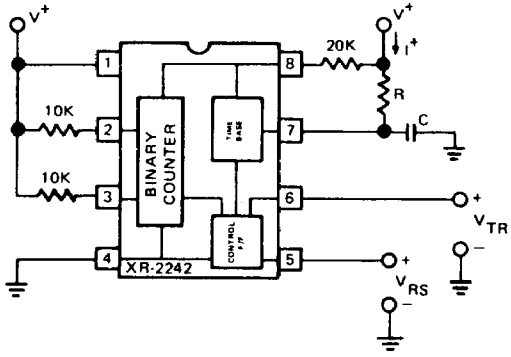


Figure 3. Generalized Test Circuit

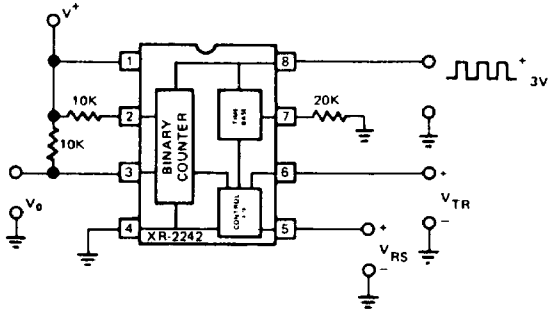


Figure 4. Test Circuit for Counter Section

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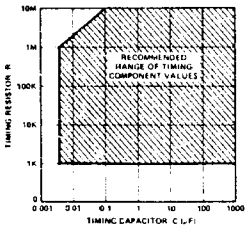


Figure 5. Recommended Range of Timing Component Values

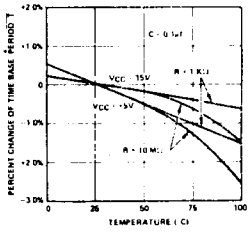


Figure 6. Temperature Drift of Time-Base Period, T

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 2 AND 3)

The binary counter outputs are buffered "open-collector" type stages. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 7.

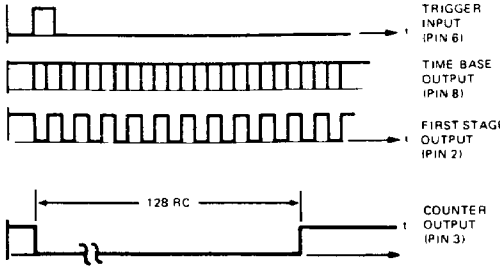


Figure 7. Timing Diagram of Output Waveforms

Basic circuit connection for timing applications is shown in Figure 8. Subsequent to a positive trigger pulse applied to pin 6, the timing output at pin 3 goes to a "low" state and will stay low for a total time duration T_0 = 128 RC, where R and C are the timing components connected to pin 7. If the switch S_1 is *open*, then the output at pin 3 would alternately change state every T_0 interval of time, and the circuit would operate in its "astable" mode. If the switch S_1 is *closed*, the circuit

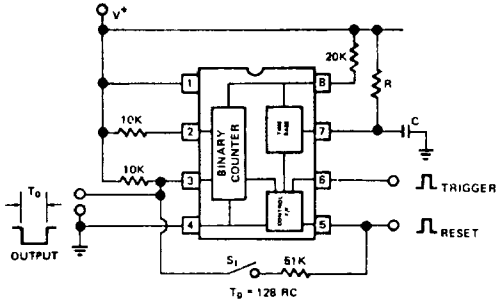


Figure 8. Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

will reset itself and complete its timing cycle after a time interval of T_0, when the output at pin 3 goes to a "high" state. This corresponds to the "monostable" mode of operation.

RESET AND TRIGGER INPUTS (PINS 5 AND 6)

The circuit is reset or triggered with positive-going control pulses applied to pins 5 and 6. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs, minimum trigger delay time and minimum re-trigger delay time are shown in Figures 9 and 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Note: In noisy operating environment, 0.01 μF capacitors to ground are recommended from reset and trigger terminals.

When power is applied with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

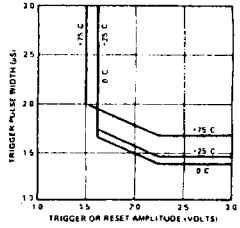


Figure 9. Minimum Trigger and Reset Pulse Widths at Pins 5 and 6

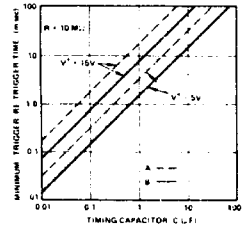


Figure 10. Trigger and Retrigger Delay Time

(A) Minimum Trigger Delay Time Subsequent to Application of Power

(B) Minimum Re-trigger Time, Subsequent to a Reset Input

TIMING TERMINAL (PIN 7)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 7 is an exponential ramp with a period T = 1.0 RC. A 1KΩ resistor to ground should be tied to this pin disable the time base.

TIME-BASE OUTPUT (PIN 8)

Time-base output is an open-collector type stage, as shown in Figure 1 and requires a 20 KΩ pull-up resistor to Pin 1 (V^+) for proper operation of the circuit. At reset state, the time-base output is at "high" stage. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 7.

ASTABLE OPERATION

The XR-2242 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 5) from the counter output (pin 3). Two typical circuit connections for this mode of operation are shown in Figures 11 and 12. In the circuit connection of Figure 11, the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 5, the circuit reverts back to its rest state. The circuit of Figure 11 is essentially the same as that of Figure 8, with the feedback switch S_1 open.

The circuit of Figure 12 is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

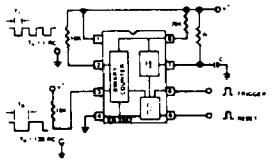
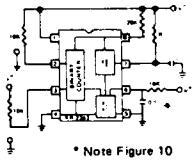


Figure 11. Astable Operation with External Trigger and Reset Controls



* Note Figure 10

Figure 12. Free-running Operation Self-Triggered When Power Supply is Turned On

OPERATION WITH EXTERNAL CLOCK

The XR-2242 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 8. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 7 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 μS.

CASCADED OPERATION:

a) Ultra-Long Delay Generation:

Ultra-long time delays, up to one-year duration, can be generated by cascading two XR-2242 timers as shown in Figure 13. In this configuration, the counter section of Unit 2 is cascaded with the counter output of Unit 1, to provide a total count of 32,640 clock cycles before the output (pin 3 of Unit 2) changes state. In the application circuit of Figure 13, the output (pin 3) of Unit 1 is directly connected to the time-base output (pin 8) of Unit 2, through a common pull-up resistor. In this manner, the counter section of Unit 2 is triggered every time the output of Unit 1 makes a *positive-going* transition. The time-base section of Unit 2 is disabled by connection pin 7 of Unit 2 to ground through a 1 KΩ resistor. The reset and trigger terminals of both units are connected together for common controls. If an additional XR-2242 were cascaded with Unit 2 of Figure 13, the total available time delay can be extended to (1.065) (10^9) RC. With an external RC = 0.1 sec, this would correspond to a time delay of 3.4 years.

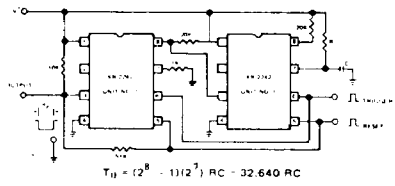


Figure 13. Cascaded Operation of Two XR-2242 Timer Circuits

b) Sequential Timing:

Two XR-2242 timers can be cascaded to produce sequential or delayed-timing pulses as shown in Figure 14. In this configuration, the second timer is triggered by the first timer, subsequent to the completion of its timing cycle. Thus, the triggering of Unit 2 is delayed by a time interval, T_1 (= 128 R_1C_1) corresponding to the timing cycle of Unit 1.

The output of Unit 2, which is normally at "high" state will stay high for a duration of T_1 = 128 R_1C_1, subsequent to the application of a trigger pulse; then go to a low state for a duration of T_2 = 128 R_2C_2 corresponding to the timing interval of Unit 2; and finally revert back to its rest state after the completion of the entire timing sequence.

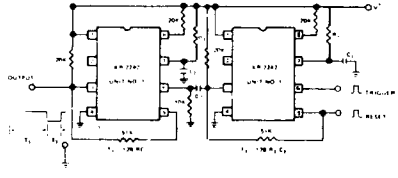
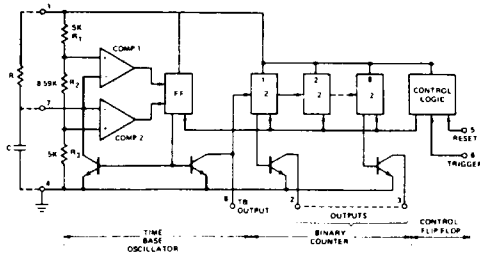


Figure 14. Sequential Timing Using Two XR-2242 Timer Circuits



EQUIVALENT SCHEMATIC DIAGRAM

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

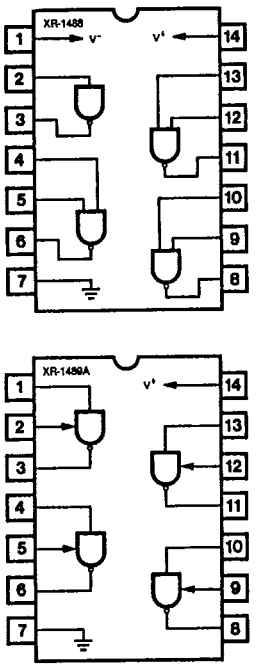
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.