Monolithic Timing Circuit

GENERAL DESCRIPTION

The XR-320 monolithic timing circuit is designed for use in instrumentation and digital communications equipment, and for a wide variety of industrial control and special testing applications. In many cases, this circuit provides a monolithic replacement for mechanical or electromechanical timing devices.

The XR-320 timing circuit generates precise timing pulses (or time delays) whose repetition rate (or length) is determined by an external timing resistor, R, and timing capacitor, C. The timing period is exactly equal to 2RC and can be continuously varied from 1 μsec to 1 hour. The circuits can be operated in a monostable or free-running (self-triggering) mode. They can be used for sequential timing and sweep generation, and also for pulse-position and pulse-width modulation.

The XR-320 integrated circuit is comprised of a stable internal bias reference, a precision current source, a voltage comparator, a flip-flop, a timing switch, and a pair of output logic drivers. The high current output at pin 12 can sink or source up to 100 milliamps of current.

FEATURES

Wide Timing Range: 1 μsec to 1 hour
High Accuracy: 1%
Excellent Temperature Stability: 100 ppm/°C
Wide Supply Voltage Range: 4.5V to 18V
Triggering with Positive or Negative-Going Pulses
Programmable
  Resistor Programming: 3 decades
  Capacitor Program: 9 decades
Logic Compatible Outputs
High Current Drive Capability: 100 mA

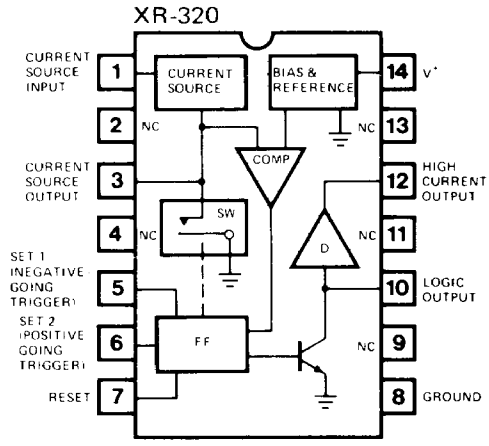
APPLICATIONS

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Internal Power Dissipation	750 mW
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-320P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-320 is an extremely versatile monolithic timer capable of delays ranging from 1 μsec to 1 hour. It works with both positive and negative triggering, and features both normally high and normally low outputs. An on board current source, programmable by an external resistor, changes the timing capacitor. This produces a true ramp function and allows accurate timing intervals equal to 2 RC.

Positive going triggering is applied to Pin 6; negative triggering is applied to Pin 5. After a trigger pulse is applied, the open collector output (Pin 10) will go high and the high current output (Pin 12) switches into the current sink mode. At timeout, the open collector pulls low, and can sink 10 mA; the high current output goes high and can source 100 mA. Utilizing the high current output requires a pull-up resistor from Pin 10 to $+V_{CC}$. The resistor must limit current to no more than 10 mA; 1 mA is sufficient. Timing is interrupted and the device is reset when Pin 7 is grounded. Astable operation is attained by tying the negative going (falling) trigger (Pin 5) to the timing capacitor (Pin 3). In this configuration, the device will automatically retrigger itself upon completion of the timing interval.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V ±5%, Test Circuit of Figure 2, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-320 MIN	XR-320 TYP	XR-320 MAX	UNITS	CONDITIONS
Supply Voltage	4.5		18	V_{dc}	
Quiescent Supply Current					
V+ = 5V		2.0	3.5	mA	
V+ = 12V		6.0	7.0	mA	
V+ = 18V		10.0	12.5	mA	
Timing Cycle Supply Current					
V+ = 5V		2.5	4.0	mA	
V+ = 12V		6.5	8.0	mA	
V+ = 18V		12.0	14.0	mA	
Timing Accuracy					
V+ = 5V		1.0	5.0	%	
V+ = 12V		1.0	5.0	%	
V+ = 18V		1.0	5.0	%	
Temperature Drift		100		ppm/°C	
Timing vs. Supply Voltage		0.1	0.5	%/V	
Stand-by Voltage (Pin 3)		0.7		V	
Comparator Threshold Voltage (Pin 3)					
V+ = 5V		2.4		V	
V+ = 12V	4.5	5.2	6.0	V	
V+ = 18V		8.4		V	
Current Source Input Voltage (Pin 1)					
V+ = 5V		4.15		V	
V+ = 12V	9.0	9.75	10.6	V	
V+ = 18V		16.15		V	
Trigger Voltage					
Set (Pin 5)		1.0	1.5	V	See Figure 11
Set 2 (Pin 6)	0.5	1.4		V	See Figure 12
Reset (Pin 7)		0.7	1.5	V	
Trigger Current					
Set 1 (Pin 5)		10		µA	
Set 2 (Pin 6)		60		µA	
Reset (Pin 7)		30		µA	
Output 1 (Pin 10) (Normally low)					
"Low" Voltage		0.1		V	
"High" Voltage	4.0	5.0		V	
Rise Time		140		nsec	
Fall Time		50		nsec	
Output 2 (Pin 12) (Normally high)					
"High" Voltage		10.4		V	I_{source} = 100 mA
"Low" Voltage		1.5		V	I_{sink} = 100 mA
Rise Time		100		nsec	
Fall Time		40		nsec	

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DEFINITIONS

Timing Accuracy: the timing error solely introduced by the XR-320, defined in per cent as:

$$100 \times \frac{\text{measured timing pulse length} - \text{2 RC based on actual component values}}{\text{2 RC based on actual component values}} \%$$

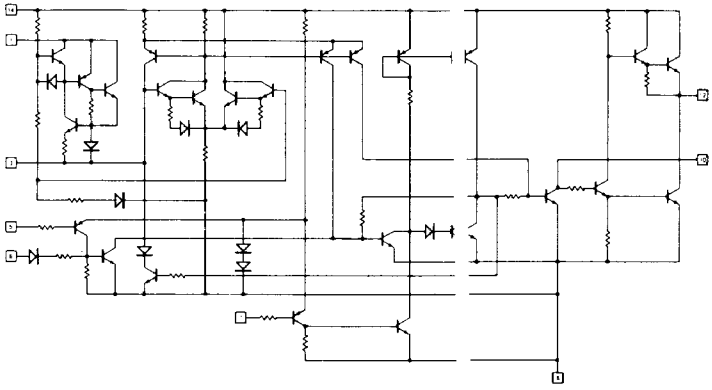
Timing vs Supply Voltage: the maximum timing drift over the power supply range of 5 to 18 volts referenced to 12 volt operation, defined in per cent per volt as:

$$\frac{100}{15} \times \frac{\text{max. timing pulse length over 5 to 18 volt supply} - \text{min. timing pulse length over 5 to 18 volt supply}}{\text{timing pulse length with 12 volt supply}} \%/V$$

Stand-by Voltage: the voltage between pin 3 and ground in reset condition.

Comparator Threshold Voltage (Pin 3): the voltage at which the internal comparator triggers the flip-flop and the timing capacitor discharges.

Trigger Voltage: the DC voltage level applied to each set or reset terminal which causes the output to change state.



EQUIVALENT SCHEMATIC DIAG RAM

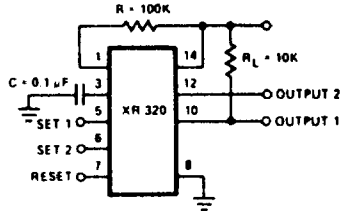


Figure 1. Test Circuit

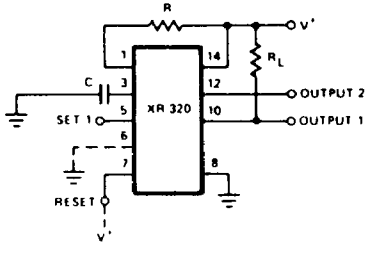


Figure 2. Monostable Operation, Negative Trigger

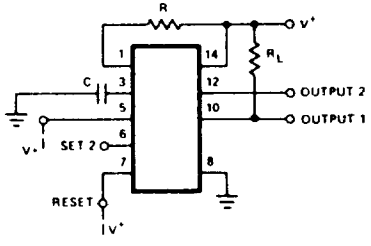


Figure 3. Monostable Operation, Positive Trigger

OPERA ıTING INSTRUCTIONS

Figure s 2 and 3 show typical connections for the XR-320. C ɔnly three external components are required for basic (ɔperation: the resistor R and capacitor C which determ ıine the time delay (2RC); and an external load resistor, R_L. The circuit provides two independent logic outputs ɔ: a medium current output (up to 10 mA) at pin 10, anc I a high current output (up to 100 mA) at pin 12. The ou tput at pin 10 is of the "bare-collector" type which r equires an external pull-up resistor, R_L, connected betw ɐeen this terminal and V^+ for proper circuit operation.

With no trigger pulse applied, the output at pin 10 is in a low stat ɐ near ground potential; and the output at pin 12 is in a h ıigh state, near V^+. The circuit is triggered by the appl ication of a negative-going pulse to pin 5 or a positive- going pulse to pin 6. At that instant, the output levels ch ɐange state such that pin 10 becomes high and pin 12 lc ɔw. The outputs will remain in this (switched) state unt il the delay time, T = 2RC, expires, at which time the (ɔutputs will return to their original state. In this mode of c ɔperation, the trigger input can be activated repeatedly ' without further influencing the time cycle, i.e., once the circuit is triggered it becomes immune to subsequent t riggering until the entire timing cycle is completed.

For reliabı 'e operation, the trigger pulse width must he shorter th an the output pulse width. Although many units will fu ınction when this rule is not observed, proper operation (ɔannot be guaranteed.

Figure 4 sl ıows the waveforms at various circuit locations for a r ıegative-going trigger applied to pin 5. A similar set of waveforms is displayed in Figure 5 for a positive-goi ng pulse applied to pin 6. The timing cycle can be resı ɐt at any time by simply grounding pin 7.

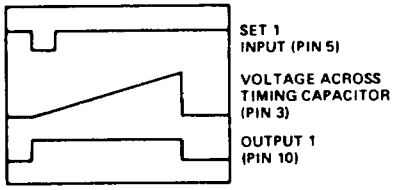


Figure 4. Waveforms for Negative-Going Trigger

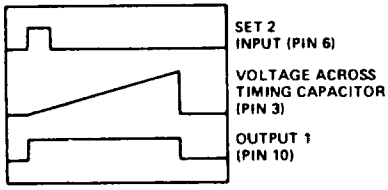


Figure 5. Waveforms for Positive-Going Trigger

DESCRIPTION OF CIRCUIT CONTROLS

TIMING RESISTOR (PIN 1)

Timing resistor, R, is connected between pin 1 and V+, pin 14. For maximum timing accuracy, R should be in the range 6 kΩ ≤ R ≤ 1 MΩ. See Figure 6 for the minimum and maximum values for R for various supply voltages.

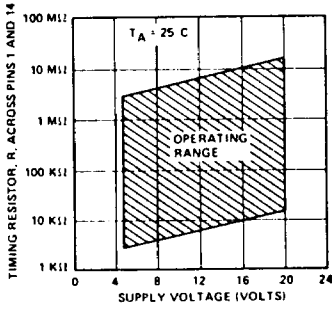


Figure 6. Operating Range as a Function of Timing Resistor and Supply Voltage

TIMING CAPACITOR (PIN 3)

Timing capacitor, C, is connected between pin 3 and ground. The time delay, T, is equal to 2RC in seconds. NOTE: A timing error can result due to the leakage current of the timing capacitor. When a capacitor with a relatively low insulation resistance (e.g. a high-valued electrolytic) is used as the timing capacitor, the resulting delay time will be much longer than 2RC because of the associated leakage current.

SET 1 — NEGATIVE TRIGGER (PIN 5)

A negative-going pulse applied to pin 5 will cause the outputs to change state. Output 1, pin 10, which is normally low will go high, Output 2, pin 12, which is normally high will go low. See Figure 11 for additional details. When not used, pin 5 should be connected to V+ to avoid false triggering.

By grounding or applying a negative pulse to the reset (Pin 7), the timing cycle is automatically interrupted and the outputs return to their original state. When the reset function is not in use, it is recommended that it be connected to V+ to avoid any possibility of false resetting.

SET 2 — POSITIVE TRIGGER (PIN 6)

A positive-going pulse applied to pin 6 will cause the outputs to change state. The normally low output at pin 10 will go high, and the normally high output at pin 12 will go low. See Figure 12 for additional details. When not used, pin 6 should be grounded to avoid false triggering.

ADDITIONAL APPLICATIONS

FREE-RUNNING MODE

By shorting pins 3 and 5, the XR-320 will operate in a "free-running" or self-triggering mode. In this mode of operation, the circuit functions as a stable clock pulse generator with a repetition rate of approximately 1/(2RC). The circuit connection and free-running frequency in this application are shown in Figure 7. Note that one cycle is not precisely equal to 2RC because of capacitor discharge time. Typical waveforms for self-triggered operation are shown in Figure 8.

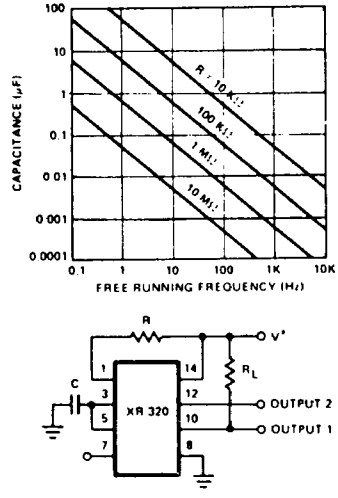


Figure 7. Free-Running Operation

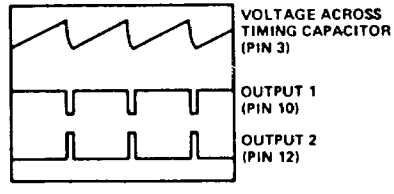


Figure 8. Waveforms for Self-Triggered Operation

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SWEEP GENERATION

In self-triggered operation, the waveform across the timing capacitor (at pin 3) is a linear ramp as shown in Figure 8. The waveform at pin 3 can be used as a highly linear sweep voltage with a total nonlinearity of less than 1%.

PULSE-WIDTH MODULATION

For this application, the XR-320 should be connected as shown in Figure 9.

The modulation input is applied to pin 1 through coupling capacitor, C_C. The input signal modulates the current through the timing resistor, R, and, in turn, changes the width of the output timing pulses. The resistor R_M, in series with the signal source, is used to control the amount of modulation for a given input signal level.

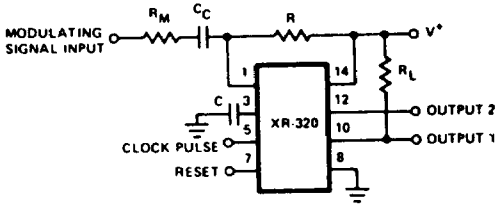


Figure 9. Circuit Connection for Pulse-width Modulation

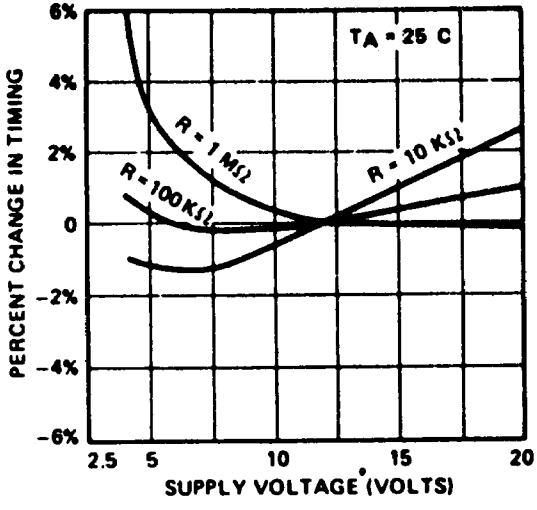


Figure 10. Change in Timing vs. Supply Voltage

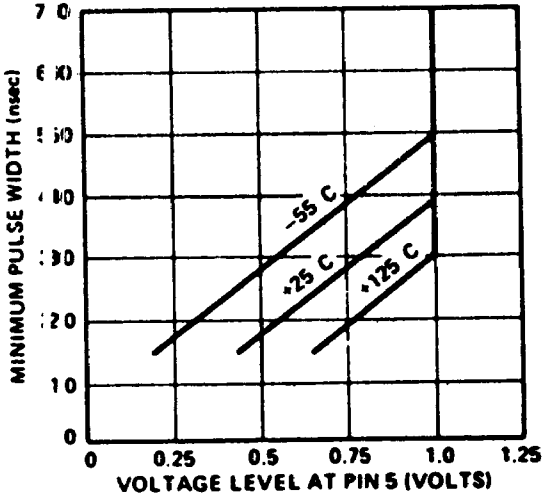


Figure 11. Minimum Pulse Width for Triggering at Pin 5

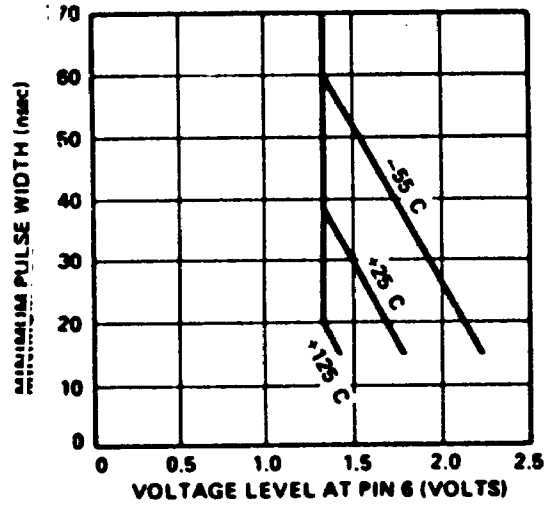


Figure 12. Minimum Pulse Width for Triggering at Pin 6

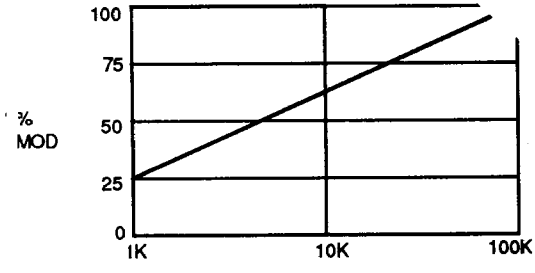


Figure 13. % MOD vs R_M

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

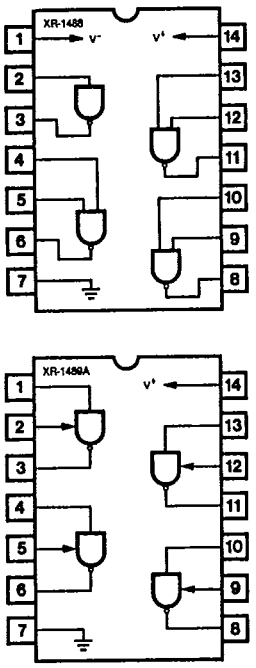
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.