Floppy Disk Read/Write

GENERAL DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a single 28 Pin monolithic solution for double-sided floppy disk drives. The device is compatible with 8", 5¼", and 3½" drives, providing all read and write functions and offering improved performance over industry standard dual chip sets, with lower external parts count. Schmitt trigger inputs and separate analog and power grounds aid noise and crosstalk immunity. Both pre and post amplifiers, plus an AGC, allow reliable operation with input signals ranging from 0.5 mV to 25mV.

The XR-3448 is available in standard or small outline 28 Pin packages. Control, write inputs, and read outputs are TTL compatible. The device operates from +12 V and +5 V supplies. The pinout is specially designed for similarity to the SSI-570 Read/Write, and in many applications, the XR-3448 acts as an improved version of that device.

FEATURES

All Read/Write Functions on a Single Chip
Schmitt Trigger Inputs for Noise Immunity
TTL Compatible
Power Up and Low Voltage Inhibit
Low Peak Shift – No Trimming Necessary
On Board AGC
Wide Read Dynamic Range
Low External Parts Count
All Delays RC Programmable
Separate Power and Signal Ground
Tunnel or Straddle Erase Compatibility

APPLICATIONS

Single or Dual Head Floppy Disk Drive Systems

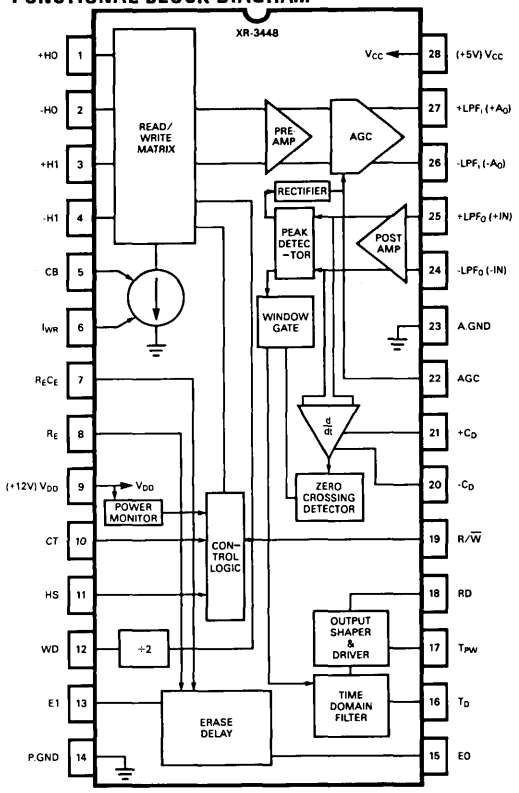
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
Pin 28 (5 V)	7 V
Pin 9 (12 V)	15 V
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	150°C
Power Dissipation (28 Pin DIL)	800 mW
Derate Above 25°C	6.5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3448CP	Plastic	0°C to +70°C
XR-3448CN	Ceramic	0°C to +70°C
XR-3448MD	Small Outline	0°C to +70°C
XR-3448CQ	Quad Surface Mount	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a high performance single chip solution for all standard floppy disk drives. TTL compatible control and interface levels, and +12 V and +5 V operation allows easy system implementation with standard components. An on-board voltage monitor, with hysteresis, supervises device voltage and disables all operation during power up and down. Dual grounds, one for the digital levels, the other for low level signals, and the use of ECL processing logic eliminates digital crosstalk and jittering coupled back into the read heads.

Read error reduction performance is greatly enhanced by the window gating logic that qualifies data pules and eliminates errors generated by noise or discontinuities during shouldering. A time domain filter further reduces errors caused by nonlinearities about data peaks. Together, these systems allow improved performance margins over simpler floppy disk read devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 430\Omega$, $R_{ED} = 10k$, $C_E = 0.05\mu F$, $R_{EH} = 10k\Omega$, $C_D = 100$ pF, $R_D = 200\Omega$, $C_{TD} = 100$ pF, $R_{TD} = 10k\Omega$, $C_{PW} = 330$ pF, $R_{PW} = 10k\Omega$, Output Load = $1k\Omega$ to V_{CC}, V_{IN} (preamp) = DC coupled 10 mVp-p sine wave, V_{IN} (postamp) = AC coupled 200 mVp-p sine wave, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	Recommended Power Supply Voltage	4.5	5	5.5	V	
V_{DD}	Recommended Power Supply Voltage	10.8	12	13.2	V	
I_{CC}	Power Supply Current (5 V)		30 33	35 40	mA mA	Read Mode Write Mode
I_{DD}	Power Supply Current (12 V)		17 22	22 25	mA mA	Read Mode Write Mode, $I_E = 0$
POWER SUPPLY MONITOR						
V_{CC}	Power Up Threshold Power Down Threshold	3.0 2.3	3.5 2.6	4.0 3.0	V V	
V_{DD}	Power Up Threshold Power Down Threshold	7.9 6.5	8.6 7.5	9.2 8.0	V V	
LOGIC INPUTS						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current			−400	μA	$V_{IL} = 0.4$ V
I_{IH}	Input High Current			20	μA	$V_{IH} = 2.4$ V
DATA OUTPUT						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 4$ mA
V_{OH}	Output High Voltage	2.7			V	$I_{OH} = 400\mu A$
T_{PW}	Pulse Width Accuracy	−20	±5	20	%	$R_{PW} = 10k\Omega$ $C_{PW} = 330$ pF
R_{PW}	Recommended Resistor Range	5		25	kΩ	
C_{PW}	Recommended Capacitor Range	100		620	pF	
TIMERS						
	Erase Delay Accuracy Erase Hold Accuracy	−15 −15	±5 ±5	15 15	% %	Error from $T_{ED} = R_{ED} C_E$ Error from $T_{EH} = (R_{ED}+R_{EH})C_E$
R_{ED}/R_{EH}	Recommended Resistor Value	5		30	kΩ	
C_E	Recommended Capacitor Value	0.01		0.068	μF	
	Time Domain Filter Accuracy	−15	±5	15	%	$R_{TD} = 10k$, $C_{TD} = 100$ pF
R_{TD}	Recommended Resistor Value	1		15	kΩ	
C_{TD}	Recommended Capacitor Value	51		330	pF	

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 430\Omega$, $R_{ED} = 10k$, $C_E = 0.05\mu F$, $R_{EH} = 10k\Omega$, $C_D = 100$ pF, $R_D = 200\Omega$, $C_{TD} = 100$ pF, $R_{TD} = 10k\Omega$, $C_{PW} = 330$ pF, $R_{PW} = 10k\Omega$, Output Load = $1k\Omega$ to V_{CC}, V_{IN} (preamp) = DC coupled 10 mVp-p sine wave, V_{IN} (postamp) = AC coupled 200 mVp-p sine wave, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
READ MODE						
PREAMP						
A_V	Differential Voltage Gain		300		V/V	f = 250 kHz, V_{CT} = 1.5 V Pin 22 Shorted to Ground
BW	Bandwidth	5	15		MHz	−3 dB Point
	Gain Flatness	−1.0		1.0	dB	f = 0 to 1.5 MHz
Z_{IN}	Differential Input Impedance	10	30		kΩ	f = 250 kHz
AGC						
	Dynamic Range		12		dB	For 3 dB Output Variation
R_{AGC}	Recommended Resistor Range	3.3	10	25	kΩ	
C_{AGC}	Recommended Capacitor Range	0.01	0.1	1	μF	
POSTAMPLIFIER & DIFFERENTIATOR						
A_V	Differential Voltage Gain	4	4.5	6	V/V	f = 250 kHz
BW	Bandwidth	5	15		MHz	−3 dB Point
	Gain Flatness	−1.0		1.0	dB	
WRITE MODE						
V_{CT}	Center Tap Output ON Voltage	V_{DD} −2.5	V_{DD} −2	V_{DD} −1.3	V	$R_E = 150\Omega$
V_E	Erase Output ON Voltage		0.5	1.0	V	$R_E = 150\Omega$
	Unselected Head Erase Leakage			100	μA	V_{EO}, V_{E1} = 12 V, $R_E = 150\Omega$
I_W	Recommended Write Current Range	3		10	mA	$R_W = 680\Omega$ to 180Ω
	Write Current Accuracy	−5	±0.2	5	%	CB = 0
	Write Current Unbalance	−1	±0.01	1	%	Head 0 to Head 1
CB	Current Boost Factor	1.25	1.30	1.35		CB = 1

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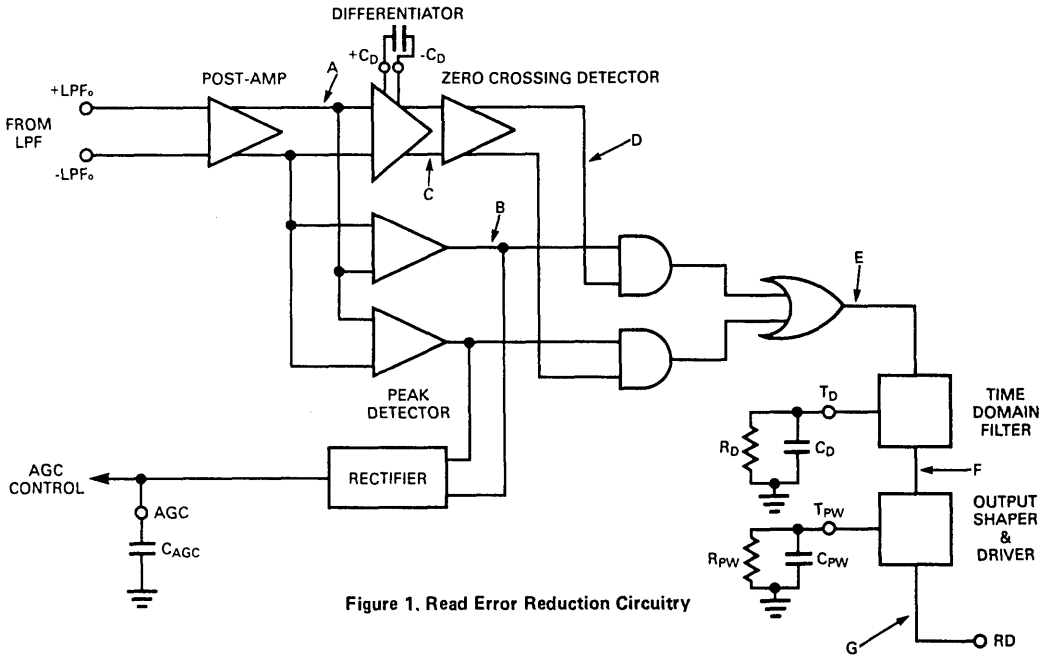


Figure 1. Read Error Reduction Circuitry

PRINCIPLES OF OPERATION

Write Mode

In the write mode, R/W (Pin 19) is held low. Data is applied to the input Schmitt trigger (Pin 12), goes through a toggle flip-flop, and into the write matrix. The proper magnetic head is selected by the matrix, depending on the level at HS (Pin 11). Both head center taps are connected to CT (Pin 10) which sources the current sunk by the proper transistor (Pin 1, 2, 3, or 4).

Write current is controlled by the resistor, R_{IW}, on I_{WR} (Pin 6); when CB (Pin 5) is pulled high, write current is boosted 30%. Tunnel erase delay and hold times are set by a capacitor and two resistors on $R_E C_E$ (Pin 7) and R_E (Pin 8). Straddle erase heads are accommodated by eliminating C_E.

Read Mode

Pulling R/W high selects data readback mode. The dual error reduction system employed by the XR-3448 greatly diminishes read error rates. The read signal is routed through a diode multiplexer into a low noise preamplifier. This output is routed to an automatic gain control (AGC) circuit which lowers peak shift: for most systems, external peak shift adjustment is unnecessary across an input dynamic range from 500 μV to 25 mV. The AGC compresses a 20 dB input variation down to a 5 dB output range. AGC response time is affected by the RC at the AGC pin (Pin 22). The compressed signal is applied to a low pass filter (LPF) which attenuates high frequency noise. A post-amplifier compensates for LPF insertion losses and drives both the Peak Detector and Active Differentiator (see Figure 1) with waveform A, shown in Figure 2. The Peak Detector is a comparator-like device that produces output whenever data input is above a threshold level (see Figure 2B). This output is employed as the Gating Logic enable. Rectified peak detector output is returned to the AGC as the control signal.

The Active Differentiator computes the first derivative of the input signal, producing waveform C of Figure 2. Zero Crossing Detector output toggles (Figure 2D) at zero crossings, which correspond to data peaks – one crossing per datum. Hysteresis in the detector aids noise immunity. The Window Gating Logic effectively provides an AND function: output (Figure 2E) appears only when (1) the Zero Crossing Detector sees a crossing, and (2) the Peak Detector sees a data peak. Spurious signals, therefore, do not cause output.

Noise and system nonlinearities however, occasionally produce closely spaced false outputs. Further error reduction is provided by a time domain filter following the gating logic. Adjacent pulses, occurring before the minimum time delay set by a resistor and capacitor on T_d (Pin 16), are ignored (Figure 2E). Since nonlinearities occur in pairs, a valid data pulse mixed with two invalid pulses still provides one meaningful output – exactly as desired. Output pulse width is determined by an RC on T_{pw} (Pin 17), which feeds the output driver with TTL level constant width pulses. The data appears at RD (Pin 18), as shown in Figure 2G.

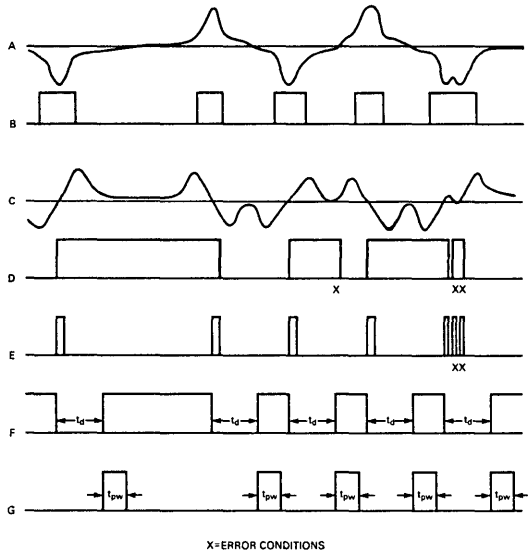


Figure 2. Read Waveforms

APPLICATIONS INFORMATION

The applications circuit of Figure 4 may be customized to match the available magnetic head, interface pulse widths, write currents, AGC times, data transfer rates, etc. Table 1 gives recommended component values and ranges.

DESIGN INSTRUCTIONS

AGC:

The AGC time constant is set by the resistor and capacitor on Pin 22. The time must be short enough that initial data does not overdrive the amplifiers, yet long enough that noise and offset levels between data bits do not register as output. Delay time is determined by:

$$T = R_{AGC}\, C_{AGC}$$

For most applications at 500 kB data rate, a time of 1 ms, using R_{AGC} = 10 kΩ and C_{AGC} = 0.1μF.

LPF

The LPF is strongly dependent on head type and other system and circuit considerations. Constant gain and phase to f = (baud rate/2) is tantamount to proper performance. Avoiding driver saturation requires that the filter current is less than 2.8 mA. The postamplifier inputs are DC biased internally. Blocking capacitors should isolate the DC level from the AGC output; optimum transient response characteristics occur when the capacitors are before the filter, directly after the AGC output.

Active Differentiator

The differentiation function requires a capacitor network across Pins 20 and 21. The dominant component, capacitor C_D, is optimum when its current slew rate is maximized. This occurs when

$$C_D = \frac{1\ \text{mA}}{(A_{VD})\,(E_P)\,(\omega_{max})\,(A_F)}$$

Where A_{VD} is the gain of the amplifier
E_P is the maximum expected input voltage
ω_{max} is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

When C_D is the only component employed, a pole is produced by C_D and the effective output resistance of Q1 and Q2 (See Figure 3), R_O. This pole lies at

$$\omega_p = \frac{1}{2R_O\, C_D}$$

where R_O is typically 40Ω.

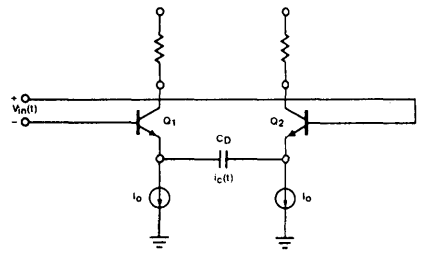


Figure 3. Simplified Active Differentiator Section

Perfect differentiation requires a phase shift of 90°. This suggests ω_p should approach ∞ since

$$\theta = \arctan\,(\omega_p/\omega_O)$$

where ω_O = operating frequency.

A large ω_p, however, produces a large noise bandwidth; a reasonable compromise sets ω_p at 10 ω_{max}. This produces a phase shift of approximately 84° and limits the noise bandwidth. The design criteria is now given by

$$\omega_{max} = \frac{1}{20(R_O C_D)}$$

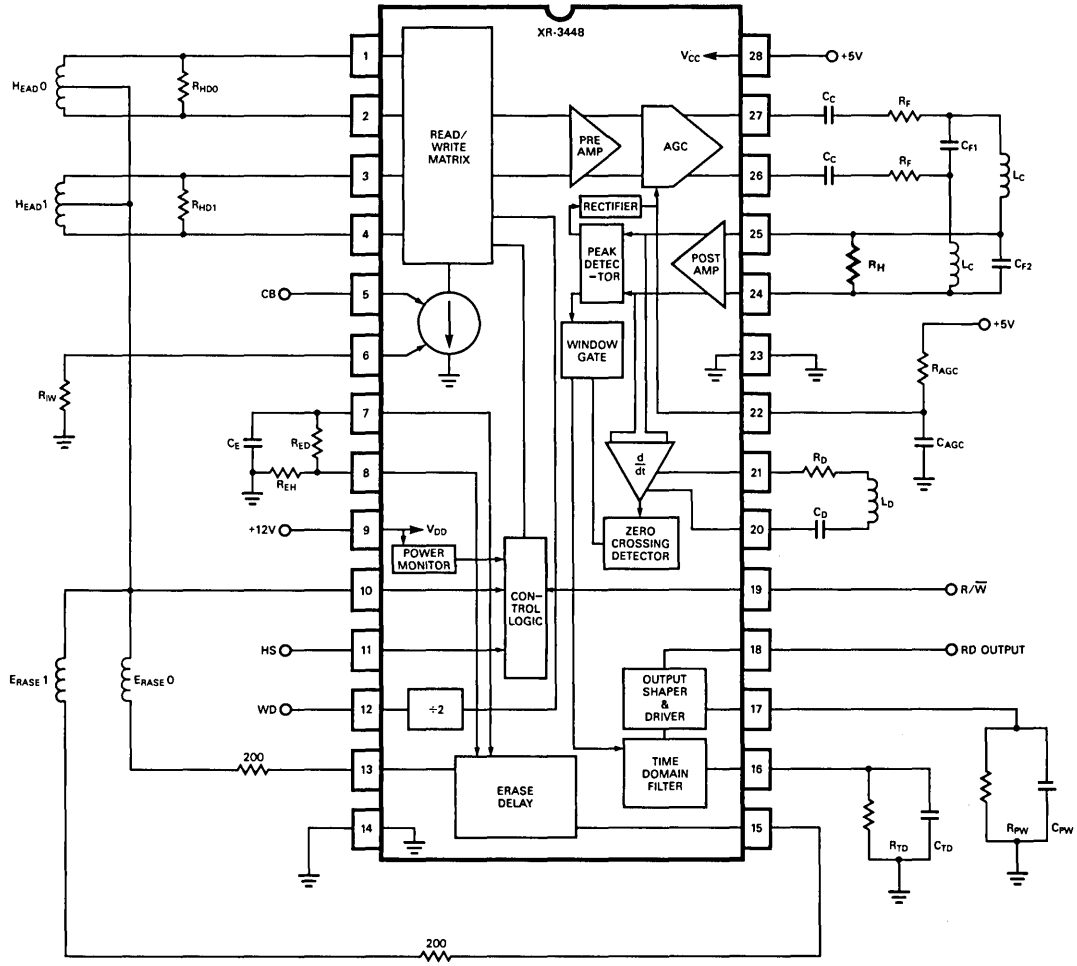


Figure 4. XR-3448 Typical Application

For maximum gain applications delete R_{AGC} and C_{AGC} and ground pin 22.

TABLE I

TYPICAL COMPONENT VALUES

Component	Typical Value	Recommended Range	Component	Typical Value
R_{IW}	560Ω	180 - 680Ω	R_H	1.5kΩ
R_{E0}, R_{E1}	280Ω	100 - 680Ω	C_C	.022μF
R_{ED}, R_{EH}	10kΩ	5k - 30kΩ	R_F	470Ω
C_E	.047μF	0.01 - 0.068μF	C_{F1}	.001μF
R_{PW}	10k	5k - 25kΩ	C_{F2}	470pF
C_{PW}	100 pF	51 pF - 1000 pF	L_C	680μH
C_{TD}	100pF	51 pF - 330 pF	R_D	200Ω
R_{AGC}	6.81k	3.3k - 25kΩ	C_D	1000pF
C_{AGC}	1μF	.01μF - 1μF	L_D	56μH

Often, R_O is too low, creating a pole at a frequency greater than 10 ω_{max}. In this case, a resistor R_D, in series with C_D gives the equation:

$$\omega_{max} = \frac{1}{20(R_D + R_O)\, C_D}$$

This allows a degree of flexibility in selecting the noise bandwidth, as shown in Figure 5.

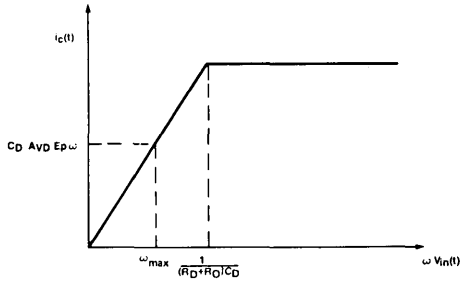


Figure 5: Differentiator Response for C_D and R

A series inductor, L_D, will further reduce noise bandwidth by introducing another pole. When selected for 10 ω_{max}, as shown in Figure 6, L_D is given by

$$L_D = \frac{1}{100(\omega_{max})^2 C_D}$$

The damping ratio, δ, should be between 0.3 and 1 where

$$\delta = \frac{(R_O + 0.5\, R_D)\, C_D}{2\sqrt{L_D C_D}}$$

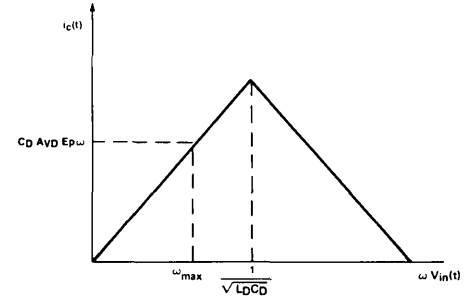


Figure 6: Differentiator Response with R_D, C_D, and L.

Peak Shift Adjustment

For the majority of applications, the inherent low peak shift of the XR-3448 requires no improvement. However, an additional trim can be implemented if necessary. The arrangement shown in Figure 7 will eliminate the current imbalance in the differentiator and reduce comparator offset voltages. The potentiometer is adjusted for symmetrical output with sinusoidal input.

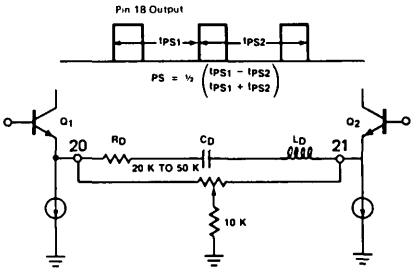


Figure 7. Nulling Network to Minimize Peak Shift (PS)

Time Doman Filter

Filter time, t, is determined by the maximum period of expected distortion, Δt, and the maximum operating frequency, f_{max}.

Determination of R and C involves the following considerations:

$$t = 0.215\, R_{TD}\, C_{TD} + 200\ nS$$

where R_{TD}: 1 kΩ ≤ R ≤ 15kΩ, and C_{TD}: 51pF ≤ C ≤ 330 pF

Output Shaper

The output shaper determines the pulse width of the data signal. Resistor and capacitor ranges follow the same guidelines as presented in the Time Domain Filter above. Pulse width is:

$$t = 0.215\, R_{PW}\, C_{PW} + 120\ nS$$

where R_{PW}: 5kΩ ≤ R ≤ 30kΩ, and C_{TD}: 100 pF ≤ C ≤ 620 pF.

Damping Resistors

Head damping resistors should be optimized for writing. Their value depends entirely on the head employed and the desired damping coefficient.

Write Current

A current mirror uses the internal voltage reference and a resistor from Pin 6 to ground for write current programming. The resistor value is determined by

$$R_{IW}\ (k\Omega) = \frac{2.35V}{I_{WR}\ (mA)}$$

Write current increases by 30% over this value when CB (Pin 5) is held at a high TTL logic level.

Additional write current steps, if necessary, are implemented as shown in Figure 8. In Figure 8(a), TTL logic lines and reistors vary current output. Figure 8(b) shows the resistive ladder method, with transistors selectively switching resistors. The varying resistance on Pin 6 causes varying write currents.

$$I_W\ (mA) = \frac{2.35V}{R_{IW}\ (total)\ (k\Omega)}$$

These method work for any number of control lines. CB (Pin 5) is still active, and will multiply current by 1.3 whenever held high.

Write Erase Resistors

Erase current is limited by series resistors from E0 and E1 to the respective erase heads. Resistor values may be approximated by:

$$R_E = \frac{V_{CT} - V_{SAT}}{I_{ERASE}}$$

For typical I_{ERASE} = 50 mA, V_{CT} = 10.5 V, and V_{SAT} = 500 mV, R_E = 200 Ω.

Erase Delay Time

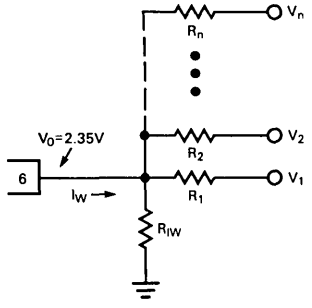
Tunnel erase delays are provided by the XR-3448. Both Erase Delay Time, T_{ED}, which controls erase initiation and Erase Hold Time, T_{EH}, which delays erase release, are controlled by a simple RC circuit. In the configuration of Figure 1, T_{ED} is calculated as:

$$T_{ED} = R_{ED}\ C_E$$

and T_{EH} is determined by

$$T_{EH} = (R_{ED} + R_{EH})\ C_E$$

Suggested resistor values range between 5kΩ and 30kΩ. C_E should range from 0.01μF to 0.068μF.

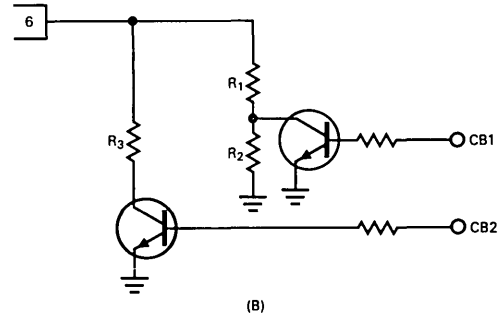


$$I_W = \frac{V_0}{R_{IW}} - \left(\frac{V_1 - V_0}{R_1}\right) - \left(\frac{V_2 - V_0}{R_2}\right) - \cdots - \left(\frac{V_n - V_0}{R_n}\right)$$

WHERE V_0 = 2.35V AND V_1 THROUGH V_n ARE LOGIC LEVELS.

(A)

CB1	CB2	R_{IW} (eff)
0	0	$R_1 + R_2$
0	1	$R_3 // R_1 + R_2$
1	0	R_1
1	1	$R_3 // R_1$



(B)

Figure 8. Obtaining Additional Write Current Steps: (A) TTL Lines and Resistors Increase and Decrease I_W. (B) Transistors Switch Resistors to Increase I_W.