Floppy Disk Read Amplifier

GENERAL DESCRIPTION

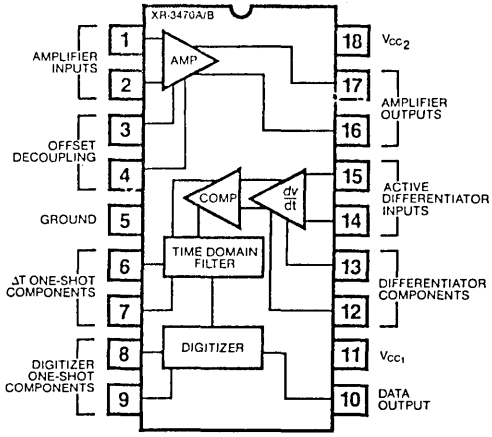
The XR-3470A/3470B is read amplifier system designed primarily for use in a floppy disk drive system. It is designed to perform the complete readback function, by accepting the readback signal from a magnetic head and converting it into digital output pulses. To perform this function, the circuit contains a high-frequency amplifier, an active differentiator, a zero-crossing detector, and a time domain filter.

The XR-3470A/3470B is suited for systems with data transfer rates up to 3 megabaud. High input sensitivity allows operation with signal levels as low as 1.4 mV pp, which gives it the flexibility to be used for single or double density floppy disk systems.

The XR-3470A/3470B offers improvements (over the standard 3470) of lower peak shift and power part-to-part input amplifier gain variations.

The XR-3470A/3470B, available in an 18 Pin DIP, is powered by +5 and +12 volt power supplies.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete Floppy Disk Read Amplifier	
Low Input Voltage detection	1.4 mV pp
Low Peak Shift 3470A	2% Max
3470B	4% Max
Low Amplifier Gain Variation	100 V/V Min
	130 V/V Max
High Amplifier Frequency Response	10 MHz, Min.

APPLICATIONS

Single/Double Density Floppy Disk Read Amplifier
Magnetic Read Amplifier

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (Pin 11)	7 V dc
Power Supply Voltage (Pin 18)	16 V dc
Input Voltage (Pins 1 and 2)	−2V to +7 V dc
Output Voltage (Pin 10)	−2V to +7 V dc
Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Operating Junction Temperature	150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3470ACN	Ceramic	0°C to +70°C
XR-3470ACP	Plastic	0°C to +70°C
XR-3470BCN	Ceramic	0°C to +70°C
XR-3470BCP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-3470A/3470B contains four internal signal blocks. Their functions are as follows: **Input Amplifier** — This section receives an input directly from the magnetic head. It provides a nominal gain of 110 V/V, with gain select pins to reduce gain or tailor it for ac response. The amplifier has differential inputs and outputs. **Active Differentiator** — This circuit differentiates the signal from the amplifier which causes a zero-crossing for each peak of the readback signal. The time constant and response of this section is externally set. **Zero-Crossing Detector** — This function is performed by a voltage comparator. It produces complementary outputs for the internal digital section. **Digital Section** — This section consists of 2 one-shots and other control circuitry. The one-shots are used to prevent false outputs, and set the output pulse width.

ELECTRICAL CHARACTERISTICS

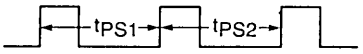
Test Conditions: T_A = 0°C to 70°C; V_{CC1} = 4.75V to 5.25V; V_{CC2} = 10V to 14V; unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GAIN AMPLIFIER SECTION						
A_{VD}	Differential Voltage Gain	100	110	130	V/V	f = 200 kHz, V_{ID} = 5 mV (RMS)
I_{IB}	Input Bias Current	—	−10	−25	μA	
V_{ICM}	Input Common Mode Range Linear Operation	−0.1	—	1.5	V	5% max THD
V_{ID}	Differential Input Voltage Linear Operation	—	—	25	mV pp	5% max THD
V_{OD}	Output Voltage Swing Differential	3.0	4.0	—	V pp	
I_O	Output Source Current, Toggled	—	8.0	—	mA	
I_{OS}	Output Sink Current	2.8	4	—	mA	Pins 16 and 17
R_I	Small Signal Input Resistance	100	250	—	kΩ	T_A = 25°C
R_O	Small Signal Output Resistance Single-Ended	—	15	—	Ω	T_A = 25°C, V_{CC1} = 5V V_{CC2} = 12V
BW	Bandwidth, −3 dB	10.0	—	—	MHz	T_A = 25°C, V_{CC1} = 5V V_{ID} = 2 mV (RMS), V_{CC2} = 12V
CMRR	Common Mode Rejection Ratio	50	—	—	dB	T_A = 25°C, f = 100 kHz A_{VD} = 40 dB, V_{CC1} = 5V V_{IN} = 200 mV pp, V_{CC2} = 12V
PSSR1	V_{CC1} Supply Rejection Ratio	50	—	—	dB	T_A = 25°C, A_{VD} = 40 dB 4.75 < V_{CC1} < 5.25, V_{CC2} = 12V
PSSR2	V_{CC2} Supply Rejection Ratio	60	—	—	dB	T_A = 25°C, A_{VD} = 40 dB 10 < V_{CC2} < 14V, V_{CC1} = 5V
V_{DO}	Differential Output Offset	—	—	0.4	V	T_A = 25°C, V_{ID} = V_{IN} = 0V
V_{CO}	Common Mode Output Offset	—	3.0	—	V	V_{ID} = V_{IN} = 0V Differential and Common Mode
e_n	Differential Noise Voltage Referred to Input	—	15	—	μV (RMS)	BW = 10 Hz to 1.0 MHz T_A = 25°C
ACTIVE DIFFERENTIATOR SECTION						
I_{OD}	Differentiator Output Sink Current	1.0	1.4	—	mA	Pins 12 and 13, V_{OD} = V_{CC1}
PS	Peak Shift 3470A	—	—	2.0	%	f = 250 kHz, V_{ID} = 1V pp
	3470B	—	—	4.0	%	I_{CAP} = 500 μA V_{CC1} = 5V, V_{CC2} = 12V See Figure 2
R_{ID}	Differentiator Input Resistance Differential	—	30	—	kΩ	T_A = 25°C
R_{OD}	Differentiator Output Resistance Differential	—	40	—	Ω	T_A = 25°C
DIGITAL SECTION						
V_{OH}	Output Voltage High Logic Level	2.7	—	—	V	Pin 10, V_{CC1} = 4.75V I_{OH} = −0.4 mA, V_{CC2} = 12V
V_{OL}	Output Voltage Low Logic Level	—	—	0.5	V	Pin 10, V_{CC1} = 4.75V I_{OL} = 8.0 mA, V_{CC2} = 12V
t_{TLH}	Output Rise Time	—	—	20	ns	Pin 10
t_{THL}	Output Fall Time	—	—	25	ns	Pin 10
$t_{1A,B}$	Timing Range Mono #1	500		4000	ns	t_{1A},t_{1B}
E_{t1}	Timing Accuracy Mono #1	85	—	115	%	R_1 = 6.4 kΩ, C_1 = 200 pF (Note 1)
t_2	Timing Range Mono #2	150	—	1000	ns	
E_{t2}	Timing Accuracy Mono #2	85	—	115	%	R_2 = 1.6 kΩ, C_2 = 200 pF (Note 2)
I_{CC1}	V_{CC1}, Power Supply Current	—	25	40	mA	
I_{CC2}	V_{CC2}, Power Supply Current	—	3	10	mA	

1. Accuracy guaranteed for R_1 and C_1 in range
   1.5 kΩ < R_1 < 10 kΩ
   150 pF < C_1 < 680 pF

2. Accuracy guaranteed for R_2 and C_2 in range
   1.5 kΩ < R_2 < 10 kΩ
   100 pF < C_2 < 800 pF

$$PS = \frac{1}{2}\left(\frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}}\right) \text{ at Pin 10}$$



I_{CAP} = current into Pin 12

Figure 2.

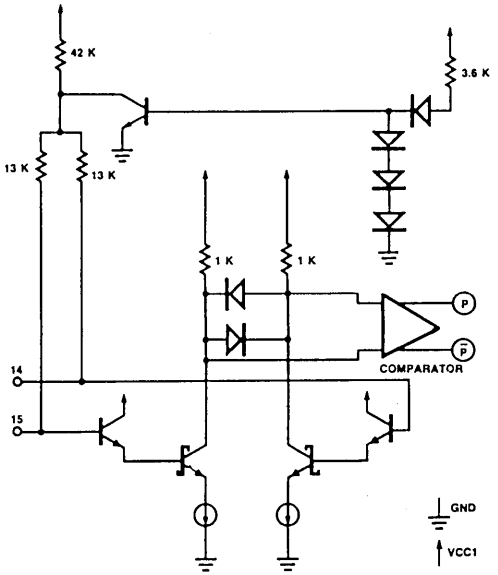
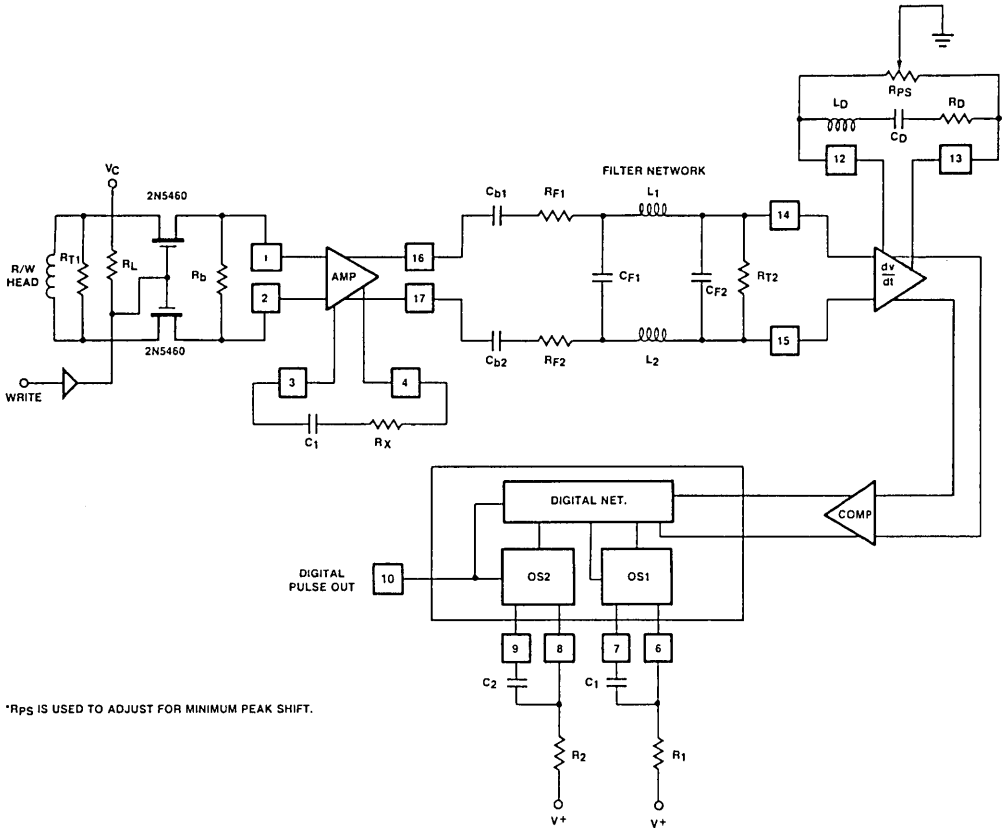


Figure 3. Active Differentiator and Zero Crossing Detector



*RPS IS USED TO ADJUST FOR MINIMUM PEAK SHIFT.

Figure 4. Generalized Circuit Connection for Floppy Disk Read System

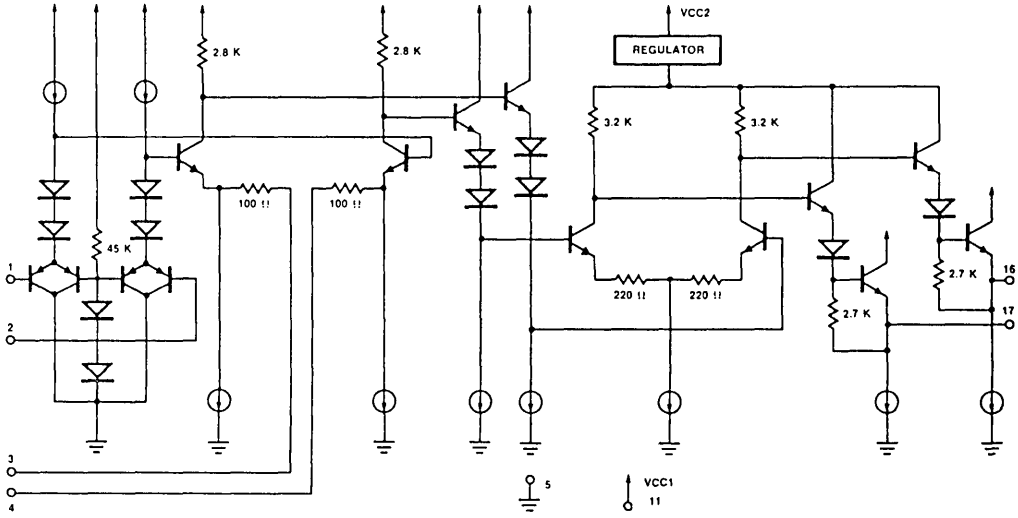


Figure 5. Input Amplifier

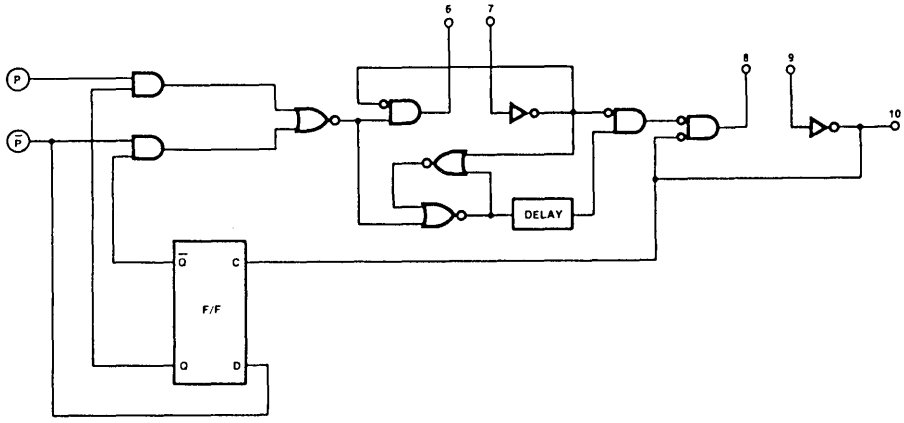


Figure 6. Digital Section

R/W HEAD COUPLING

When switching from the write channel to the read channel, one must be careful not to present a differential voltage to the inputs of the amplifier, for this will result in an amplified swing at the output of the amplifier, which will cause peak shifting at the digital output. A balanced diode network or FET switches, as shown in Figure 4, may be used to overcome this problem.

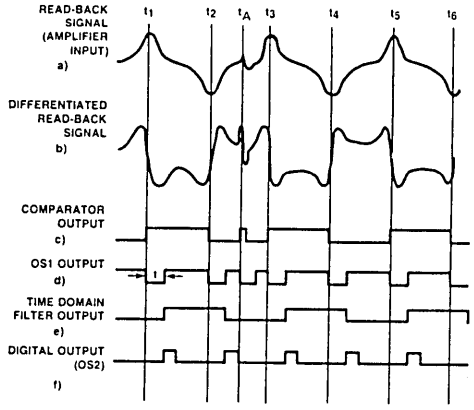


Figure 7a-f. Waveforms Through the XR-3470A/3470B

AMPLIFIER STAGE

The amplifier stage will typically amplify the read back signal by a factor of 110. In order to eliminate any offset between the amplifier stages, a capacitor, C_1, should be inserted between Pins 3 and 4. If the input signal to the amplifier is to be above 25 mV, clamping of the amplifier may occur. To reduce the gain, a resistor R_X may be inserted in series with C_1 between Pins 3 and 4. The graph in Figure 8 shows a plot of normalized gain vs R_X.

It should be noted that capacitor C_1 with R_X and the resistance looking into Pins 3 and 4, will create a pole at approximately

$$\omega p = \frac{1}{(R_X + 250)\, C_1}$$

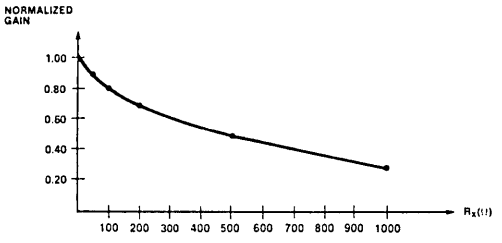


Figure 8. Normalized Gain vs R_X for Amplifier Stage

so C_1 should not be made too low. C_1 = 0.1 μF is nominal for most floppy disk applications.

FILTER NETWORK

The filter network, between the XR-3470A/3470B amplifier stage and differentiator stage, is subject to several system and circuit considerations.

The filter network, first and foremost, must be designed to pass all frequencies up to 1/2 the maximum baud rate, with a constant gain and phase shift. This frequency can be stated as f_{max}, where

$$f_{max} = 1/2\ (\text{Baud rate})_{max}$$

In order to avoid saturation of the amplifier current sources, the current into the filter must not exceed 2.8 mA. In order to meet this condition the impedance of the filter must be governed by the following constraint

$$Z_{min} > \frac{(A_{VD}\, E_P)_{max}}{2.8\ \text{mA}}$$

where A_{VD} is the gain of the amplifier
E_p is the maximum peak voltage of the input signal

The differentiator inputs are dc biased internally. This implies that the dc level from the amplifier stage must be blocked in order not to disturb these levels. Therefore blocking capacitors, C_{b1} and C_{b2}, should be placed before the differentiator inputs. In order to keep the transient response to a minimum it is best to place the dc blocking capacitors before the filter network.

ACTIVE DIFFERENTIATOR

The amplified filtered read back signal is fed into the active differentiator. Here, the peaks of the read back signal are transformed into zero crossings as shown by Figures 7a and 7b.

In order to perform the differentiator function a capacitor C_D is needed across Pins 12 and 13. The selection of C_D for accurate zero crossing is optimized by maximizing current slew rate through C_D, which occurs when

$$C_D = \frac{1\ \text{mA}}{(A_{VD}\, E_P \omega)_{max}\, A_F}$$

Where A_{VD} is the gain of the amplifier
E_p is the maximum expected input voltage
ω is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

As can be seen from Figure 9; the capacitor C_D and the effective output resistance, R_O of transistors Q1 and Q2 produce a pole given by

$$\omega_p = \frac{1}{2R_OC_D}$$

where R_O is typically 40Ω.

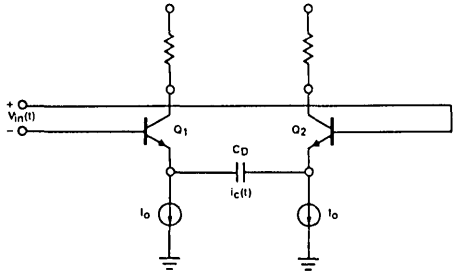


Figure 9. Simplified Active Differentiator Section

In order to obtain a phase shift approaching 90° for perfect differentiation ω_p would have to approach ∞ since

$$\theta = \tan^{-1}(\omega_p/\omega_o)$$

$$\omega_o = \text{operating frequency}$$

It must be considered, however, that making ω_p as high as possible also produces a noise bandwidth as high as possible.

In order to come to a reasonable compromise ω_p should be selected to be ten times the maximum expected operating frequency.

$$\omega_p = 10\,\omega_{max}$$

where ω_{max} is the maximum operating frequency of the system in radians/sec.

Doing this produces a phase shift of approximately 84°, while limiting the noise bandwidth. The design criteria is now given by

$$\omega_{max} = \frac{1}{20R_OC_D}$$

It may be that R_O is too low, creating a pole at a higher frequency than 10 ω_{max}. If this is so one can insert a resistor R_D in series with C_D, giving the equation

$$\omega_{max} = \frac{1}{20RC_D}$$

where $R = R_O + 0.5R_D$

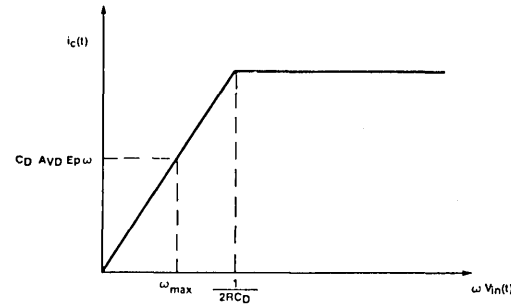


Figure 10. Differentiator Response for C_D and R

In order to reduce the noise bandwidth further a second pole can be introduced at 10 ω_{max} by placing an inductor in series with C_D and R_D, where L_D is given by

$$L_D = \frac{1}{100(\omega_{max})^2\,C_D}$$

The damping ratio, δ, should be between .3 and 1 where

$$\delta = \frac{(R_O + 0.5R_D)\,C_D}{2\sqrt{L_DC_D}}$$

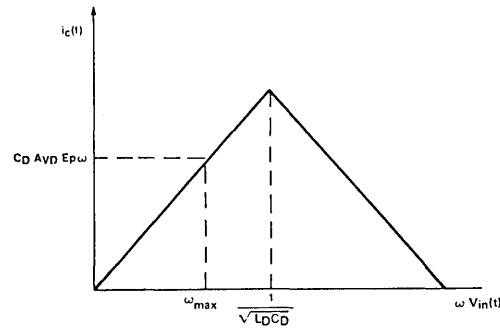


Figure 11. Differentiator Response with R_D, C_D, and L

PEAK SHIFT CONSIDERATIONS

The arrangement shown in Figure 12 will eliminate the current imbalance in the differentiator, and offset in the comparator, thus minimizing the peak shift at the digital output. The potentiometer is adjusted with a minimum sinusoidal Epω at the input, for symmetrical digital waveform at the digital output, Pin 10.

ZERO CROSSING DETECTOR

The differentiated output signals from the active differentiator are run into a comparator. Since the outputs of the active differentiator are 180° out of phase, the comparator will produce an output pulse whenever the differentiated signal crosses zero. This is shown in Figures 7b and 7c.

MONOSTABLE #1 (OS1)

This one shot is used to prevent false digital outputs due to noise at zero crossings as shown at time t_A, in Figure 7a. The adjustment of the one shot is done via external components R_1 and C_1 where

$$1.5\ K < R_1 < 10\ K$$
$$0.150\ pF < C_1 < 680\ pF$$
$$\text{and } t = R_1C_1\ (0.625) + 0.2\ \mu sec$$

The value of t is determined by the maximum period of expected distortion, ΔT, and the maximum operating frequency

$$\text{where } \Delta T < t < \frac{1}{4f_{max}} - \frac{\Delta T}{2}$$

The one shot is triggered on the rising and falling edge of the comparator output as can be seen in Figures 7c and 7d. The time domain filter will change state on the rising edge of OS1's output if and only if the pulse width of the comparator output is greater than the time of OS1's pulse, t. This is shown in Figures 7c, 7d, and 7e.

MONOSTABLE #2 (OS2)

This one shot is used to adjust the pulse width of the digital output pulses at Pin 10. The adjustment of this one shot is done via external components R2 and C2 where

$$1.5\ K < R2 < 10\ K$$
$$150\ pF < C2 < 680\ pF$$

The pulse width of the output pulse is given by

$$t_O = R_2C_2\ (0.625)$$

This one shot is triggered on the rising and falling edges of the time domain filter output, as shown on Figures 7e and 7f, giving the corresponding digital pulses for the peaks of the read back signal, shifted by OS1's time, t, as can be seen from Figures 7a, 7d, and 7f.

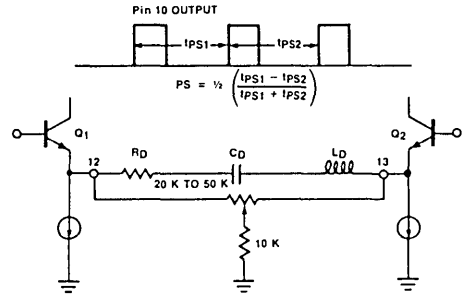


Figure 12. Nulling Network to Minimize Peak Shift (PS)