Programmable Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4202 is an array of four independent operational amplifiers on a single silicon chip. The operating current of the array is externally controlled by a single resistor or current source, allowing the user to trade-off power dissipation for bandwidth.

FEATURES

Programmable
Micropower Operation
Wide Input Voltage and Common Mode Range
Internal Frequency Compensation
No Latch-Up
Matched Parameters
Short-Circuit Protection

APPLICATIONS

The following approximate relations are useful for design:

Gain-Bandwidth Product	≈	50 I_{SET}	(kHz)
Power Supply Current	≈	30 I_{SET}	(μA)
Slew Rate	≈	20 I_{SET}	(V/ms)

Where: I_{SET} is in μA

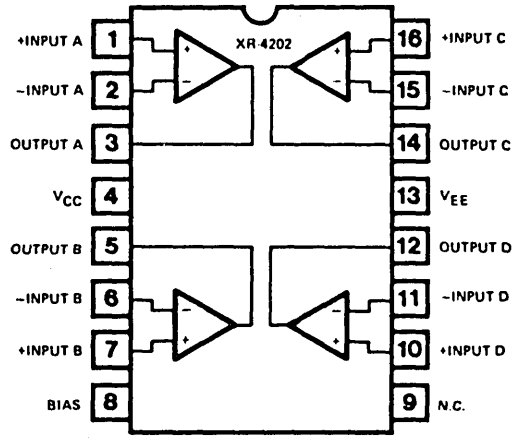
$$I_{SET} = \frac{V_{EE} - V_{BE}}{R_{SET}}$$

WHERE V_{BE} DIODE VOLTAGE ≈ 0.65V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Common Mode Range	V_{EE} to V_{CC}
Short Circuit Duration	Indefinite
Storage Temperature	−60°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4202N	Ceramic	−40°C to +85°C
XR-4202P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-4202 is a quad independently programmable operational amplifier featuring improved performance over industry standard devices such as the 741. Amplifier bias currents can be "programmed" by a single resistor to Pin 8. Bias currents can range from less than 1μA, thus affording the designer flexibility along the device speed/power consumption trade off curve.

ELECTRICAL CHARACTERISTICS

Test Conditions: High Power Mode (V_S = ±15V, I_{SET} = 75 μA and T_A = +25°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Short Circuit Current	5	17	30	mA	I_{SC}	0°C≤ T_A≤70°C
Supply Current	0.8	1.7	6.0	mA	I_S	Note 3
Input Offset Voltage		0.8	5.0	mV	V_{io}	R_S≤10 KΩ
Input Bias Current		80	500	nA	I_b	
Input Off-set Current		10	200	nA	I_{io}	
Input Resistance	0.1	0.6		MΩ	R_{in}	
Input Common Mode Voltage Range	12	±14		±V	V_{iCM}	
Common Mode Rejection Ratio	70	110		dB	CMRR	
Voltage Supply Rejection Ratio		15	150	μV/V	PSRR	
Large Signal Voltage Gain	74	88		dB	A_{VOL}	R_L = 3 KΩ; ΔV_O = ±10 V
Output Voltage Swing	±10	±13.6		±V	V_{out}	R_L = 3 KΩ
Gain-Bandwidth Product		3.5		MHz	f_1	
Phase Margin		45		Deg.		
Rise Time		70		ns	t_R	ΔV_O = ±20 mV
Overshoot		20		%	t_o	ΔV_O = ±20 mV
Channel Separation		120 105		dB dB		Any amp. pair: freq. = 1 Hz, R_L = 3 K Ω Any amp. pair: freq. = 10 KHz, R_L = 3 K Ω
Slew Rate		1.5		V/μs	dV_{out}/dt	
Input Voltage Noise		25		nV/√Hz	e_n	Bandwidth 100 Hz to 10 KHz

Note: Short circuit may be taken to either supply line or ground on only one amplifier at a time.

ELECTRICAL CHARACTERISTICS

Test Conditions: High Power Mode (V_S = ±15V, I_{SET} = 75 μA and T_A = −55°C to +125°C)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Offset Voltage		0.8	10	mV	V_{io}	R_S ≤10 KΩ
Input Bias Current		80	1500	nA	I_b	
Input Offset Current		10	200	nA	I_{io}	
Large Signal Voltage Gain	68	88		dB	A_{vol}	R_L 3 KΩ ΔV_O = ±10 V

ELECTRICAL CHARACTERISTICS

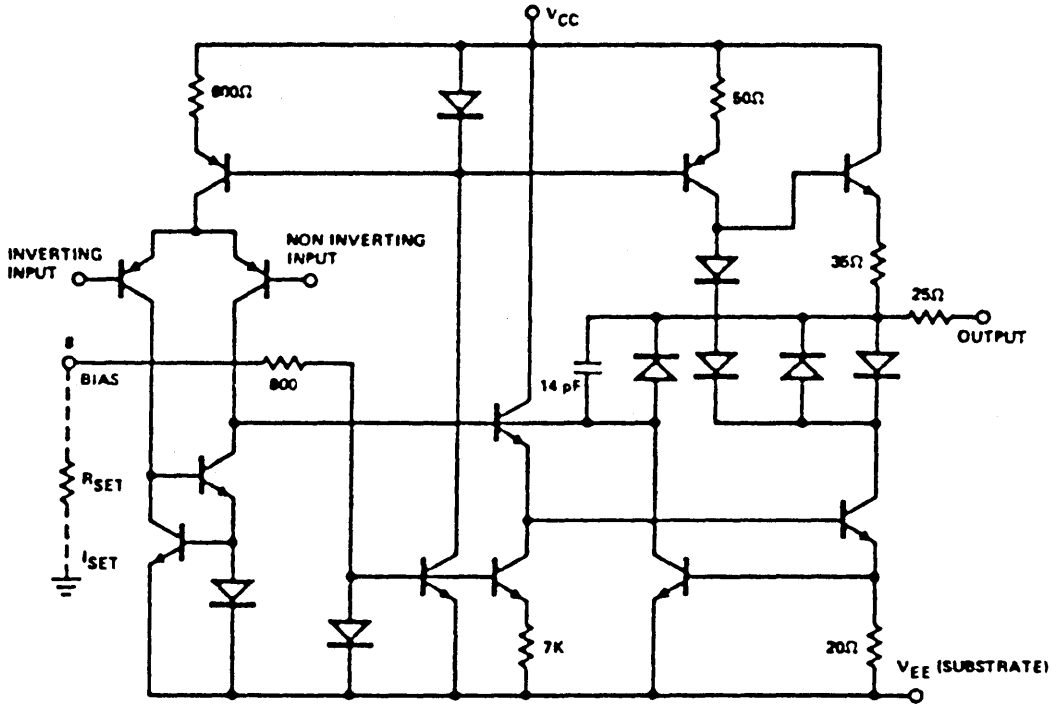
Test Conditions: Micropower Mode (I_{SET} = 1 μA, V_S = ±1.5V)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Supply Current			100	μA	I_S	Note 3
Input Bias Current			200	nA	I_B	
Input Offset Current			20	nA	I_{OS}	
Input Offset Voltage		0.5	5	mV	V_{os}	$R_S \leq$ 10 KΩ
Input Resistance	0.5			MΩ	R_{in}	
Input Common Mode Voltage Range	0.3	±0.8		±V	V_{iCM}	
Common Mode Rejection Ratio	60	100		dB	CMRR	
Voltage Supply Rejection Ratio		20	200	μV/V	PSRR	
Large Signal Voltage Gain	66	80		dB	A_{vol}	$R_L \geq$ 100 KΩ
Gain-Bandwidth Product		50		kHz	GBW	
Phase Margin		75		Deg.		
Slew-Rate		20		V/ms	dV_{out}/dt	
Rise Time		7		μs	t_R	ΔV_O = ±20 mV
Overshoot		0		%	t_o	ΔV_O = ±20 mV
Channel Separation		120 120		dB dB		Freq. = Hz: R_L = 20 KΩ, ΔV_O = ±0.5 V Freq. = 1 KHz: R_L = 10 KΩ, ΔV_O = ±0.5V
Equivalent Input Voltage Noise		200		nV√Hz	e_n	Bandwidth = 100 Hz to 10 KHz

PARAMETER MATCHING (I_{SET} = 75 μA (2))

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Offset Voltage		1		±mV	V_{os}	$R_S \leq$ 10 KΩ
Input Bias Current		10		±nA	I_B	
Input Offset Current		2		±nA	I_{os}	
Gain-Bandwidth Product		100		±KHz	f_1	
Slew Rate		0.2		±V/μs	dV_o/dt	

NOTES: 1. All tests refer to a single op amp unless otherwise specified.
2. Tests apply for parameter matching between any op amp pair.
3. Tests apply to four op amps and bias network.



EQUIVALENT SCHEMATIC DIAGRAM