# Monolithic Tone Decoder

## GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

## FEATURES

Bandwidth adjustable from 0 to 14%.
Logic compatible output with 100 mA current sinking capability
High stable center frequency.
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor.

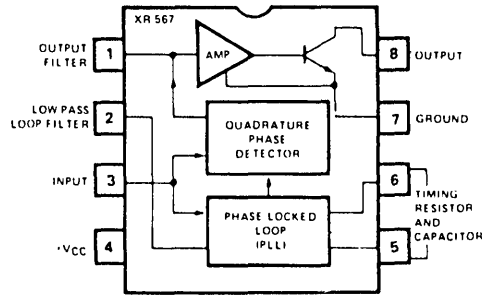
## APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | 10 volts |
| Power Dissipation (package limitation) | |
| Ceramic Package | 385 mW |
| Plastic Package | 300 mW |
| Derate Above +25°C | 2.5 mW/°C |
| Temperature | |
| Operating | |
| XR-567M | −55°C to +125°C |
| XR-567CN/567CP | 0°C to +70°C |
| Storage | −65°C to +150°C |

## FUNCTIONAL BLOCK DIAGRAM




## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-567M | Ceramic | −55°C to +125°C |
| XR-567CN | Ceramic | 0°C to +70°C |
| XR-567CP | Plastic | 0°C to +70°C |

## SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate employing the XR-L567 in low power circuits.

# XR-567

## ELECTRICAL CHARACTERISTICS

**Test Conditions:** $V_{CC}$ = +5V, $T_A$ = 25°C, unless otherwise specified. Test circuit of Figure 2.

| PARAMETERS | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Supply Voltage Range | 4.75 | | 9.0 | V dc | |
| Supply Current | | | | | |
| Quiescent XR-567M | | 6 | 8 | mA | $R_L$ = 20kΩ |
| XR-567C | | 7 | 10 | mA | $R_L$ = 20 kΩ |
| Activated XR-567M | | 11 | 13 | mA | $R_L$ = 20 kΩ |
| XR-567C | | 12 | 15 | mA | $R_L$ = 20 kΩ |
| Output Voltage | | | 15 | V | |
| Negative Voltage at Input | | | −10 | V | |
| Positive Voltage at Input | | | $V_{CC}$ + 0.5 | V | |
| **CENTER FREQUENCY** | | | | | |
| Highest Center Frequency | 100 | 500 | | kHz | |
| Center Frequency Stability | | | | | |
| Temperature $T_A$ = 25°C | | 35 | | ppm/°C | See Figure 9 |
| 0 < $T_A$ < 70°C | | ±60 | | ppm/°C | See Figure 9 |
| −55 < $T_A$ < +125°C | | ±140 | | ppm/°C | See Figure 9 |
| Supply Voltage | | | | | |
| XR-567M | | 0.5 | 1.0 | %/V | $f_o$ = 100 kHz |
| XR-567C | | 0.7 | 2.0 | %/V | $f_o$ = 100 kHz |
| **DETECTION BANDWIDTH** | | | | | |
| Largest Detection Bandwidth | | | | | |
| XR-567M | 12 | 14 | 16 | % of $f_o$ | $f_o$ = 100 kHz |
| XR-567C | 10 | 14 | 18 | % of $f_o$ | $f_o$ = 100 kHz |
| Largest Detection Bandwidth Skew | | | | | |
| XR-567M | | 1 | 2 | % of $f_o$ | |
| XR-567C | | 2 | 3 | % of $f_o$ | |
| Largest Detection Bandwidth Variation | | | | | |
| Temperature | | ±0.1 | | %/°C | $V_{in}$ = 300 mV rms |
| Supply Voltage | | ±2 | | %/V | $V_{in}$ = 300 mV rms |
| **INPUT** | | | | | |
| Input Resistance | | 20 | | kΩ | |
| Smallest Detectable Input Voltage | | 20 | 25 | mV rms | $I_L$ = 100 mA, $f_i$ = $f_o$ |
| Largest No-Output Input Voltage | 10 | 15 | | mV rms | $I_L$ = 100 mA, $f_i$ = $f_o$ |
| Greatest Simultaneous Outband Signal to Inband Signal Ratio | | +6 | | dB | |
| Minimum Input Signal to Wideband Noise Ratio | | −6 | | dB | $B_n$ = 140 kHz |
| **OUTPUT** | | | | | |
| Output Saturation Voltage | | 0.2 | 0.4 | V | $I_L$ = 30 mA, $V_{in}$ = 25 mV rms |
| | | 0.6 | 1.0 | V | $I_L$ = 100 mA, $V_{in}$ = 25 mV rms |
| Output Leakage Current | | 0.01 | 25 | μA | |
| Fastest ON-OFF Cycling Rate | | $f_o$/20 | | | |
| Output Rise Time | | 150 | | ns | $R_L$ = 50Ω |
| Output Fall Time | | 30 | | ns | $R_L$ = 50Ω |

## DEFINITION OF XR-567 PARAMETERS

### CENTER FREQUENCY $f_0$

$f_0$ is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor $R_1$ between pins 5 and 6, and capacitor $C_1$ from pin 6 to ground $f_0$ can be approximated by

$$f_0 \approx \frac{1}{R_1 C_1}$$

where $R_1$ is in ohms and $C_1$ is in farads.

### DETECTION BANDWIDTH (BW)

The *detection bandwidth* is the frequency range centered about $f_0$, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of $f_0$, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_0 C_2}}$$

where $V_i$ is the input signal in volts, rms, and $C_2$ is the capacitance at pin 2 in $\mu$F.

### LARGEST DETECTION BANDWIDTH

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

### DETECTION BAND SKEW

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, $f_0$. It is defined as $(f_{max} + f_{min} - 2 f_0)/f_0$, where $f_{max}$ and $f_{min}$ are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls).

## DESCRIPTION OF CIRCUIT CONTROLS

### OUTPUT FILTER — $C_3$ (Pin 1)

Capacitor $C_3$ connected from pin 1 to ground forms a simple low-pass *post detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3 C_3$, where $R_3$ (4.7 kΩ) is the internal impedance at pin 1.

The precise value of $C_3$ is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that $C_3$ be $\geq 2\,C_2$, where $C_2$ is the loop filter capacitance at pin 2.

If the value of $C_3$ becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across $C_3$ reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of $C_3$ is too small, the beat rate at the output of the quadrature detector (see Functional Block Diagram) may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

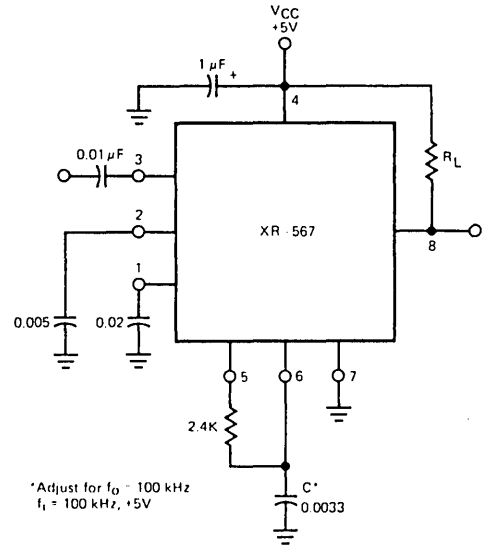



**Figure 2. XR-567 Test Circuit**

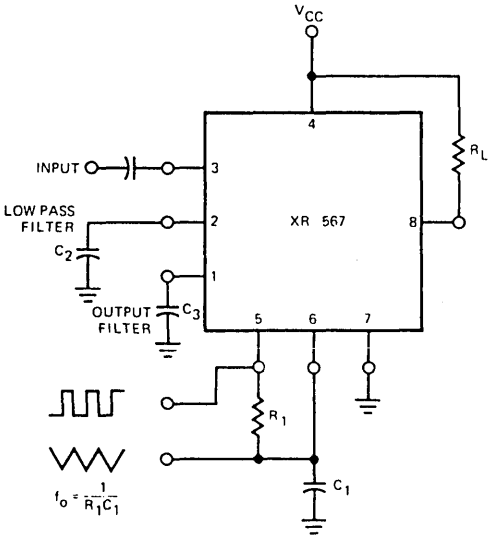



**Figure 3. XR-567 Connection Diagram**

## TYPICAL CHARACTERISTIC CURVES

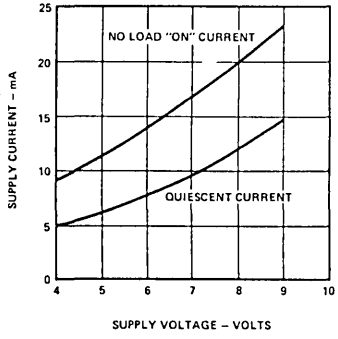



**Figure 4. Supply Current Versus Supply Voltage**

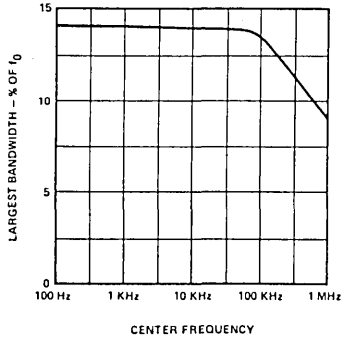



**Figure 5. Largest Detection Bandwidth Versus Operating Frequency**

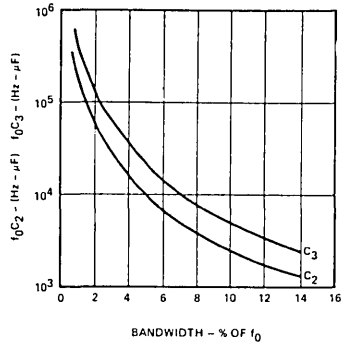



**Figure 6. Detection Bandwidth as a Function of $C_2$ and $C_3$**

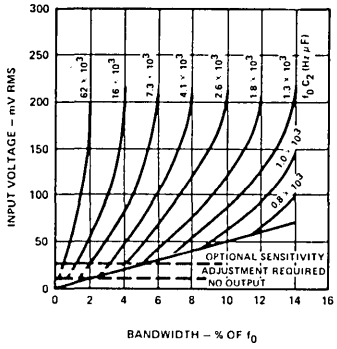



**Figure 7. Bandwidth Versus Input Signal Amplitude ($C_2$ in μF)**

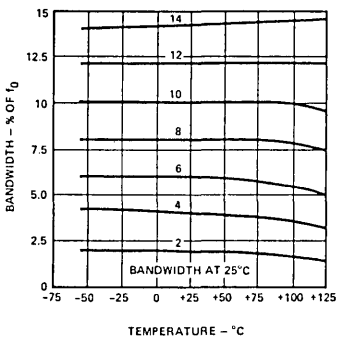



**Figure 8. Bandwidth Variation with Temperature**

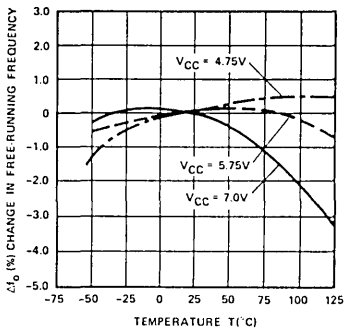



**Figure 9. Frequency Drift with Temperature**



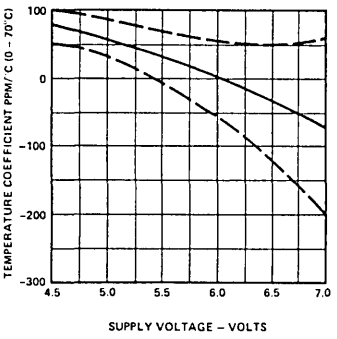



**Figure 10. Temperature Coefficient of Center Frequency (Mean and S.D.)**

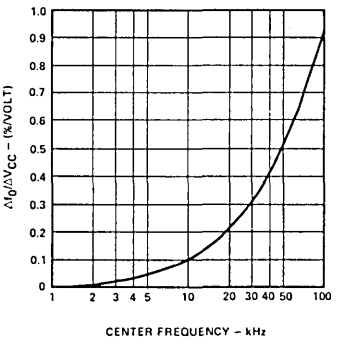



**Figure 11. Power Supply Dependence of Center Frequency**

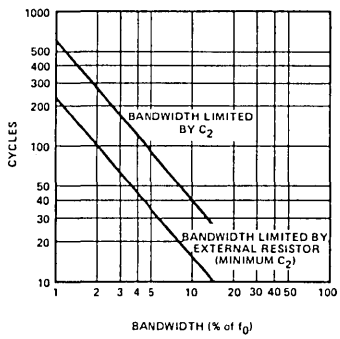



**Figure 12. Greatest Number of Cycles Before Output**

### LOOP FILTER — $C_2$ (Pin 2)

Capacitor $C_2$ connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-567. The filter time constant is given by $T_2 = R_2C_2$, where $R_2$ (10 kΩ) is the impedance at pin 2.

The selection of $C_2$ is determined by the detection bandwidth requirements, as shown in Figure 6. For additional information see section on "Definition of XR-567 Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 $f_o$, with a slope of approximately 20 mV/% frequency deviation.

### INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ.

### TIMING RESISTOR $R_1$ AND CAPACITOR $C_1$ (Pins 5 and 6)

The center frequency of the decoder is set by resistor $R_1$ between pins 5 and 6, and capacitor $C_1$ from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately $V_{CC}$ – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

### LOGIC OUTPUT (Pin 8)

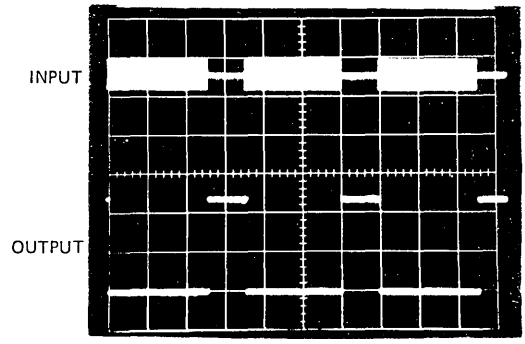
Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, $R_L$, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, $R_L$ can be connected to a supply voltage, V+, higher than the $V_{CC}$ supply. For safe operation, V+ ≤ 20 volts.

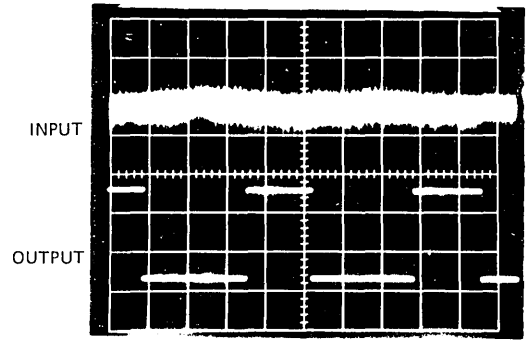
## OPERATING INSTRUCTIONS

### SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the XR-567 is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components $R_1$, $C_1$, $C_2$, and $C_3$.




Response to 100 mV rms tone burst.
$R_L$ = 100 ohms.




Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = –6 dB $R_L$ = 100 ohms

Noise Bandwidth = 140 Hz

**Figure 13. Typical Response**

1. $R_1$ and $C_1$ should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, $R_1$ should be selected such that 2kΩ ≤ $R_1$ ≤ 20 kΩ, and the $R_1C_1$ product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, $C_2$, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of $C_2$ accordingly. Or, if the input amplitude variation is known, the required $f_oC_2$ product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i$ > 200 mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the $f_oC_2$ product.

3. Capacitor $C_3$ sets the ·nd edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If $C_3$ is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value of $C_3$ is 2 $C_2$.

Conversely, if $C_3$ is too large, turn-on and turn-off of the output stage will be delayed until the voltage across $C_3$ passes the threshold value.

## PRINCIPLE OF OPERATION

The XR-567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, $f_o$, is determined by the selection of $R_1$ and $C_1$ connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, $C_2$; and the output response speed is controlled by the output filter capacitor, $C_3$.

## OPTIONAL CONTROLS

### PROGRAMMING

Varying the value of resistor $R_1$ and/or capacitor $C_1$ will change the center frequency. The value of $R_1$ can be changed either mechanically or by solid state switches. Additional $C_1$ capacitors can be added by grounding them through saturated npn transistors.

### SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus maximum operating speed is obtained when the value of capacitor $C_2$ is minimum. At the instant an input signal is applied its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of $C_2$ and $C_3$, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o},\ C_3 = \frac{260}{f_o}\ \mu F$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 14 can be used to bring the quiescent $C_3$ voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

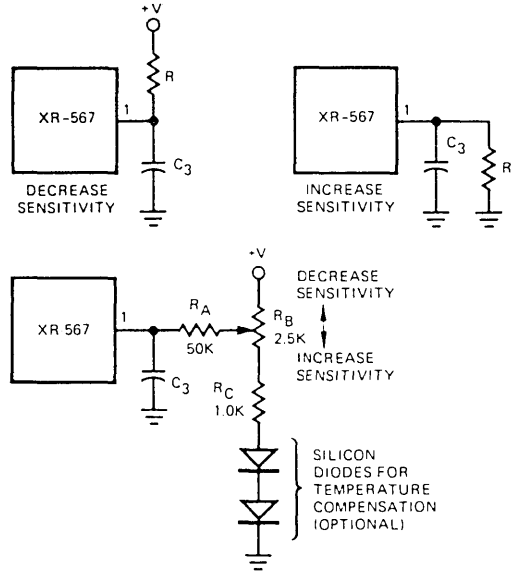



**Figure 14. Optional Sensitivity Connections**

## CHATTER

When the value of $C_3$ is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (pin 1) or, by increasing the size of capacitor $C_3$. Generally, the feedback method is preferred since keeping $C_3$ small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 15. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

### SKEW ADJUSTMENT

The circuits shown in Figure 16 can be used to change the position of the detection band (capture range) with-

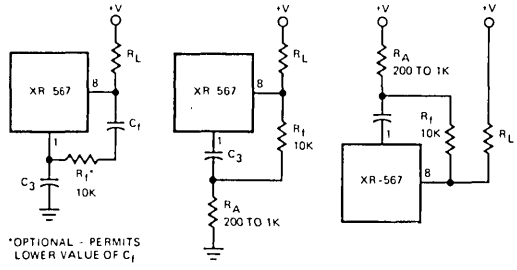



**Figure 15. Methods of Reducing Chatter**

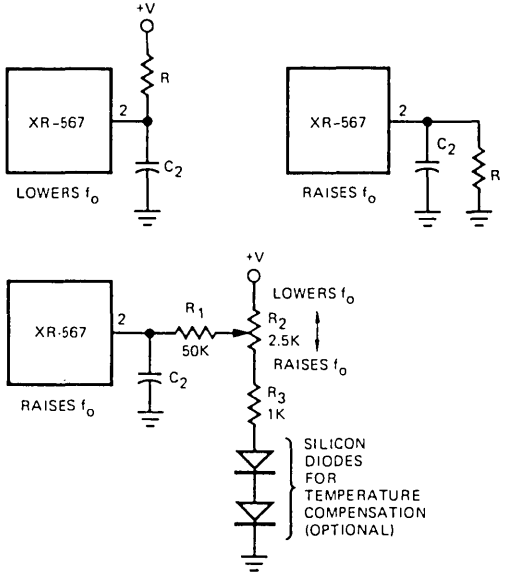



**Figure 16. Connections to Reposition Detection Band**

in the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since $R_3$ also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

### OUTPUT LATCHING

In order to latch the output of the XR-567 "on" after a signal is received, it is necessary to include a feedback resistor around the output stage, between pin 8 and pin 1, as shown in Figure 17. Pin 1 is pulled up to unlatch the output stage.

### BANDWIDTH REDUCTION

The bandwidth of the XR-567 can be reduced by either increasing capacitor $C_2$ or reducing the loop gain. Increasing $C_2$ may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 18 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. The reduced impedance level at pin 2 will require a larger value of $C_2$ for a given cut-off frequency.

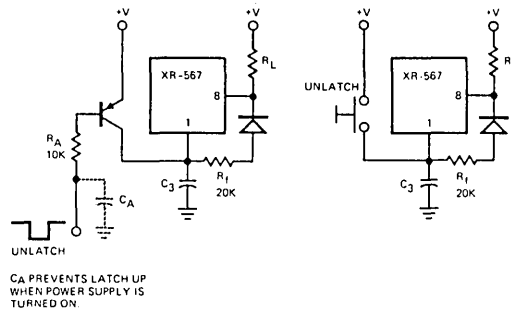
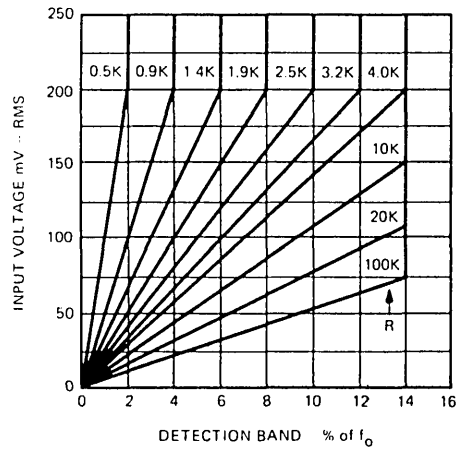
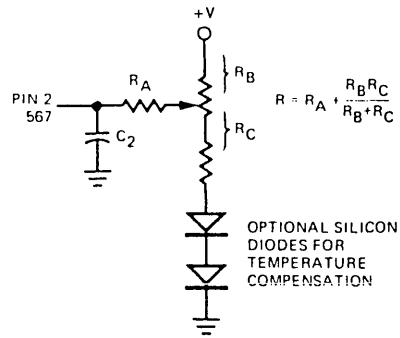



**Figure 17. Output Latching**




$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

NOTE: ADJUST CONTROL FOR SYMMETRY OF DETECTION BAND EDGES ABOUT $f_o$.

**Figure 18. Bandwidth Reduction**

## PRECAUTIONS

1. The XR-567 will lock on signals near $(2n + 1)\ f_o$ and produce an output for signals near $(4n + 1)\ f_o$, for n = 0,1,2 - etc. Signals at 5 $f_o$ and 9 $f_o$ can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 12.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

## ADDITIONAL APPLICATIONS

### DUAL TIME CONSTANT TONE DECODER

For some applications it is important to have a tone decoder with narrow bandwidth and fast response time. This can be accomplished by the dual time constant tone decoder circuit shown in Figure 19. The circuit has two low-pass loop filter capacitors, $C_2$ and $C'_2$. With no input signal present, the output at pin 8 is high, transistor $Q_1$ is off, and $C'_2$ is switched out of the circuit. Thus the loop low-pass filter is comprised of $C_2$, which can be kept as small as possible for minimum response time.

When an in-band signal is detected, the output at pin 8 will go low, $Q_1$ will turn on, and capacitor $C'_2$ will be switched in parallel with capacitor $C_2$. The low-pass filter capacitance will then be $C_2 + C'_2$. The value of $C'_2$ can be quite large in order to achieve narrow bandwidth. Notice that during the time that no input signal is being received, the bandwidth is determined by capacitor $C_2$.

### NARROW BAND FM DEMODULATOR WITH CARRIER DETECT

For FM demodulation applications where the bandwidth is less than 10% of the carrier frequency, an XR-567

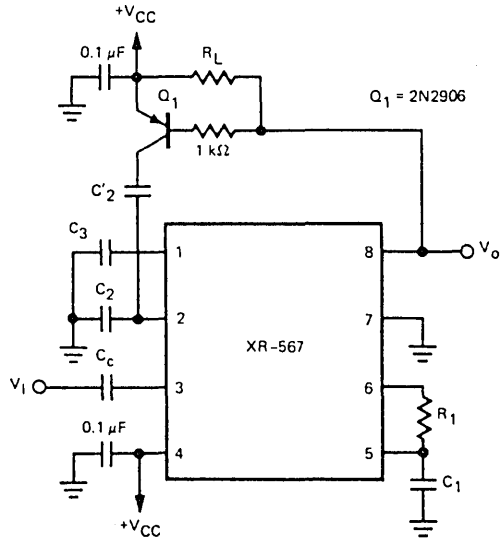



**Figure 19. Dual Time Constant Tone Decoder**

can be used to detect the presence of the carrier signal. The output of the XR-567 is used to turn off the FM demodulator when no carrier is present, thus acting as a squelch. In the circuit shown, an XR-215 FM demodulator is used because of its wide dynamic range, high signal/noise ratio and low distortion. The XR-567 will detect the presence of a carrier at frequencies up to 500 kHz.

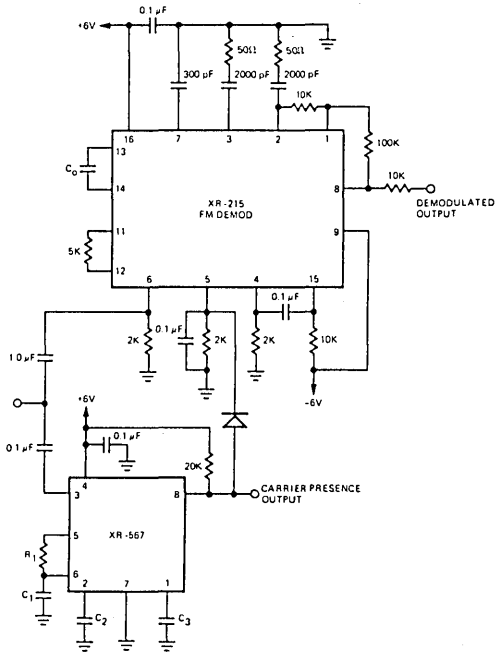



**Figure 20. Narrow Band FM Demodulator with Carrier Detect**

## DUAL TONE DECODER

In dual tone communication systems, information is transmitted by the simultaneous presence of two separate tones at the input. In such applications two XR-567 units can be connected in parallel, as shown in Figure 21 to form a dual tone decoder. The resistor and capacitor values of each decoder are selected to provide the desired center frequencies and bandwidth requirements.

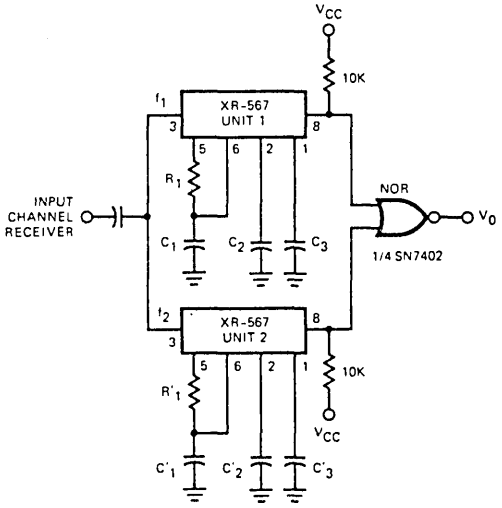



**Figure 21. Dual Tone Decoder**

## PRECISION OSCILLATOR

The current-controlled oscillator (CCO) section of the XR-567 provides two basic output waveforms as shown in Figure 22. The squarewave is obtained from pin 5, and the exponential ramp from pin 6. The relative phase relationships of the waveforms are also provided in the figure. In addition to being used as a general purpose oscillator or clock generator, the CCO can also be used for any of the following special purpose oscillator applications:

1. **High-Current Oscillator**

   The oscillator output of the XR-567 can be amplified using the output amplifier and high-current logic output available at pin 8. In this manner, the circuit can switch 100 mA load currents without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 23. The oscillator frequency can be modulated over ±6% in frequency by applying a control voltage to pin 2.

2. **Oscillator with Quadrature Outputs**

   Using the circuit connection of Figure 24 the XR-567 can function as a precision oscillator with two separate squarewave outputs (at pins 5 and 8, respectively) that are at nearly quadrature phase with each other. Due to the internal biasing arrangement the actual phase shift between the two outputs is typically 80°.

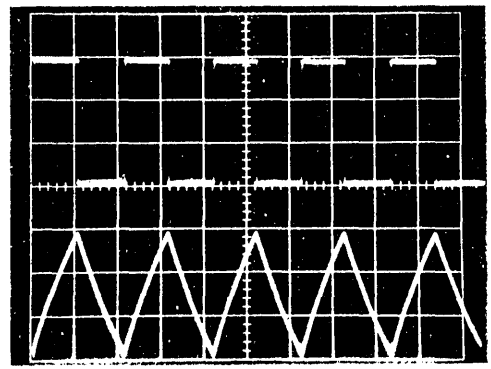


**Figure 22. Oscillator Output Waveform Available From CCO Section.**
**Top: Square Wave Output at Pin 5:**
**Amplitude = (V+ −1.4V), pp.,**
**Avg. Value = V+/2**
**Bottom: Exponential Triangle Wave at Pin 6:**
**Amplitude = 1V pp., Avg. Value = V+/2**

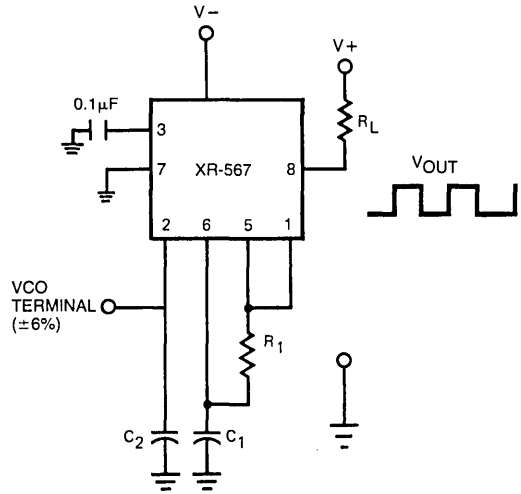



**Figure 23. Precision Oscillator to Switch 100 mA Loads**

3. **Oscillator with Frequency Doubled Output**

   The CCO frequency can be doubled by applying a portion of the squarewave output at pin 5 back to the input at pin 3, as shown in Figure 25. In this manner, the quadrature detector functions as a frequency doubler and produces an output of 2 $f_0$ at pin 8.

## FSK DECODING

XR-567 can be used as a low speed FSK demodulator. In this application the center frequency is set to one of

the input frequencies, and the bandwidth is adjusted to leave the second frequency outside the detection band. When the input signal is frequency keyed between the *in-band* signal and the *out-band* signal, the logic state of the output at pin 8 is reversed. Figure 26 shows the FSK input ($f_2 = 3\ f_1$) and the demodulated output signals, with $f_0 = f_2 = 1$ kHz. The circuit can handle data rates up to $f_0/10$ baud.

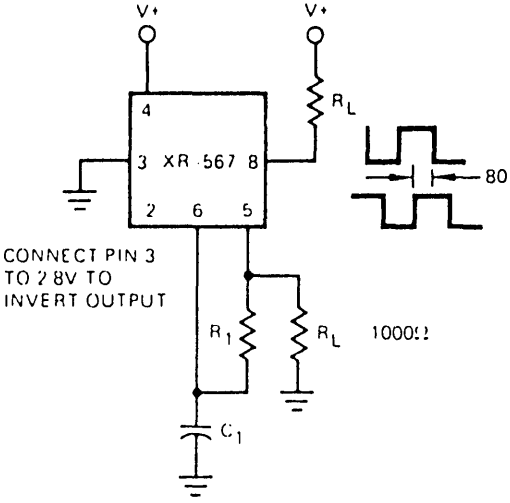



**Figure 24. Oscillator with Quadrature Output**

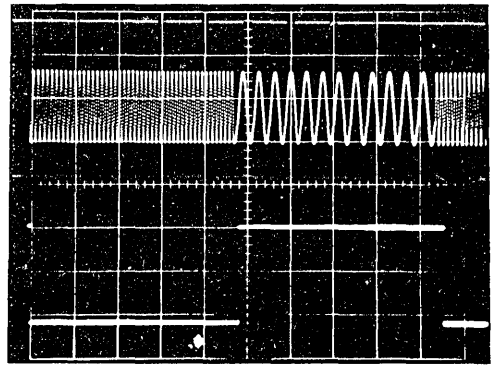
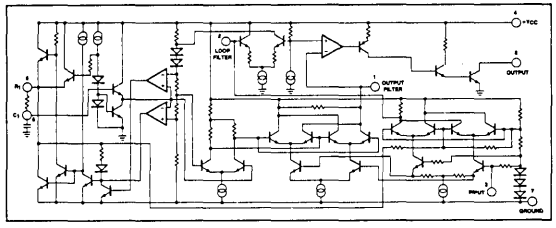


**Figure 26. Input and Output Waveforms for FSK Decoding**
**Top: Input FSK Signal ($f_2 = 3f_1$)**
**Bottom: Demodulated Output**



EQUIVALENT SCHEMATIC DIAGRAM

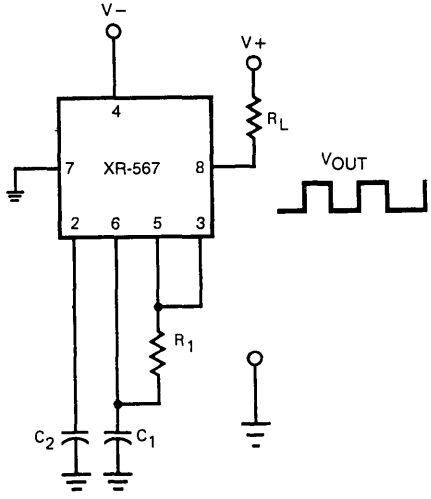



**Figure 25. Oscillator with Double Frequency Output**