# T1, T148C, & 2 M Bit/s PCM Line Repeater

## GENERAL DESCRIPTION

The XR-T5600/T5620 is a bipolar monolithic repeater IC designed for PCM carrier systems operating at 1.544 M bit/s (T1), 2 M bit/s, or 2.37 M bit/s (T148C). It provides all of the active circuits required for one side of a PCM repeater. A crystal filter clock extraction version of XR-T5600/T5620 is available as XR-T5700/T5720.

## FEATURES

Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports
2 M Bit/s Capability

## APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 M Bit/s PCM Repeater
T1C PCM Repeater (requires external preamplifier)

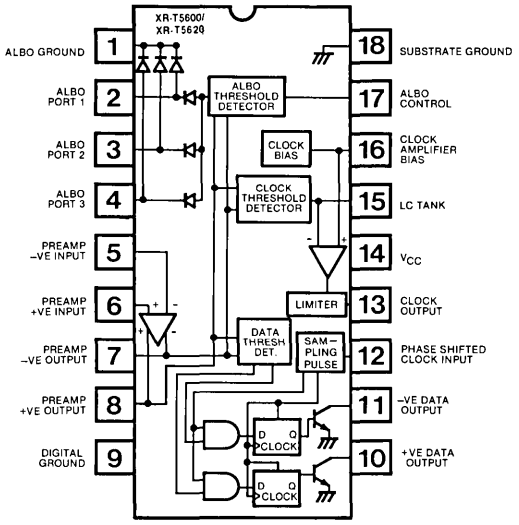
## ORDERING INFORMATION

| Part Number | Package | Operation Temperature |
|---|---|---|
| XR-T5600 | Plastic | −40°C to 85°C |
| XR-T5620 | Plastic or Ceramic | −40°C to 85°C |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage Temperature | -65°C to +150°C |
| Operating Temperature | -40°C to +85°C |
| Supply Voltage | -0.5 to +10 V |
| Supply Voltage Surge (10 ms) | +25 V |
| Input Voltage (except Pin 2,3,4,17) | -0.5 to 7 V |
| Input Voltage (Pin 2,3,4,17) | -0.5 to +0.5 V |
| Data Output Voltage (Pin 10, 11) | 20 V |
| Voltage Surge (Pin 5,6,10,11) (10 msec only) | 50 V |

## FUNCTIONAL BLOCK DIAGRAM




## SYSTEM DESCRIPTION

The XR-T5600/T5620 performs most of the functions required for one side of a PCM repeater operating at 2 M bit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build-out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into the external tank coil at Pin 15. The sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488 ns) in the latches. They appear as half-width output pulses at Pins 10 and 11.

## ELECTRICAL CHARACTERISTICS

**Test Conditions:** $T_A = 25°C$, $V_{CC} = 5.1\ V \pm 5\%$, unless specified otherwise (see Figure 1).

| PARAMETERS | PINS | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Supply Current | 14 | | 22 | 30 | mA | |
| Data Output Leakage Current | 10,11 | | 0 | 100 | μA | $V_{pull\text{-}up} = 15\ V$, $V_{CC} = 5.35\ V$ |
| ALBO Port Off Voltage | 2,3,4 | | 0 | 0.1 | V | |
| Amplifier Pin Voltage | 5,6,7,8 | 2.4 | 2.9 | 3.4 | V | |
| DYNAMIC CHARACTERISTICS AMPLIFIER | | | | | | |
| Output Offset Voltage | | -50 | 0 | 50 | mV | $R_S = 8.2\ k\Omega$ |
| AC Gin @ 1 MHz | | 47 | 50 | 53 | dB | |
| Input Impedance | | 20 | | | kΩ | |
| Output Impedance | | | | 200 | Ω | |
| ALBO | | | | | | |
| ALBO Off Impedance | | 20 | | 25 | kΩ | |
| ALBO On Imepdance | | | | 25 | Ω | |
| THRESHOLDS | | | | | | |
| ALBO Threshold | | 1.4 | 1.5 | 1.6 | V | |
| Clock Threshold as % of ALBO Threshold | | 68 | | 80 | % | |
| DATA Threshold as % of ALBO Threshold | | 42 | | 49 | % | |
| Clock Drive Current | | 0.7 | | 1.4 | mA | At $V_O = V_{ALBO}$ Threshold |
| OUTPUT STAGES | | | | | | $R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$ |
| Output Pulse Rise Time | | | | 40 | ns | |
| Output Pulse Fall Time | | | | 40 | ns | |
| Output Pulse Width | | 224 | 244 | 264 | ns | |
| Output Pulse Width Differential | | -10 | | +10 | ns | |
| Buffer Gate Voltage (Low) | | 0.65 | | 0.95 | V | |
| Buffer Gate Voltage Differential | | -0.15 | | 0.15 | V | |

## ELECTRICAL CHARACTERISTICS

**Test Conditions:** Unless otherwise stated, all characteristics shall apply over the operating temperature range of -40°C to +85°C with $V_{CC}$ = 5.1 V ± 5%, all voltages referred to ground = 0 V.

| SYMBOL | PARAMETERS | PINS | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| GENERAL (Ref. Figure 2) | | | | | | | |
| $I_S$ | Supply Current | 14 | | 22 | 30 | mA | |
| $I_{LD}$ | Data Output Leakage Current | 10,11 | | 6 | 100 | µA | From $V_S$ (See Note 1) |
| | Amplifier Pin Voltages | 5,6,7,8 | 2.4 | 2.9 | 3.4 | V | |
| | ALBO Ports Off Voltage | 2,3,4 | | 0 | 0.1 | V | |

Note: 1. $V_S$ = 15 V, $V_{CC}$ = 5.35 V

| AMPLIFIER (Ref. Figure 2, Only Pins 1, 9, 10...18 connected) | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Input Offset Voltage | 5 & 6 | -10 | | +10 | mV | $R_S$ = 8.2 kΩ (See Note 1) |
| | Input Bias Current | 5 & 6 | 0 | | 5 | µA | $R_S$ = 8.2 kΩ (See Note 1) |
| | Input Offset Current | 5 & 6 | -1 | | 1 | µA | $R_S$ = 8.2 kΩ (See Note 1) |
| | Output Offset Voltage | 7 & 8 | -50 | 0 | 50 | mV | $R_S$ - 8.2 kΩ (See Note 1) |
| | Common Mode Rejection Ratio | 7 & 8 | 30 | | | dB | $V_{CC}$ ±10% |
| | Output Voltage Swing | 7 & 8 | 2.2 | | | V | |

Note: 1. $R_S$ = Source Resistance

| CLOCK AMPLIFIER (Ref. Figure 2, Disconnect Pin 15 from Pin 16) | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Input Offset Voltage | 15 & 16 | 0.5 | | 6 | mV | $R_S$ = 10 kΩ (See Note 1) |
| | Input Bias Current | 15 & 16 | | | 10 | µA | T = 25°C |
| | Max. Output Voltage | 13 | 0.7 | | | V | |
| | Min. Output Voltage | 13 | 0.7 | | | V | |
| | Max./Min. Output Voltage Difference | – | 0.7 | | 50 | mV | |

Notes:
1. $R_S$ = Source resistance, Pin 15 positive with respect to Pin 16
2. Pin 15 = Pin 16 = 3.6 V
3. Pin 15 = 2.6 V, Pin 16 = 3.6 V
4. Pin 15 = 4.6 V, Pin 16 = 3.6 V
5. Calculation only

| SYMBOL | PARAMETERS | PINS | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| ALBO (Ref. Figure 2) | | | | | | | |
| | On Current | 1 | 3 | | | mA | $V_8$-$V_7$ = ± 1.75 V |
| | Drive Current | 17 | 0.4 | | 1.4 | mA | $V_8$-$V_7$ = ± 1.75 V |
| | Resistance Pin 17 to Ground | | 35 | 50 | 70 | kΩ | Not Powered |

DYNAMIC CHARACTERISTICS



| AMPLIFIER (Ref. Figure 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ao | AC Gain @ 1 MHz | 5 to 8 | 47 | 50 | 53 | dB | |
| $Z_{in}$ | Input Impedance | 5 | 20 | | | kΩ | (See Note 1) |
| $Z_{out}$ | Output Impedance | 7,8 | | | 200 | Ω | (See Note 2) |

Notes: 1. At 1 MHz, AC ground Pins 7 and 8, disconnect 51 Ω resistor, allow for in-circuit R,C
2. At 1 MHz, use Figure 2

| CLOCK AMPLIFIER (Ref. Figure 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ao | AC Gain | 15, 16 to 13 | 32 | | | dB | (See Note 1) |
| BW | -3 dB Bandwidth | 15, 16 to 13 | 10 | | mHz | | (See Note 2) |
| $t_d$ | Delay | 15 to 13 | 8 | | 12 | ns | (See Note 3) |
| $Z_{out}$ | Output Impedance | 13 | | | 200 | Ω | (See Note 4) |

Notes: 1. Remove dc offset, at 2.048 MHz, Pin 13 = 1 V pk-pk sine wave
2. Remove dc offset, Pin 13 = 1 V pk-pk sine wave
3. Remove dc offset, Pin 15 = 2 V pk-pk sine wave; delay from Pin 15 negative-going zero crossover to Pin 13 positive edge
4. Remove dc offset, at 2.048 MHz

| ALBO (Ref. Figure 2) | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Off Impedance | 2,3,4 | 20 | | | kΩ | (See Note 1) |
| | Intermediate Impedance Difference | 2,3,4 | | | 5 | % | (See Note 2) |
| | On Impedance | 2,3,4 | | | 25 | Ω | (See Note 3) |
| | Transconductance | 7/8 to 1 | | | 0.03 | dB | (See Note 4) |

Notes: 1. At 1 MHz, allow for in-circuit R,C
2. At 1 MHz, $V_8$-$V_7$ adjusted for current at Pin 1 = 100 μA
3. At 1 MHz, $V_8$-$V_7$ adjusted for ± 1.75 V
4. At 1 MHz, change in $V_8$-$V_7$ for current at Pin 1 = 10 μA to 100 μA

| SYMBOL | PARAMETERS | PINS | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| THRESHOLD VOLTAGES (Ref. Figure 3) | | | | | | | |
| | ALBO Threshold +ve | 8-7 | 1.4 | 1.5 | 1.6 | V | (See Notes 1 & 2) |
| | ALBO Threshold -ve | 7-8 | 1.4 | 1.5 | 1.6 | V | (See Notes 1 & 2) |
| | ALBO Threshold Difference | – | -5 | 0 | 5 | % | (See Note 3) |
| | Clock Drive on Current (peak) +ve | 18 | | 1.0 | 1.4 | mA | (See Note 4) |
| | Clock Drive on Current (peak) -ve | 18 | | 1.0 | 1.3 | mA | (See Note 5) |
| | Clock Drive on Current Difference | – | -5 | 0 | 5 | % | (See Note 3) |
| | Clock Threshold +ve | 87 | 68 | | 80 | % | (See Notes 1, 6, 8) |
| | Clock Threshold -ve | 7-8 | 68 | | 80 | % | (See Notes 1, 7, 8) |
| | Clock Threshold Difference | – | -5 | 0 | 5 | % | (See Note 3) |
| | Data Threshold +ve | 8-7 | 44 | 46 | 48 | % | (See Notes 1,8,9,11) |
| | Data Threshold -ve | 7-8 | 44 | 46 | 48 | % | (See Notes 1,8,10,11) |
| | Data Threshold Difference | – | -3 | 0 | 3 | % | (See Note 3) |

Notes: 1. Pk/pk voltage at Pins 7 and 8 of a 1 MHz sine wave derived through amplifier and measured differentially
2. Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3 mA
3. Calculation only
percentage difference calculated from $\left(\frac{\text{higher value}}{\text{lower value}} - 1\right) \times 100$ %
4. $V_8$-$V_7$ adjusted to ALBO threshold +ve voltage, ref. Pin 16 = 3.6 V
5. $V_7$-$V_8$ adjusted to ALBO threshold -ve voltage, ref. Pin 16 = 3.6 V
6. $V_8$-$V_7$ adjusted to peak current at Pin 18 = ½ (clock drive on current peak +ve)
7. $V_7$-$V_8$ adjusted to peak current at Pin 18 = ½ (clock drive on current peak -ve)
8. Figure taken as a percentage of lower ALBO threshold
9. $V_8$-$V_7$ increased until 1 MHz PRF on counter at Pin 10
10. $V_7$-$V_8$ increased until 1 MHz PRF on counter at Pin 11
11. With 2,048 MHz 2 V pk-pk sine wave to Pin 15 with 180 $\mu$H in parallel with 36 $\Omega$ to Pin 16 = 3.6 V

| OUTPUT STAGES (Ref. Figure 3. Use 180 $\mu$H inductor between Pins 15 and 16. Apply 2.048 MHz 2V pk/pk to Pin 15.) | | | | | | | |
|---|---|---|---|---|---|---|---|
| $t_r$ | Output Pulse Rise Time +ve | 10 | | | 40 | ns | 10% - 90% |
| $t_r$ | Output Pulse Rise Time -ve | 11 | | | 40 | ns | 10% - 90% |
| $t_f$ | Output Pulse Fall Time +ve | 10 | | | 40 | ns | 10% - 90% |
| $t_f$ | Output Pulse Fall Time -ve | 11 | | | 40 | ns | 10% - 90% |
| $t_W$ | Output Pulse Width +ve | 10 | 224 | 244 | 264 | ns | at 50% |
| | Output Pulse Width -ve | 11 | 224 | 244 | 264 | ns | at 50% |
| $\Delta t_W$ | Output Pulse Width Difference | – | -10 | | 10 | ns | |
| $V_{OL}$ | Buffer Gate Voltage (low) +ve | 10 | 0.65 | | 0.95 | V | |
| $V_{OL}$ | Buffer Gate Voltage (low) -ve | 11 | 0.65 | | 0.95 | V | |
| $\Delta V_{OL}$ | Buffer Gate Voltage Difference | – | -0.15 | | 0.15 | V | |

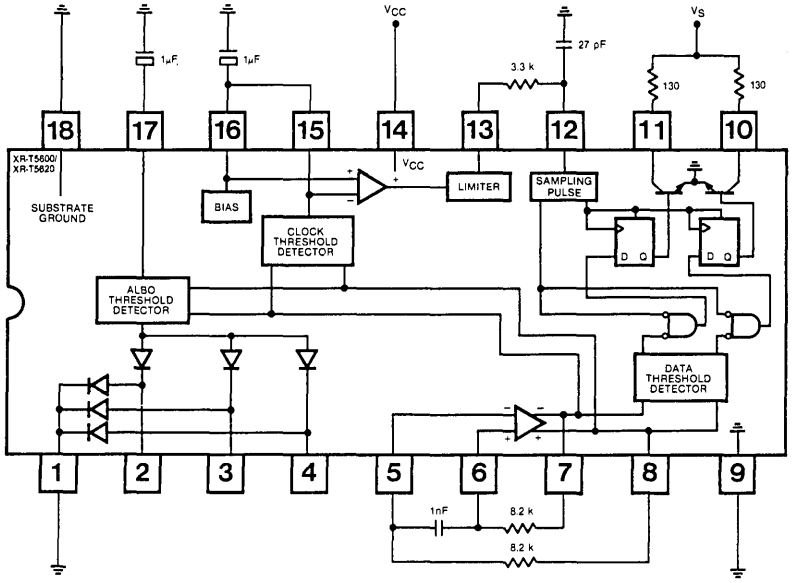



Figure 2. D.C. Parameter Test Circuit

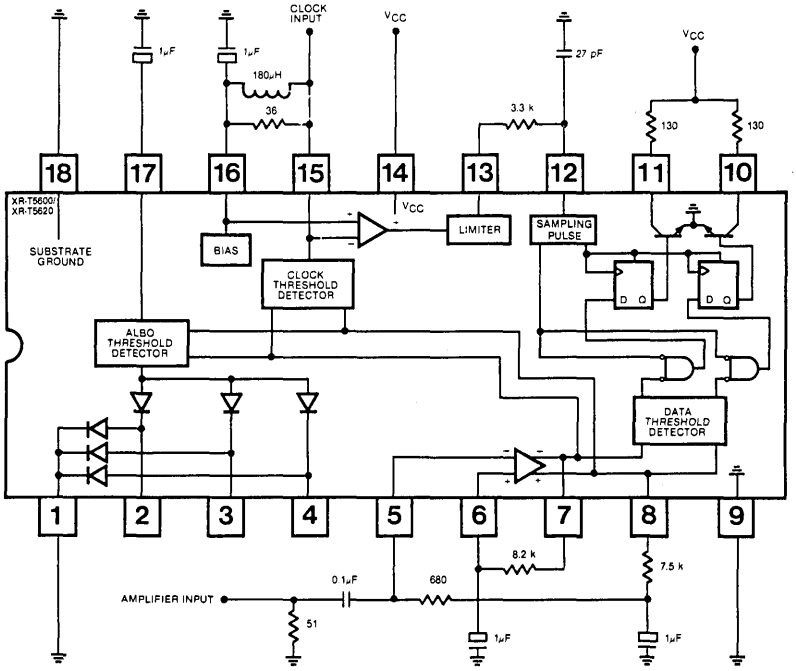



Figure 3. A.C. Parameter Test Circuit

| SYMBOL | PARAMETERS | PINS | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| SAMPLE PULSE WIDTH (Ref. Figure 4, Cy = 27 pF) | | | | | | | |
| | Sample Pulse Width | | | 10 | | ns | (See Notes 1...5) |

Notes:
1. The sample pulse width is the period during which the output latches are opened to accept a signal above the data hold at Pin 7 or 8 and cause a half-width output pulse at Pin 11 or 10 respectively.
2. Sample pulse width is specified with a 2.048 MHz TTL waveform at clock input (Pin 15) and a 2,400 MHz Schottky TTL waveform at amplifier input in the circuit of Figure 4. Figure 7 shows the relevant IC waveforms.
3. Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through ouput circuit to frequency counter.
4. Sample pulse width = X ns + (0,1 x measured frequency in kHz) ns where X is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5. X to be within the range of 10 nx < X < 12 ns. THis requires HF layout techniques with the amplifier operated closed loop.

| SAMPLE PULSE GENERATOR INPUT WAVEFORM (pin 12 - Ref. Figure 4, Cy = 40 pF) | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Output Pulse Frequency | 10,11 | 1,024 -100 ppm | 1,024 | 1,024 +100 ppm | MHz | (See Note 1) |

Note: 1. With 2,048 MHz ±100 ppm TTLwaveform at clock input. With half of above waveform frequency at amplifier input.

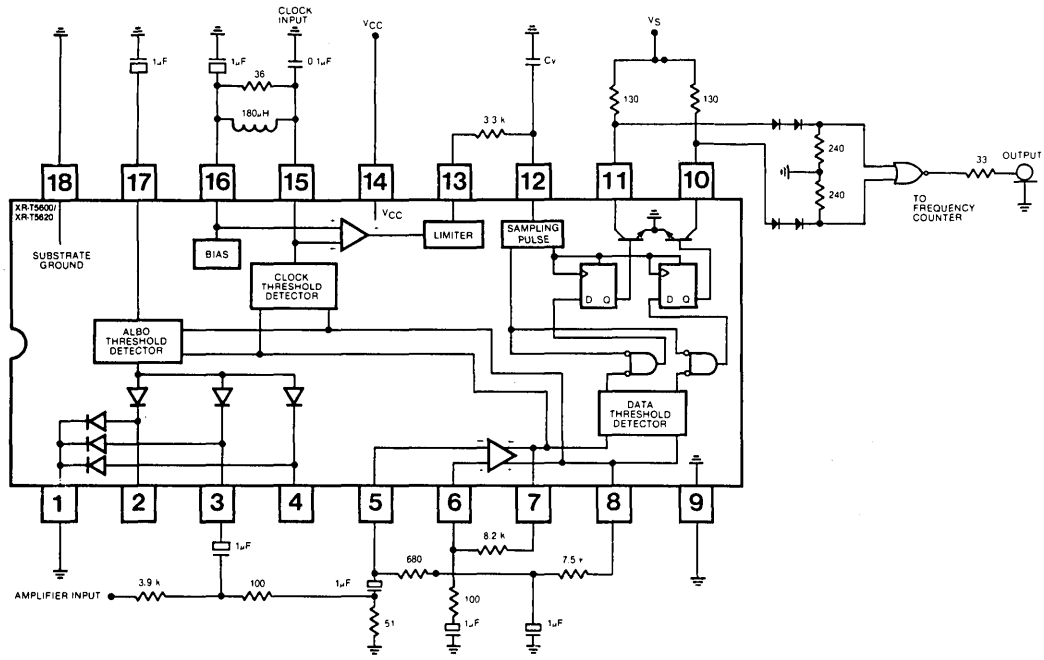



**Figure 4. Sampling Pulse Test Circuit**

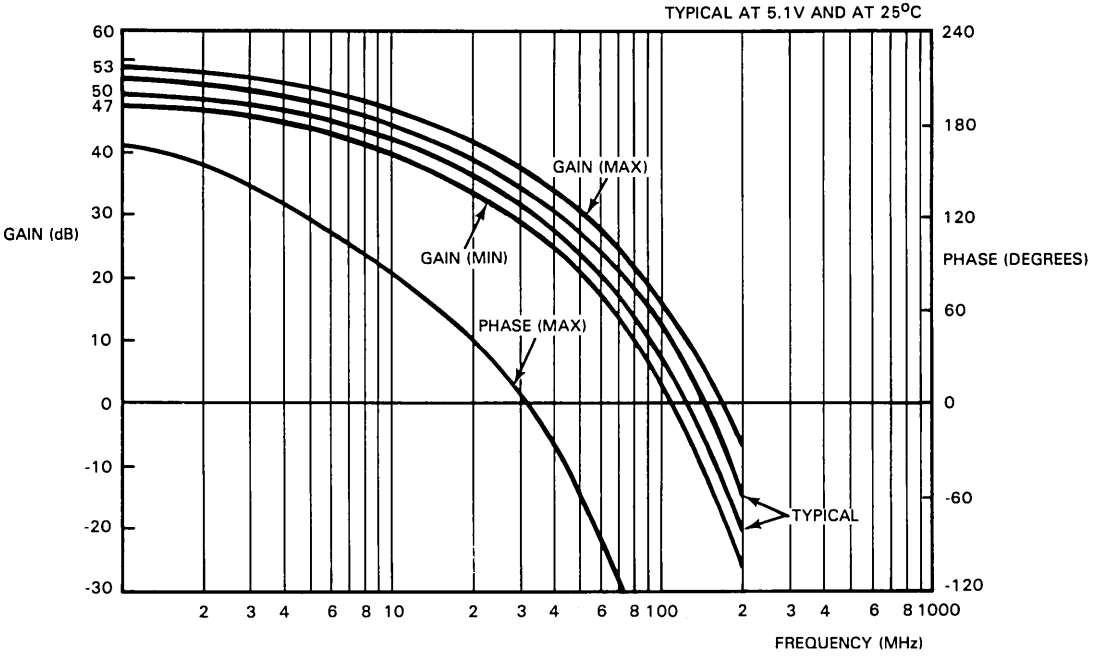



**Figure 5. Typical and Limiting Values of Gain and Phase**

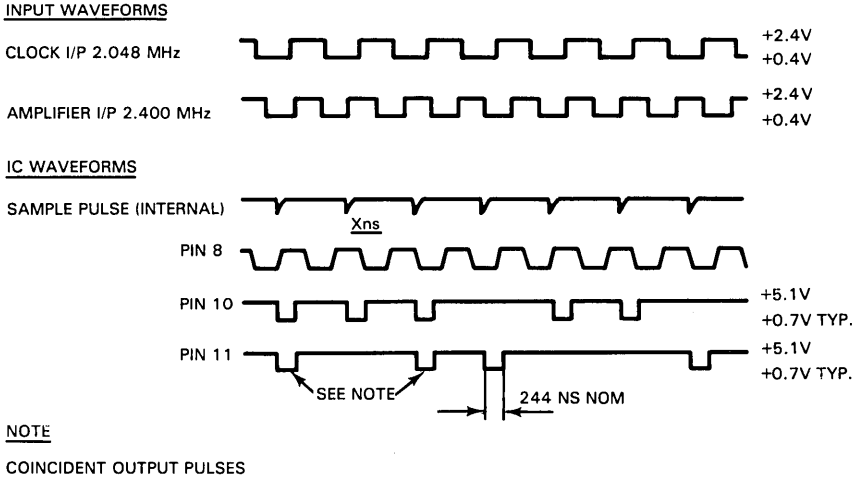
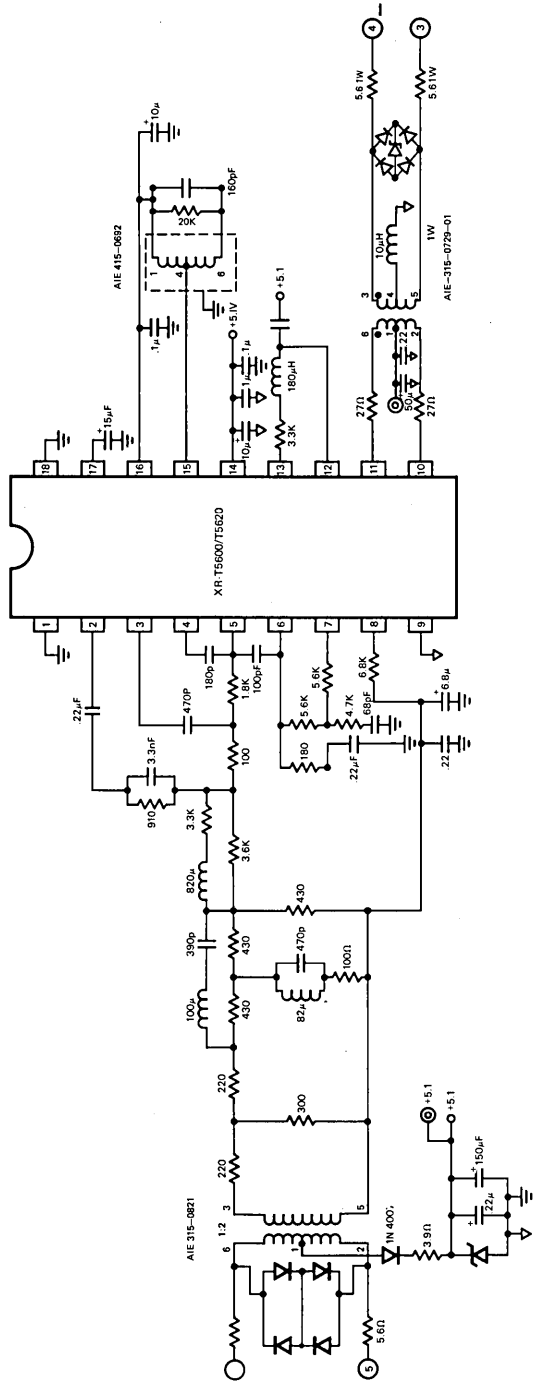
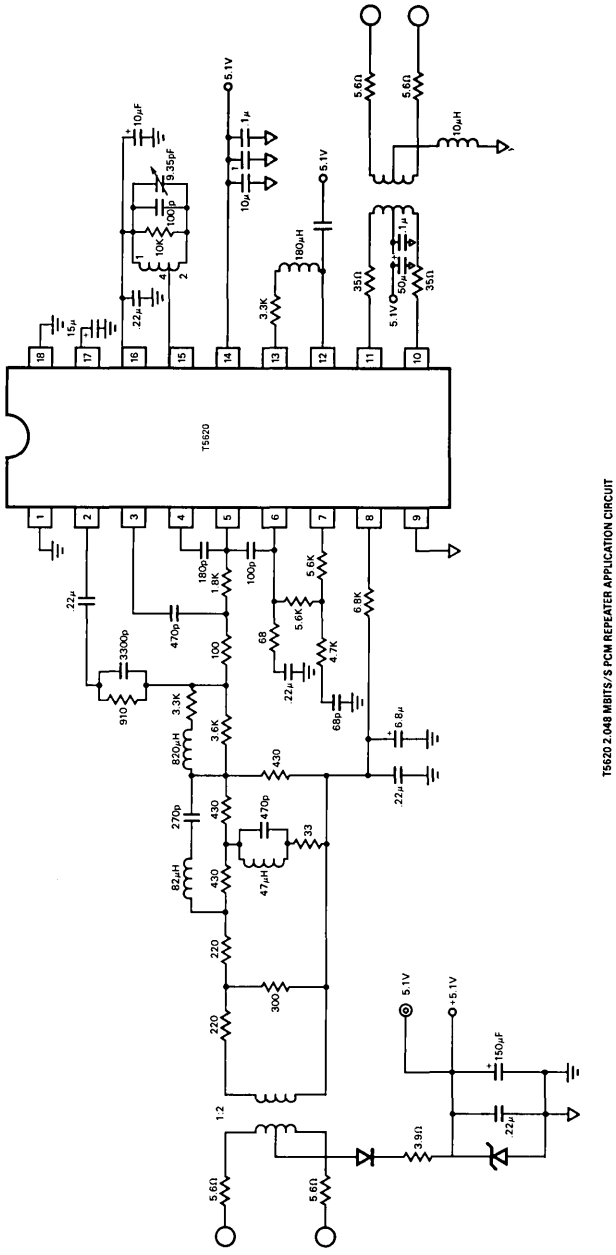



**Figure 6. IC Waveforms for Measuring Sampling Pulse Width**




T5600/T5620 1.544 M BITS/SEC REPEATER APPLICATION CIRCUIT




T5620 2.048 MBITS/S PCM REPEATER APPLICATION CIRCUIT