PCM Line Interface Chip

GENERAL DESCRIPTION

The XR-T5680 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 10 M Bits/s and the signal level to the receiver can be attenuated by −10 dB cable loss at half the bit rate. Total current consumption is between 27-46 mA at +5.0 V.

FEATURES

Single +5.0 V Supply
Receiver Input Can Be Either Balanced or Unbalanced
Up to 10 MBits/s Operation
TTL Compatible Interface

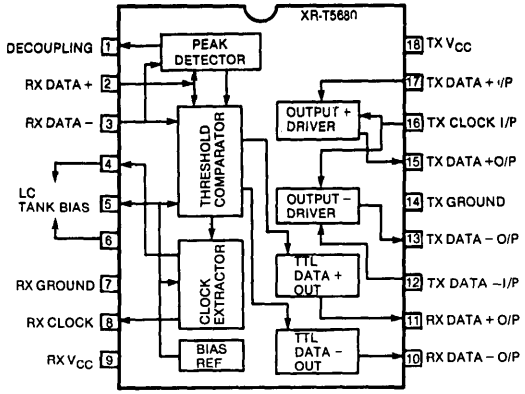
APPLICATIONS

T1, T1C, T148C, T2, 2048 & 8448 KBits/s
PCM Line Interface
CPI
DMI

ABSOULTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5680	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. A tank circuit tuned to the appropriate frequency is added to the later operation. The clock signal, data + data − all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40.0 mA. With full width data applied to the inputs together with a synchronized clock. The output will generate a bipolar signal when driving a centre-tapped transformer. A typical circuit diagram to XR-T5680 is shown in Figure 1, and the DC characteristics are indicated in the Electrical Characteristics chart.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, T_A = 0° - 70°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	Output Drivers Opens
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 4
*Clock Output/Low Level		0.4	0.8	V	Measured at Pin 8, I_{OL} = 1.0 mA
*Clock Output/High Level	3.0	3.6		V	Measured at Pin 8 I_{OH} = −400μA
*Data Output/Low Level		0.4	0.8	V	Measured at Pins 10,11 I_{OL} = 1.0 mA
*Data Output/High Level	3.0	3.6		V	Measured at Pins 10,11 I_{OH} = −400μA
Output Driver/Low Level	0.6		0.95	V	Measured at Pins 13,15 I_{OL} = 40 mA
Output Driver Current Sink			40	mA	Measured at Pins 13,15 V_{OL} = 0.95 V
Output Driver Rise Time		20	25	ns	Measured at Pins 13,15 with 150Ω Pull-up to +5.0 V CL = 15 pF
Output Driver Fall Time		20	25	ns	Measured at Pins 13,15 with 150Ω Pull-up to +5.0 V CL = 15 pF

*These output terminals are LS-TTL compatible.

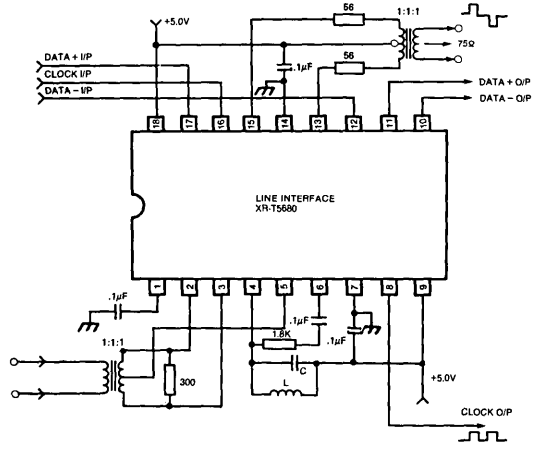


Figure 2. A recommended Circuit Diagram