

PCM Transceiver Chip

GENERAL DESCRIPTION

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CERDIP 18 pin package. The transceiver is designed for short line application (<-10 dB) such as in digital multiplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 Mbits/s so it covers T1, T148C, and Europe's 2.048 Mbit/s PCM system. The device is designed to operate over the temperature range of 0°C to $+70^{\circ}\text{C}$.

FEATURES

- Single +5.0 V Supply
- Receiver Can Accept Either Balanced or Unbalanced Inputs
- TTL Compatible Interface
- Transmitter and Receiver in One Package

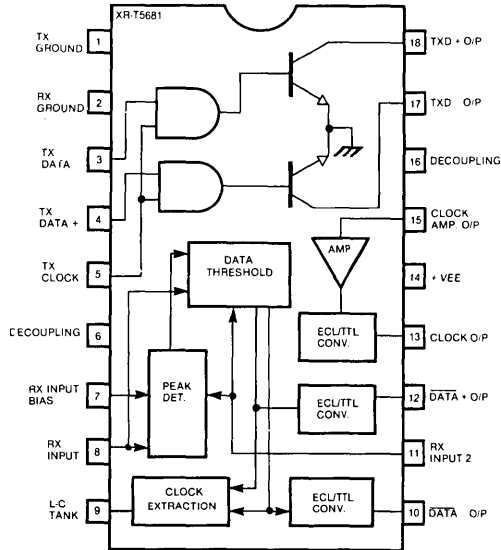
APPLICATIONS

- T1, T148C, and 2.048 Mbits/s PCM Line Interface
- CPI
- DMI

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to $+150^{\circ}\text{C}$
Operating Temperature	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5681	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The functions of the circuit terminals are defined in the Functional Block Diagram. At the receive direction, the incoming bipolar signal which has been attenuated and distorted by the cable is applied to the input of the peak detector. The variable threshold voltage produced by the peak detector controls the data comparator for P and N rails signal extractions. Timing information is obtained by means of a full wave rectifier and an L-C resonant circuit tuned at the appropriate frequency. All data and clock outputs are LSTTL compatible.

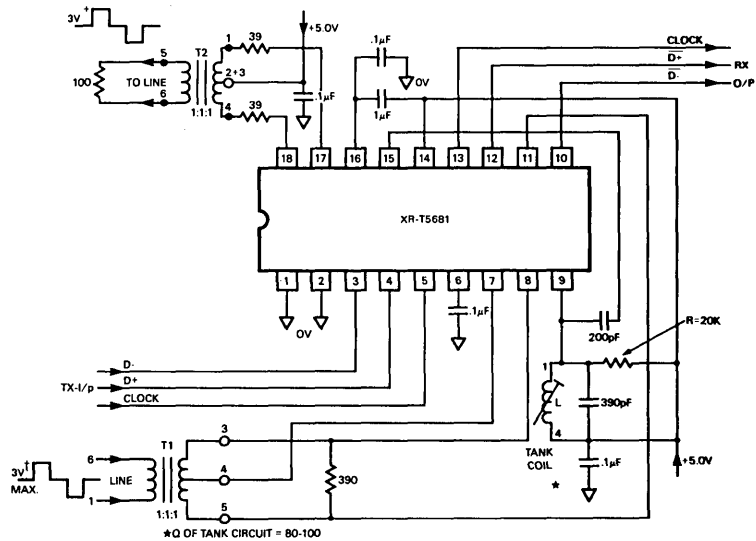
At the transmitter, the outputs have two identical non-saturating open collector stages which can drive the output line transformer directly with a maximum current of 40 mA. Full width, TTL compatible, P and N rail signals at the inputs and a 50% duty cycle TTL clock are needed to form the bipolar line signal at the secondary of the transformer. The output signal conforms to CCITT G.703 recommendation. A circuit diagram connected for 2048 K bits/s line interface application is shown in Figure 1.

XR-T5681

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC} = 5.0\text{ V}$, $T_A = 0^\circ\text{C} - +70^\circ\text{C}$, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	T_X Drivers Open
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 9,
Clock O/P/Low Level		0.3	0.8	V	Measured at Pin 13, $I_{OL} = 1.0\text{ mA}$
Clock O/P/High Level	3.0	4.3		V	Measured at Pin 13, $I_{OH} = 400\mu\text{A}$
Data O/P/Low Level		0.4	0.8	V	Measured at Pins 10,12, $I_{OL} = 1.0\text{ mA}$
Data O/P/High Level	3.0	4.5		V	Measured at Pin 10,12, $I_{OH} = 400\mu\text{A}$
Transmitter O/P/Low Level	0.6		0.95	V	Measured at Pin 13,15, $I_{OL} = 40\text{ mA}$
Transmitter O/P/Current Sink			40	mA	Measured at Pin 13,15, $V_{OL} = 0.95\text{V}$
Transmitter O/P/Rise Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to $+5.0\text{ V}$, $C_L = 15\text{ pF}$
Transmitter O/P/Fall Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to $+5.0\text{ V}$, $C_L = 15\text{ pF}$



T1 = AIE input transformer part no. 315-0785
 Tank Coil = AIE part no. 415-0804 (only terminal 1 & 4 being used).
 MAX Input voltage to T1 primary = 3 Vp or 6 Vp-p at 5.0 V supply.
 ADJUST L until min. clock jitter is obtained at pin 13.
 T2 = AIE part no. 318-0696

Figure 2. Circuit Connection Diagram for 2048Kbits/s operating